VLSI Technology

Communication Products Group

Data Sheet

ISDN
VLSI's ISDN Processor (VIPem) VNS80000B

Version 2.5
Date: Sept. 97

VLSI Proprietary

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Version History VIP P2 / VIPem

Document Version	Date	Changes
2.0		Specification of the VIP (P2) revised hardware.
2.1		1. Modified pin-out. 2. Updated boot procedure. 3. Minor editorial changes. 4. Modified Power-On reset threshold. 5. Updated specification of the LCD contrast control driver.
2.2		1. Updated registers map & register bit usage. 2. Updated I/O port multifunctional use. 3. Minor editorial changes. For detailed description of the changes see the 'VIP Delta List 2.1 -> 2.2'.
2.21		1. Ported document to PC Word 7.0. 2. Corrected page numbers in register map.
2.3		1. Corrected description of PIO pins. 2. Added description of bit length variation. 3. Corrected the values for the capacitor of the decoupling inputs. 4. Changed table for ConfTest pins (just the style). 5. Changed intS0_Reg bits [14:12]. 6. Changed ConfigS0_Reg bits [23:22]. 7. Changed resetS0_Reg bits [5,1]. 8. Updated SDCI timing picture. 9. Updated Errata List. 10. Minor editorial changes.
2.4		1. Added values for power specification. 2. Added 'Data flow of the incoming D-channel information'. 3. Added 'Data flow of the outgoing D-channel information. 4. Added 'Data flow of the B-channel audio samples'. 5. Added table for DRAM configurations. 6. Added description for SDO pin. 7. Changed G.711 (codec) to the correct expression 'VBAFE'. 8. Corrected t_4 for ROM/RAM timing. 9. Corrected values for caps connected to CREF and REF 10. Updated SDCI timing diagram, Removed 256 kHz and 4096 kHz SDCI frequencies. 11. Updated DRAM timing. 12. Removed 'Transmitted bit length' from intS0Reg. 13. Removed chapter 7 'VNS80000 Errata List'. 14. Removed chapter 8.1 'Specification History P1. 15. Removed chapter 8.3 'Delta Specification P1-P2'. 16. Minor editorial changes (incl. update of pictures for better reading).
2.5		1. Added text for start up in Hardware Configuration

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Document Version	Date	Changes
		2. Added clock switch bit in VBAFEReg 3. Added clock switch in features 4. Added clock switch in chapter 'clock oscillators and watchdog' 5. Corrected values for S0 Receiver Ref and Cref 6. Removed testS0_Reg 7. Minor editorial changes (incl. update of pictures for better reading).

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1. OVERVIEW

1.1 Application

The VLSI's ISDN Processor (VIP) is a single chip ISDN subscriber circuit which includes most of the circuitry required to implement an ISDN terminal conforming to the Euro - ISDN standards (ETS 300 012, ETS 300 0125, ETS 300 102-1). A typical system configuration is shown below.

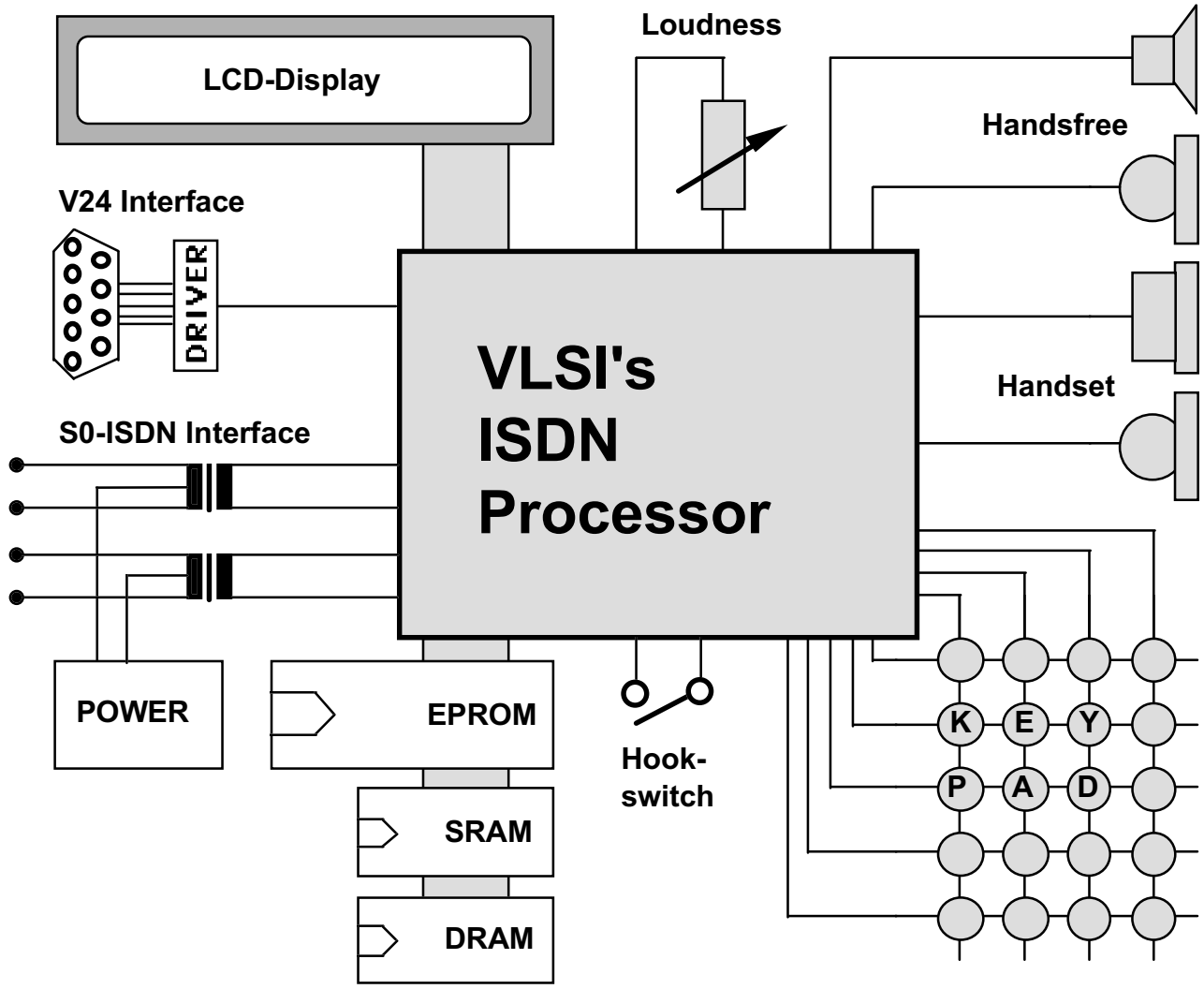

Figure 1-1: ISDN Telephone

Figure 1-1 shows the VIP in a typical terminal application. The S0 interface is active and in addition to the internal VBAFE (voice band analogue front end) an external CODEC is connected through the SDCI interface (Serial DSP / CODEC Interface). In this configuration the VIP is the master for the external CODEC.

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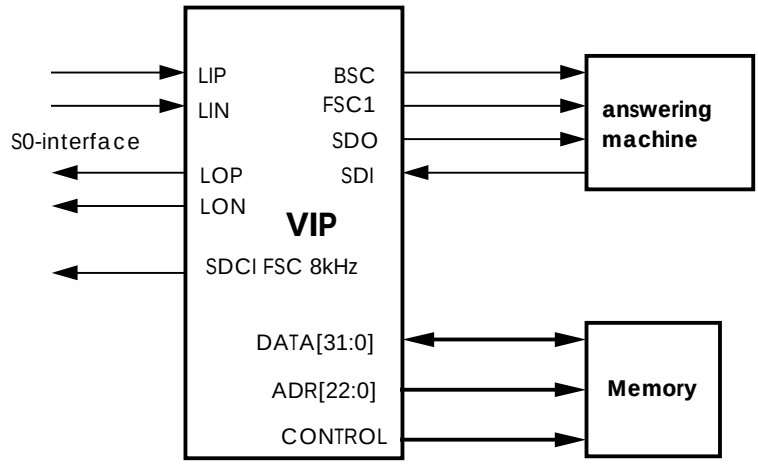

Figure 1-2: ISDN Terminal Application

Figure 1-2 shows the VIP in a PABX application. The timing for the SDCI interface is provide by the frame sync of the PCB highway. The S0 interface is also available.

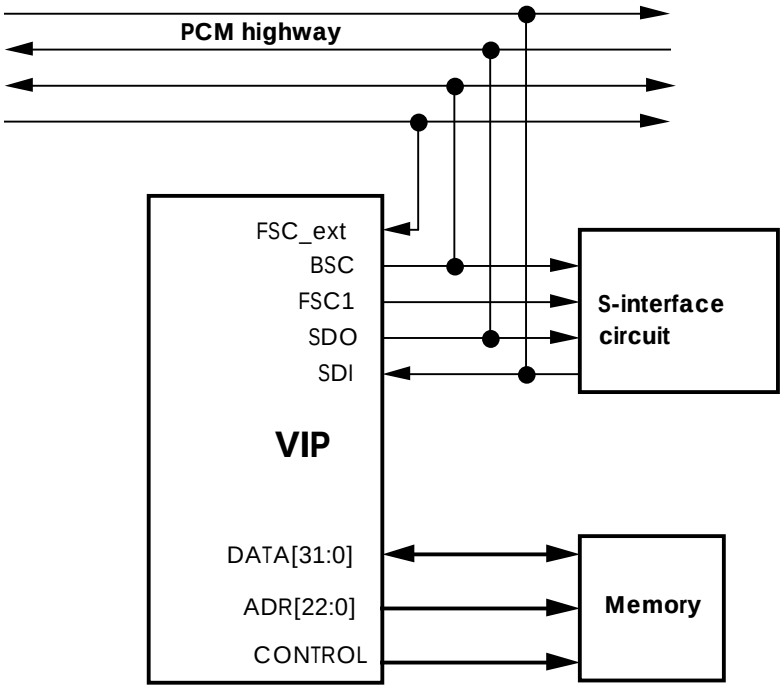

Figure 1-3: ISDN PABX Application

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1.2 Key Features and Benefits

FEATURES	BENEFITS
• Static 32-bit RISC controller with a 32-bit address-space running at 36.8 or 12.2 MHz (software controlled). Includes sophisticated debug features, instruction length 32- or 16-bit in a flexible memory-mapped architecture.	• Improves reliability, reduces system size and cost, very high performance, code efficiency, low power. Development tools available include C compiler, simulator and debugger.
• Internal 3k byte fast access general purpose SRAM (cache memory).	• Optimised execution of critical code.
• Internally programmable clock speed.	• Power conservation, improved reliability.
• Programmable power-down feature with event wake up.	• Power conservation, improved reliability.
• Supports 8/16/32-bit external SRAM/ ROM and 16/32-bit DRAM.	• Maximises memory system performance and utilisation.
• Supports a range of memory speeds from 54 ns - 1.2 us, with software programmable waitstate generation.	• Maximises memory system performance and utilisation, minimises cost.
• Interrupt controller, fully maskable for all peripherals.	• Flexibility and efficiency interrupt processing.
• S0 interface containing analogue transceiver, data-clock recovery and framing.	• Direct connection to S0 bus via transformer.
• D-channel data link controller with basic layer 2 function in hardware.	• Flexible system solution allowing easy implementation of either standard or proprietary protocols.
• VBAFE complete with programmable analogue front end, additional input and output and power down modes capable of driving directly the ringer- and loudhearing speaker.	• Direct connection to telephone hand-set and provision for hands-free or speaker phone, reduced system component count.
• Standard 64-bit serial DSP/CODEC interface.	• Allowing direct connection of up to three external devices like CODEC's, DSP's, etc.
• On-Chip boot volume	• Support of simple and effective program loading during production.
• Internal PCM format 14-bit linear.	• Low distortion.
• Two analogue to digital converters for volume control etc..	• Reduced system component count.
• n x 6 keypad scanner which generates interrupts on key press.	• Reduced processor overhead.
• Buffered parallel LCD controller interface and LED drive via bi-directional programmable I/O ports.	• Reduced system component count.
• Serial UART interface with baud rates from 1.2 kBaud to 230.4 kBaud.	• Flexible product architecture through industry standard interface.
• 2.5 ms timer.	• Operating system clock and event timing.
• Powerful test architecture.	• High fault coverage.
• Packaged in 160 pin MQFP.	• Easy to manufacture, inexpensive.

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2. FUNCTIONAL DESCRIPTION

2.1 Function

VLSI's ISDN Processor (VIP) provides a powerful programmable engine for ISDN subscriber communications. It combines a static 32-bit ARM7 RISC processor with a 16- or 32-bit instruction set including the embeddedICE (a on-chip debug facilities), a on-chip high speed memory, a S0 interface transceiver, a D-channel data link controller, a VBAFE, an industry standard serial interface (UART), a standard serial DSP/CODEC interface (SDCI), a keypad interface, interrupt controller and watchdog timer and power management features.

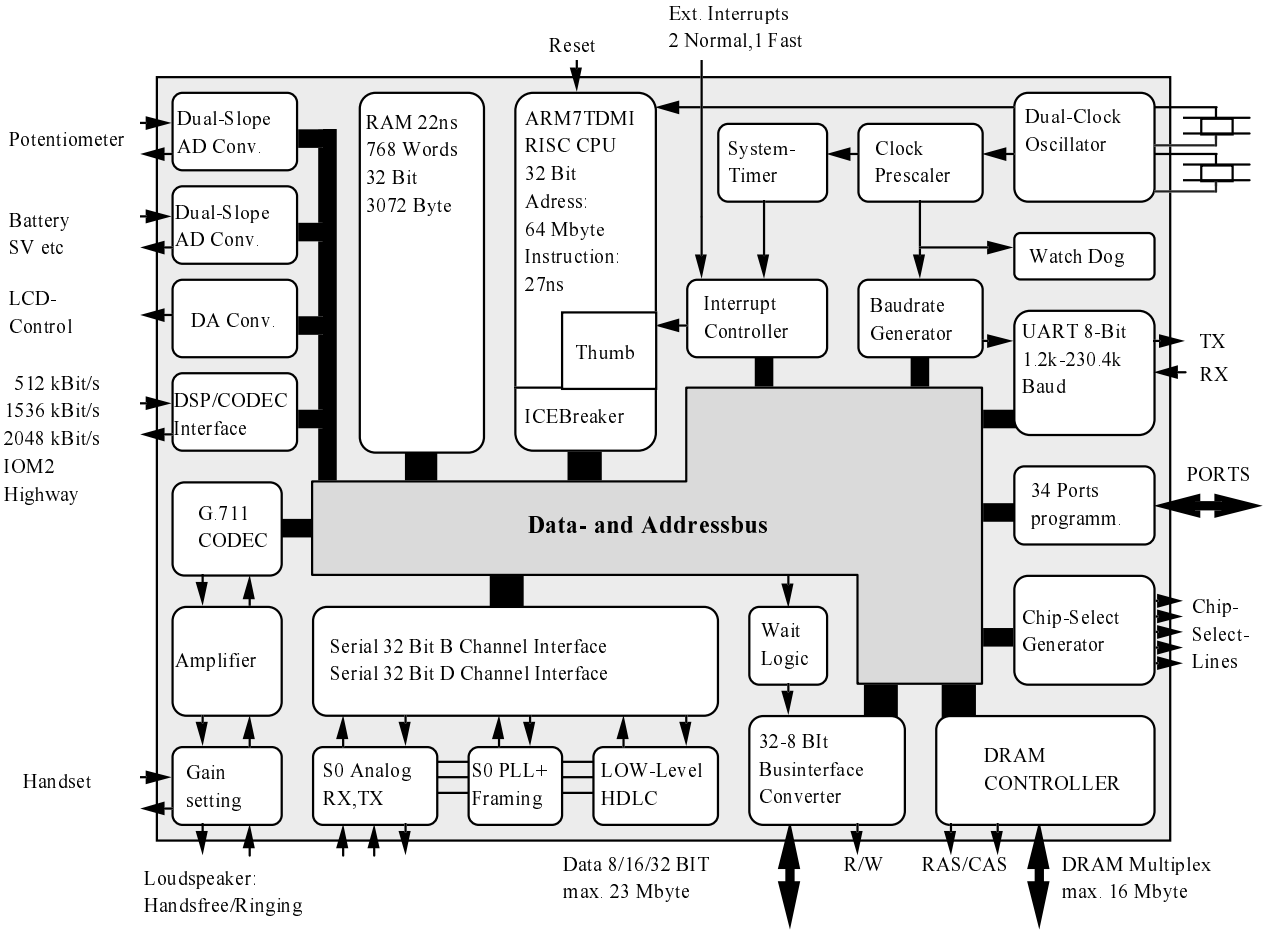

Figure 2-1: VIP Block Diagram

The on-chip S0 interface transceiver allows direct connection via a transformer and surge protection to the S0 bus. It contains all the basic Layer 1 functions such as data respectively clock recovery and framing. The D-channel data link controller provides most of the Layer 1 function and the basic Layer 2 frame formatting including zero-insertion/deletion, alarm condition detection, start-stop flag generation and detection. The remaining functions are easily performed by the powerful CPU.
The VBAFE contains an analogue front end that allows direct connection to the telephone hand-set. An additional input and output is provided for use in hands-free operation. This output is able to directly drive

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the loudspeaker in hands-free mode operation or for ringing. Both inputs and outputs have independently programmable gains. All amplification stages have a programmable power-down mode.
A flexible power management controller enables to vary the programmable system clock speed. This allows optimised processor performance and power consumption minimisation. Both features are fully software configurable.
In addition to the above the VIP also contains 2 ADC (integrating, single slope) as well as a number of ports (bi-directional programmable) and a DAC e.g. to be used for LCD contrast control.

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2.2 Pin List

Pin #	Signal Name	Type	Function
1	VDD	Supply	Digital power supply
2	VSS	Ground	Digital ground
3	ADR[15]	Output	Address [15]
4	ADR[14]	Output	Address [14]
5	ADR[12]	Output	Address [12]
6	ADR[13]	Output	Address [13]
7	ADR[7]	Output	Address [7]
8	ADR[8]	Output	Address [8]
9	ADR[6]	Output	Address [6]
10	ADR[9]	Output	Address [9]
11	VDD	Supply	Digital power supply
12	VSS	Ground	Digital ground
13	ADR[5]	Output	Address [5]
14	ADR[11]	Output	Address [11]
15	ADR[4]	Output	Address [4]
16	ADR[3]	Output	Address [3]
17	ADR[10]	Output	Address [10]
18	ADR[2]	Output	Address [2]
19	ADR[1]	Output	Address [1]
20	ADR[0]	Output	Address [0]
21	VDD	Supply	Digital power supply
22	VSS	Ground	Digital ground
23	D[7]	Bidirec	Data[7]
24	D[6]	Bidirec	Data[6]
25	D[0]	Bidirec	Data[0]
26	D[5]	Bidirec	Data[5]
27	D[1]	Bidirec	Data[1]
28	D[4]	Bidirec	Data[4]
29	D[2]	Bidirec	Data[2]
30	D[3]	Bidirec	Data[3]
31	VDD	Supply	Digital power supply
32	VSS	Ground	Digital ground
33	D[8]	Bidirec	Data[8]
34	D[9]	Bidirec	Data[9]
35	D[10]	Bidirec	Data[10]
36	D[11]	Bidirec	Data[11]
37	D[12]	Bidirec	Data[12]
38	D[13]	Bidirec	Data[13]
39	D[14]	Bidirec	Data[14]
40	D[15]	Bidirec	Data[15]

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Pin #	Signal Name	Type	Function
41	VDD	Supply	Digital power supply
42	VSS	Ground	Digital ground
43	Xin	Analogue	Quartz for the 36.864 MHz oscillator
44	Xout	Analogue	Quartz for the 36.864 MHz oscillator
45	VDD	Supply	Digital power supply
46	VSS	Ground	Digital ground
47	XinLP	Analogue	Quartz for the 460 kHz oscillator
48	XoutLP	Analogue	Quartz for the 460 kHz oscillator
49	UART_SIN	Input	Serial data in of the UART
50	UART_SOUT	Output	Serial data out of the UART
51	PIO2[7]	Bidirec	I/O port2 [7]
52	PIO2[6]	Bidirec	I/O port2 [6]
53	PIO2[5]	Bidirec	I/O port2 [5]
54	PIO2[4]	Bidirec	I/O port2 [4]
55	PIO2[3]	Bidirec	I/O port2 [3]
56	PIO2[2]	Bidirec	I/O port2 [2]
57	PIO2[1]	Bidirec	I/O port2 [1]
58	PIO2[0]	Bidirec	I/O port2 [0]
59	VDD	Supply	Digital power supply
60	VSS	Ground	Digital ground
61	PIO1[22]	Bidirec	I/O port1 [22]
62	PIO1[21]	Bidirec	I/O port1 [21]
63	PIO1[20]	Bidirec	I/O port1 [20]
64	PIO1[19]	Bidirec	I/O port1 [19]
65	PIO1[18]	Bidirec	I/O port1 [18]
66	PIO1[17]	Bidirec	I/O Port1 [17]
67	PIO1[16]	Bidirec	I/O port1 [16]
68	VDD	Supply	Digital power supply
69	VSS	Ground	Digital ground
70	PIO1[15]	Bidirec	I/O port1 [15]
71	PIO1[14]	Bidirec	I/O port1 [14]
72	PIO1[13]	Bidirec	I/O port1 [13]
73	PIO1[12]	Bidirec	I/O port1 [12]
74	PIO1[11]	Bidirec	I/O port1 [11]
75	PIO1[10]	Bidirec	I/O port1 [10]
76	PIO1[9]	Bidirec	I/O port1 [9]
77	PIO1[8]	Bidirec	I/O port1 [8]
78	VDD	Supply	Digital power supply
79	VSS	Ground	Digital ground
80	PIO1[7]	Bidirec	I/O port1 [7]

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Pin #	Signal Name	Type	Function
81	PIO1[6]	Bidirec	I/O port1 [6]
82	PIO1[5]	Bidirec	I/O port1 [5]
83	PIO1[4]	Bidirec	I/O port1 [4]
84	PIO1[3]	Bidirec	I/O port1 [3]
85	PIO1[2]	Bidirec	I/O port1 [2]
86	PIO1[1]	Bidirec	I/O Port1 [1]
87	PIO1[0]	Bidirec	I/O port1 [0]
88	VDD	Supply	Digital power supply
89	VSS	Ground	Digital ground
90	VSS_AMP_LS	Ground	Ground for the analogue front end
91	PwoLSn	Analogue	Loudspeaker output
92	VDD_AMP_LS	Supply	Supply for the analogue front end
93	PwoLSp	Analogue	Loudspeaker output
94	VSS_AMP_HS	Ground	Ground for the analogue front end
95	PwoHSn	Analogue	Handset earpiece output
96	VDD_AMP_HS	Analogue	Supply for the analogue front end
97	PwoHSp	Analogue	Handset earpiece output
98	PIO2[8]	Bidirec	I/O port2 [8]
99	PIO2[9]	Bidirec	I/O port2 [9]
100	PIO2[10]	Output	LCD contrast control
101	VDD	Supply	Digital power supply
102	VSS	Ground	Digital ground
103	KEYin[6]	Input	Keypad column line[6]
104	KEYin[5]	Input	Keypad column line[5]
105	KEYin[4]	Input	Keypad column line[4]
106	KEYin[3]	Input	Keypad column line[3]
107	KEYin[2]	Input	Keypad column line[2]
108	KEYin[1]	Input	Keypad column line[1]
109	ConfTest[1]	Input	hardware configuration signal[1]
110	ConfTest[2]	Input	hardware configuration signal[2]
111	ConfTest[3]	Input	hardware configuration signal[3]
112	ConfTest[4]	Input	hardware configuration signal[4]
113	ConfTest[5]	Input	hardware configuration signal[5]
114	Vrefn	Analogue	Test and de-coupling PIN for the AFE analogue front end
115	Vrefp	Analogue	Test and de-coupling PIN for the analogue front end reference voltage
116	Auxin	Analogue	Hands-free microphone input
117	Auxip	Analogue	Hands-free microphone input
118	Vxin	Analogue	Hand-set microphone input
119	Vxip	Analogue	Hand-set microphone input
120	VDD_AVD	Supply	Supply for the analogue front end

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Pin #	Signal Name	Type	Function
121	VSS_AVS	Ground	Ground for the analogue front end
122	ADC1in	Analogue	Analogue digital converter #1 input
123	ADC2in	Analogue	Analogue digital converter #2 input
124	VSS_AVS	Ground	Ground for the analogue front end
125	LIP	Analogue	S0 positive input signal
126	LIN	Analogue	S0 negative input signal
127	Cref	Analogue	Decoupling capacitor #1
128	Ref	Analogue	Decoupling capacitor #2
129	VSS_AVS_S0	Ground	Ground for the S0 receiver
130	VDD_AVD_S0	Supply	Power supply for the S0 receiver
131	GND	NC	Not connected
132	GND	NC	Not connected
133	VSS	Ground	Digital ground
134	LON	Output	SO negative output signal, open drain
135	LOP	Output	SO positive output signal, open drain
136	GND	NC	Not connected
137	GND	NC	Not connected
138	VDD	Supply	Digital power supply
139	VSS	Ground	Digital ground
140	Reset	Input	Reset, active low
141	FSC1	Output	Frames Sync 1 of the SDCI interface
142	BSCK	Bidirec	Bit clock of the SDCI interface
143	SDO	Output	Serial data out of the SDCI interface
144	SDI	Input	Serial data in of the SDCI interface
145	VDD	Supply	Digital power supply
146	VSS	Ground	Digital ground
147	/WR0	Output	Memory write #0
148	/WR1	Output	Memory write #1
149	/RDio	Output	I/O read spike free
150	/RD	Output	Memory read
151	/CS16boot	Output	Chip select for 16-bit boot-EPROM
152	/CS8	Output	Chip select for 8-bit EPROM
153	/CS8boot	Output	Chip select for 8-bit boot-EPROM
154	VDD	Supply	Digital power supply
155	VSS	Ground	Digital ground
156	ADR[20]	Output	Address [20]
157	ADR[19]	Output	Address [19]
158	ADR[18]	Output	Address [18]
159	ADR[17]	Output	Address [17]
160	ADR[16]	Output	Address [16]

Table 2-1: PIN List

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3. SUB-MODULE DESCRIPTION

3.1 ARM CPU and SRAM

3.1.1 ARM

The ARM7TDMI is a member of the Advanced RISC Machines (ARM) family of general purpose 32-bit microprocessors, which offer high performance for very low power consumption and size.
The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective chip.
Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.
The memory interface has been designed to allow the performance potential to be realised without incurring high costs in the memory system. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals facilitate the exploitation of the fast local access modes offered by industry standard dynamic RAMs.

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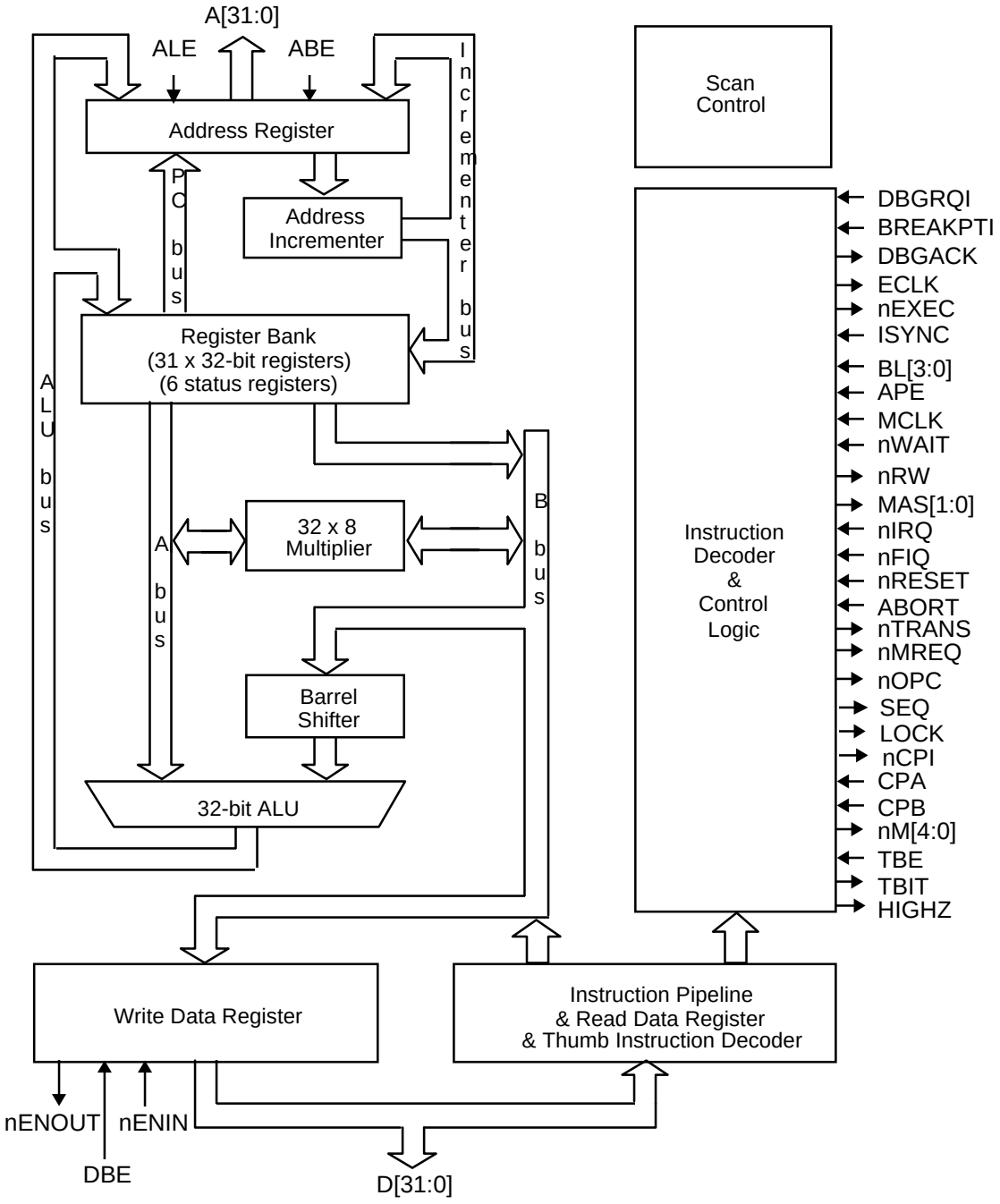

Figure 3-1: ARM Block Diagram

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3.1.1.1 Thumb Concept

The ARM7TDMI processor employs a unique architectural strategy known as THUMB, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue. The key idea behind THUMB is that of a super-reduced instruction set. Essentially, the ARM7TDMI processor has two instruction sets:

- the standard 32-bit ARM set
- a 16-bit THUMB set

The THUMB set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because THUMB code operates on the same 32-bit register set as ARM code.

THUMB code is able to provide up to 65% of the code size of ARM, and 160% of the performance of an equivalent ARM processor connected to a 16-bit memory system.

THUMB instructions operate with the standard ARM register configuration, allowing excellent interoperability between ARM and THUMB states. Each 16-bit THUMB instruction has a corresponding 32-bit ARM instruction with the same effect on the processor model.

The major advantage of a 32-bit (ARM) architecture over a 16-bit architecture is its ability to manipulate 32-bit integers with single instructions, and to address a large address space efficiently. When processing 32-bit data, a 16-bit architecture will take at least two instructions to perform the same task as a single ARM instruction.

However, not all the code in a program will process 32-bit data (for example, code that performs character string handling), and some instructions, like branches, do not process any data at all.

If a 16-bit architecture only has 16-bit instructions, and a 32-bit architecture only has 32-bit instructions, then overall the 16-bit architecture will have better code density, and better than one half the performance of the 32-bit architecture. Clearly 32-bit performance comes at the cost of code density.

THUMB breaks this constraint by implementing a 16-bit instruction length on a 32-bit architecture, making the processing of 32-bit data efficient with a compact instruction coding. This provides far better performance than a 16-bit architecture, with better code density than a 32-bit architecture.

THUMB also has a major advantage over other 32-bit architectures with 16-bit instructions. This is the ability to switch back to full ARM code and execute at full speed. Thus critical loops for applications such as

- fast interrupts
- DSP algorithms

can be coded using the full ARM instruction set, and linked with THUMB code. The overhead of switching from THUMB code to ARM code is folded into sub-routine entry time. Various portions of a system can be optimised for speed or for code density by switching between THUMB and ARM execution as appropriate.

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3.1.1.2 EmbeddedICE

ARM7TDMI contains hardware extensions for advanced debugging features. These are intended to ease the user's development of application software, operating systems, and the hardware itself.

The debug extensions allow the core to be stopped either on a given instruction fetch (breakpoint) or data access (watchpoint), or asynchronously by a debug-request. When this happens, ARM7TDMI is said to be in debug state. At this point, the core's internal state and the system's external state may be examined. Once examination is complete, the core and system state may be restored and program execution resumed.

ARM7TDMI is forced into debug state either by a request on one of the external debug interface signals, or by an internal functional unit known as embeddedICE. Once in debug state, the core isolates itself from the memory system. The core can then be examined while all other system activity continues as normal.

ARM7TDMI's internal state is examined via a JTAG-style serial interface, which allows instructions to be serially inserted into the core's pipeline without using the external data bus. Thus, when in debug state, a store-multiple (STM) could be inserted into the instruction pipeline and this would dump the contents of ARM7TDMI's registers. This data can be serially shifted out without affecting the rest of the system.

The ARM7TDMI-ICEbreaker module, provides integrated on-chip debug support for the ARM7TDMI core. ICEbreaker is programmed in a serial fashion using the ARM7TDMI TAP (Test Access Port) controller. It consists of two real-time watchpoint units, together with a control and status register. One or both of the watchpoint units can be programmed to halt the execution of instructions by the ARM7TDMI core via its BREAKPT signal. Execution is halted when a match occurs between the values programmed into ICEbreaker and the values currently appearing on the address bus, data bus and various control signals. Any bit can be masked so that its value does not affect the comparison.

Either watchpoint unit can be configured to be a watchpoint (monitoring data accesses) or a breakpoint (monitoring instruction fetches). Watchpoints and breakpoints can be made to be data-dependent.

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3.1.2 SRAM

The integrated high speed static RAM with a capacity of 3 kBytes is organised as 768 32-bit words. Read operations are executed without any wait states. Write operations on the other hand require a wait state; the access time is 27 ns. This memory is used for time- or performance-critical code only (e.g. fast interrupt execution or DSP like operations).

3.1.3 On Chip Boot Volume

To simplify the production process of VIP based products an on chip boot volume has been implemented. This boot volume supports the individualisation of Flash-EPROM's during the production process. After a watch dog retrigger the boot volume procedure expect data to be loaded via the UART. These bytes get stored into the internal SRAM starting at address 0x100. After receiving 1796 (0x704) bytes the code at address 0x100 will be executed.

On activation of the on chip boot volume procedure by the hardware configuration pins ConfTest[5:1] the following process get started:

- Power up reset / watch-dog retrigger
- UART send '@'
- UART expect line feed character (0x0A)
- UART expect data
- Data from the UART will be loaded into the internal SRAM starting at address 100 hex
- After receiving of 1796 (0x704) bytes address 256 (0x100) will be executed

For the communication between the VIP and the host the following settings are used:

- 9600 baud
- 8 bit, no parity, 1 stop bit, no protocol or handshake

The watchdog is set to 2.56 sec. To send the 0x704 bytes at 9600 baud will take at least 1.9s.

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3.2 Memory Interface

The memory interface allows the connection of 8-, 16- or 32-bit static RAM/ROM and 16-bit or 32-bit DRAMs. There is always a 8-bit memory area (starting 0x100000). For the upper memory area (starting 0x1000000) it can be selected by the ConfTest pins weather 16- or 32-bit access is used.

Write access to the internal memory and the registers is only 32 bit wide possible.

23 Mbytes static RAM/ROM and 16 Mbytes dynamic RAM are accessible. In each of the four ranges, the wait states are programmable in sixteen steps, ranging from one to 48 wait states. After reset the wait state count ten respectively 298.3 ns is used. The DRAM timing controller supports both non sequential and fast page mode DRAM access.

The addressing range associated with the CS lines is fixed.

Name	Function	Comment
A[20:0]	Address lines	Output
A[21]	Address line	Output or programmable I/O port
A[22]	Address line	Output or programmable I/O port
D[15:0]	Data lines	Bidirec.
D[31:16]	Data lines	Bidirec. or programmable I/O port
/RAS	DRAM row address select	Output or programmable I/O port
/CAS0	DRAM select #0	Output or programmable I/O port
/CAS1	DRAM select #1	Output or programmable I/O port
/RD	Memory read	Output
/RDio	I/O read	Output, spike free I/O read
/WR0	Memory write # 0 select	Output
/WR1	Memory write # 1 select	Output
/CS8boot	Chip select for 8-bit boot-EPROM	Output
/CS8	Chip select for 8-bit EPROM/SRAM	Output
/CS16boot	Chip select for 16/32-bit boot-EPROM	Output
/CS16a	Chip select for 16/32-bit ROM/SRAM *)	Output or programmable I/O port
/CS16b	Chip select for 16/32-bit ROM/SRAM *)	Output or programmable I/O port
/CS16C	Chip select for 16/32-bit ROM/SRAM *)	Output or programmable I/O port

Table 3-1: Memory Signals

*) Using 2(4) 8-bit RAMs for the 16(32)-bit memory area:
This configuration allows 32-bit (STR), 16-bit (STRH) or 8-bit (STRB) write accesses to the memory. As it cannot determined which type of access is used by the C-compiler (e.g. to write variables of type 'char'), this seems to be the safest approach to build RAM, which can be byte-wide accessed.
WR0 is used to strobe data in the even addresses of the memory, WR1 for odd addresses.
For 32-bit wide memory, build of 8 bit RAMs, external logic is necessary.
Using 16(32)-bit RAM in the 16(32)-bit memory area:
In this configuration, no byte write accesses is supported, unless special RAMs employed with several special chip select signals for byte access are used. For 32-bit memory, it is even not possible to write 16-bit words only. During such an accesses, always the full word is written determined by the strobe signal WR0. The content of the memory which should be retained (e.g. 24-bit in case of an 8-bit write access to 32-bit memory) is destroyed.

The boot location is selectable by pin strapping for further details see chapter 'Hardware Configuration'. A write enable decoder separates byte from word writing. 9 chip select signals together with fully decoded address ranges for RAM, ROM and I/O usage provide high flexibility.

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RAS and CAS signals are generated. The address multiplexed minimal system has a software refresh. DRAM's with 256 k to 4 M address organisation are supported. Square ROW/CAS-Address from nine to eleven bits are supported. For further details see chapter 'DRAM Write' at page 79.

Figure 3-2 shows the resulting memory map.

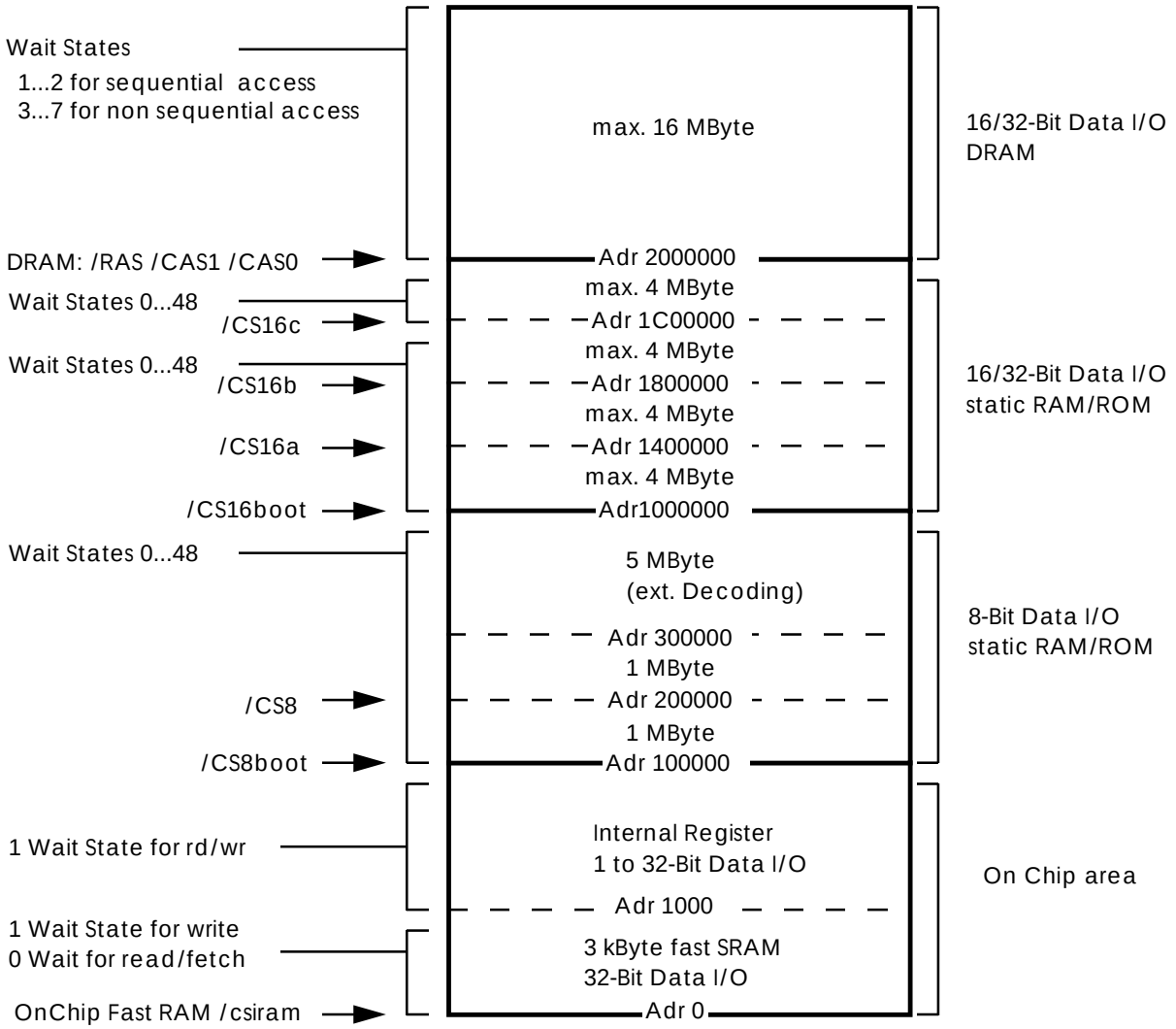

Figure 3-2: Memory Map

	used addresses	16 bit wide access	32 bit wide access
2* 9 address lines	256 k	512 kByte = 4 MBit	1 MByte = 8 MBit
2* 10 address lines	1 M	2 MByte = 16 MBit	4 MByte = 32 MBit
2* 11 address lines	4 M	8 Mbyte = 64 MBit	16 MByte = 128 MBit

Table 3-2 : Possible DRAM configurations

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3.3 Interrupt Controller

External and internal interrupt signals are detected and can be read from the internal status register of the interrupt controller. The interrupt controller has two independent interrupt levels. One interrupt level is for the ARM7 fast interrupt and the other interrupt level is for the ARM7 normal interrupt.
The fast interrupt controller has seven interrupt sources. The latency time for these interrupts is about 1 us. All fast interrupts are maskable. The fast interrupts are latched.
The normal interrupt controller has fourteen interrupt sources which are all maskable. The normal interrupts are latched. The latency of the normal interrupts depend on the size of the fast interrupt routine (i.e. the time that this routine uses).

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3.4 S0 Interface

3.4.1 S0 Framer

Two 26-bit parallel full duplex data register are the interface between the internal data bus and the analogue S0 front end. All bits in the S0 frame are accessible. Automatic frame generation and detection including insertion and deletion of the DC balancing bits is performed.

The DPLL driven by the zero crossing detector of the receiver generates the bit and frame clocks, with low output jitter and a search mode for quick synchronisation.

3.4.2 D-Channel Controller

The D-channel controller performs the D1-, D2- and Echo bit processing (see S0 Data Register). A low level HDLC processor does the Layer2 frame generation for the D-channel including start- and stop flag generation and detection, zero insertion and deletion.
Using the powerful ARM CPU, all processing and generation of the data octets between the start- and stop flags- including the frame check sequence - can be performed in software. The data transfer between CPU and D-channel controller is done via a full duplex 4-byte deep FIFO.

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3.4.2.1 Data flow of the outgoing D-channel information

The following description assumes a software structure that is based on the OSI layer model, where layer 1 is the physical layer and layer 2 is the data link layer. The D-channel controller is activated in the idcReg.

Layer 2 of the software requests a D-channel frame to be sent. This request has to be handled in the Fast Interrupt (FIRQ) Handler. The FIRQ handler has to check the number of consecutive 1 received in the D-channel. This number can be read from the configS0_Reg [23:20]. If the D-channel is available the FIRQ handler can write the first 4 bytes to the D_TxReg and store the remaining bytes in a software fifo. To start the D-channel transmission the idcReg has to be set accordingly.

The data in the D_TxReg will then be processed by the hardware. The opening and closing flag are added and the '0' insertion is done as required in the LAP-D protocol. Then these bits are placed in the D-channel bits in the S0_TxDataReg. Then this half frame is automatically transmitted.

When the first 4 bytes are transmitted the normal interrupt 'D-channel TxEmpty' is issued and the next bytes from the software fifo can be written to the D_TxReg. If the last bytes of the message are to be send the number of bytes has to be set accordingly in the idcReg. The closing flag will be generated by the hardware.

A normal interrupt 'D-channel TxCompl' indicates that the last byte of the layer 2 frame has been sent.

If a collision occurs on the D-channel the normal interrupt 'D-channel TxAbort' is issued by the VIP and the D-channel transmission is stopped immediately by the hardware. The retransmission of the frame has to be handled by the software.

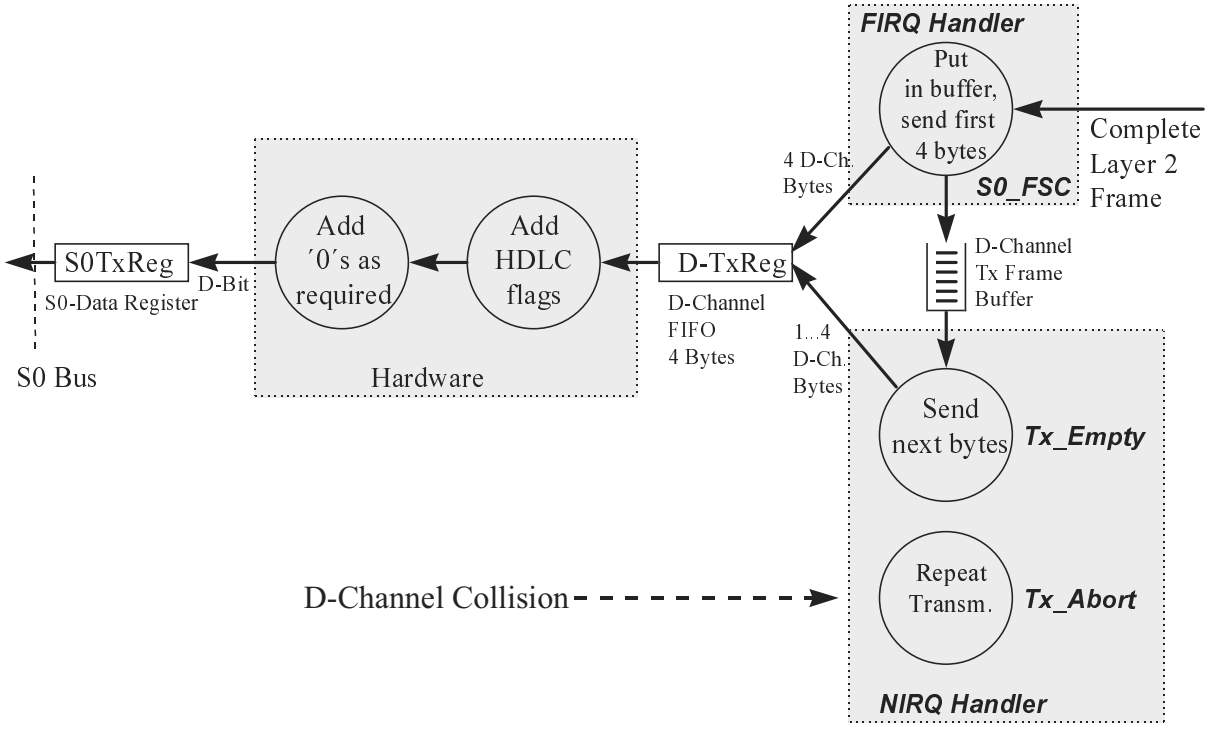

Figure 3-3 : D-channel Tx flow

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3.4.2.2 Data flow of the incoming D-channel information

If the D-channel controller is activated in the idcReg the D-channel bits received in the S0 frame are extracted automatically. The '0' deletion is done and the flags are stripped. The received bytes are then stored in the D_RxReg. When 4 complete bytes were received a 'D-channel RxFull' interrupt is generated and the D-channel bytes can be read from the D_RxReg.

When a closing flag was detected by the hardware a 'D-channel RxSFD' interrupt is issued. The remaining data bytes are stored in the D_RxReg. The number of valid bits can be read from the idcReg. The D-channel frame has been received completely and can be sent to the layer 2 software.

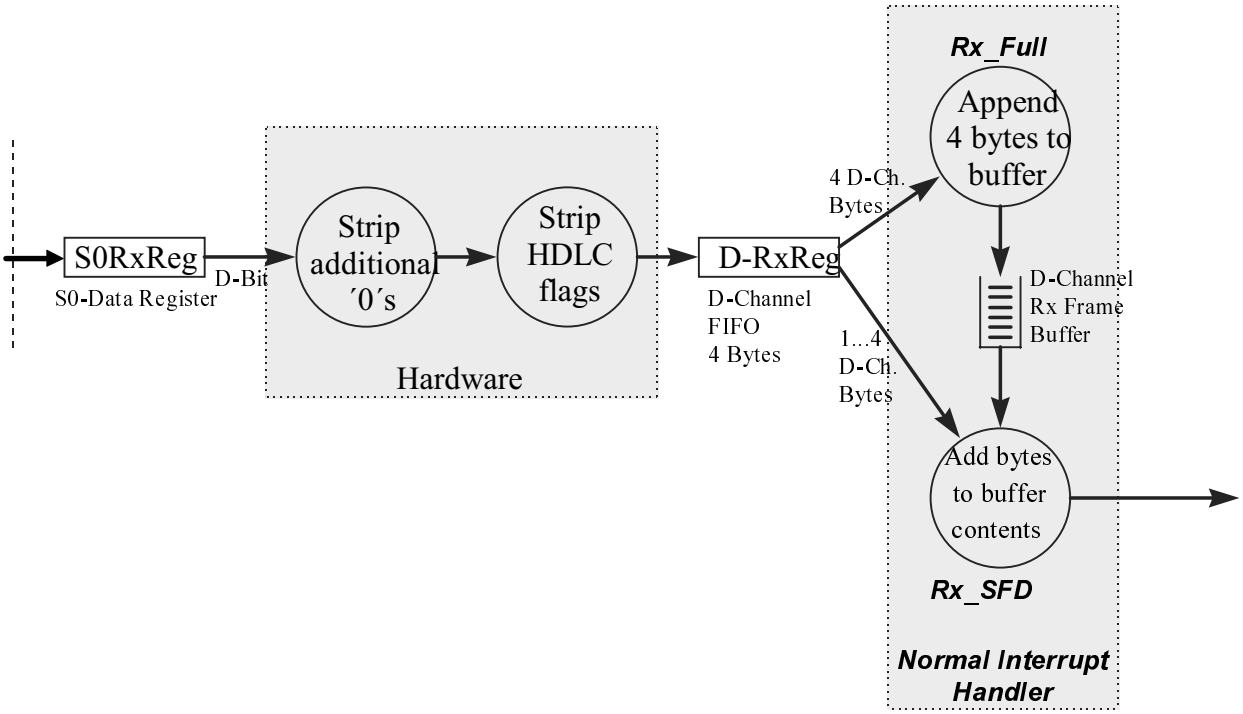

Figure 3-4 D-channel Rx flow

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3.4.3 S0 Transmitter

Features

- Pulse shaping to fit template with nominal loading (200 Ω on the driver side)
- Pulse shaping to fit template with 400 W load (or 1600 W on the driver side)
- The line driver is coupled to a standard (2:2):(1:1) transformer
- Meets I.430 layer 1 specification
- Current limiting capability
- Supports short passive bus, extended passive bus and point-to-point systems

The line driver in conjunction with the transformer and the external components (see Figure 3-5) generates controlled positive and negative pulses. A 12.288 MHz clock *) is used for pulse shaping. When driving a pulse, the driver can be modelled as a current source. The nominal value of current is 7.5 mA. Therefore the pulse amplitude is precisely controlled and the nominal level at the line driver output is ±1.5 V and ± 750 mV at the transformer outputs with a 50 Ω load.

*) this frequency is derived from the 36.864 MHz oscillator.

Special care has been taken to minimise the influence of the driver on the zero-crossing detector. The receiver can attain zero crossing sensitivity better than ±10 mV whilst the driver is driving a +/ 1.5 V pulse. This requires a decoupling of nearly 40 dB, and is accomplished by careful layout isolation, use of pseudo-differential structures and by using separate supply pads.

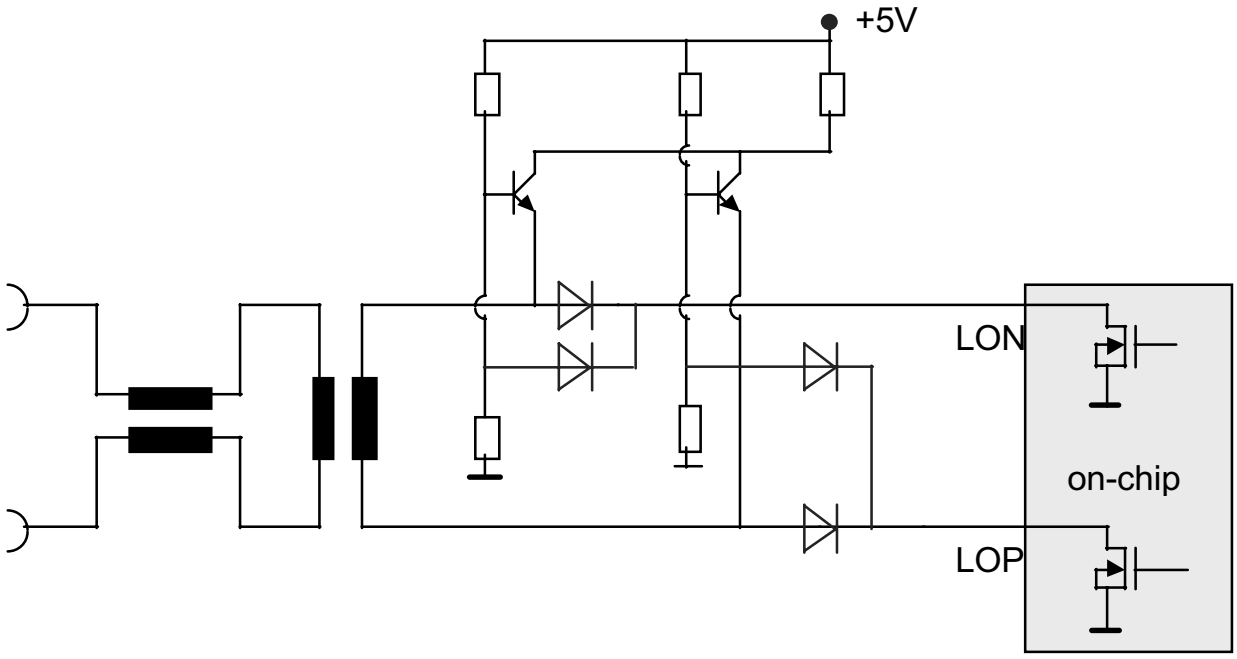

Figure 3-5: S0 Transmitter

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3.4.4 S0 Receiver

Features

- Zero-crossing detection with hysteresis selectable in four step between ± 6.7% to ± 26.7 % of the programmable input threshold.
- positive / negative pulse detection selectable in four step between ± 33% to ± 100% of the nominal pulse amplitude.
- Power-down mode leaves only the zero-crossing detector powered up in order to save power.

On the chip the signals from the secondary side of the 1:2 receive transformer - LIN and LIP - are connected to current input stage followed by a zero crossing and a data detection comparator. The nominal threshold of the zero crossing detection and the data detection are relative to the input current and are set by the external serial resistors.

The hysteresis of the zero crossing detector can be set in four steps between ± 6.7% and ± 26.7% of the nominal threshold to get the best compromise between high frequency noise rejection and input sensitivity. Respectively the threshold for the input data can set in four steps between ± 33% and ± 100 % of the nominal threshold.
Wakeup mode is initialised by the zero-crossing detector upon detection of activity on the line during sleep mode.

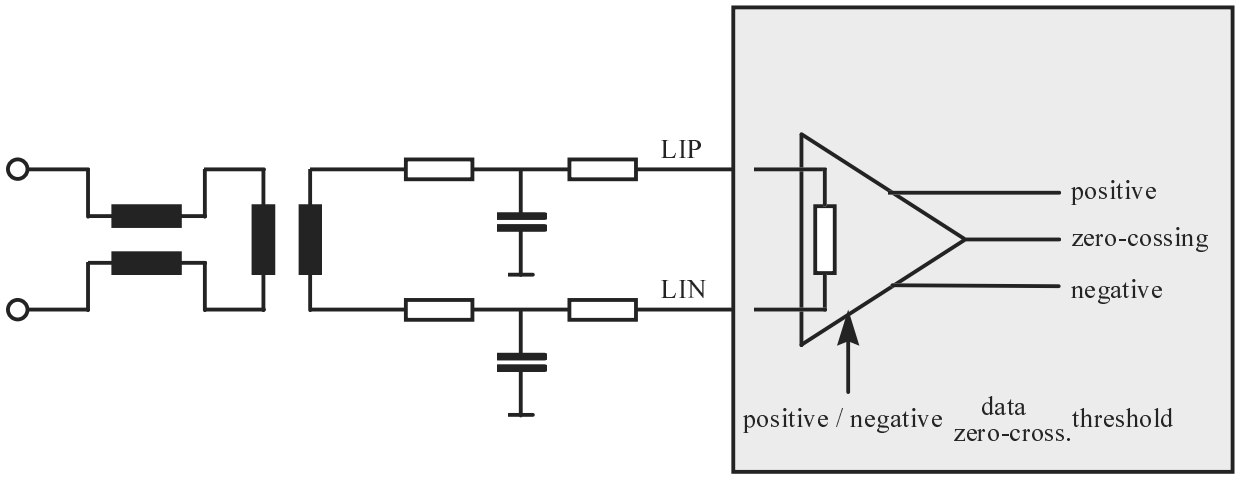

Figure 3-6: S0 Receiver

3.4.5 Decoupling Inputs

The S0 interface has two inputs for decoupling capacitors. For normal operation of the S0 interface capacitors have to be connected between Ref (220nF) / Cref (10nF, can be reduced up to 1 nF if necessary) and GND.

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3.5 Analogue Front End

The ISDN has an analogue front end (see
Figure 3-7 below) that connects directly to a handset, a hands-free microphone and a loudspeaker. The VBAFE includes D/A- and A/D conversion and filtering. To adapt to transducer tolerances the microphone preamplifier, the earpiece amplifier and the loudspeaker amplifier have programmable gain.

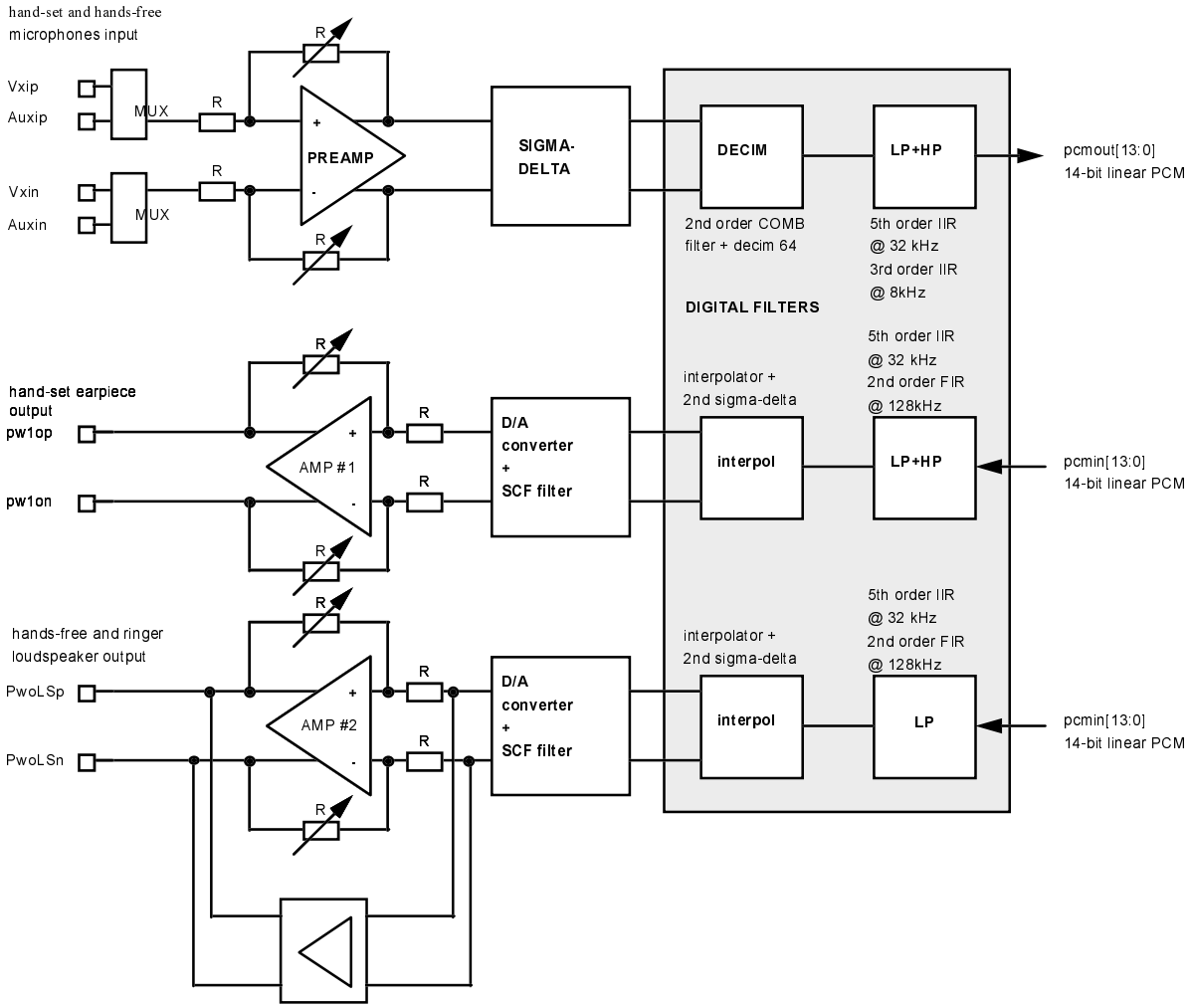

Figure 3-7: Analogue Front End

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3.5.1 Transmit Analogue Front End

The transmit path converts a signal from the analogue low level microphone input to 8 kHz digital samples according to ITU G.714/715. The microphone signal is amplified by a dedicated low-noise preamplifier whose gain is programmable. The frequency response may be adjusted at this point using appropriate external components.

Following the preamplifier is the encoder section, which uses a second-order oversampled converter operating at 2.048 MHz. The data coming out of the sigma-delta are digitally processed through a decimation filter for sampling rate reduction before subsequent low-pass and high-pass filtering.

The low noise microphone preamplifier is capable of directly interfacing with one of two microphones. The preamplifier gain is programmable in 64 steps.

3.5.2 Receive Analogue Front End

The G. 714/715 receive path decoder is basically the same in the opposite direction. The 8 kHz 14 bit linear data samples at the input are low-pass filtered and interpolated in two successive steps in order to limit the presence of high-frequency components outside the voice band. The data are further processed by a second-order digital modulator and are then converted into analogue signals which are filtered to further remove high frequencies before going into one of the two push-pull differential amplifiers. Most of the analogue circuitry uses differential design. This allows processing of signals with twice as much amplitude as in a single-ended design and virtually eliminates injected noise from supplies and substrate. The gain of the output amplifier is adjustable.
The side tone - calculated by the CPU - can be injected into the hand-set path if required.
There are two speaker interfaces; one to drive the earpiece transducer and one for the loudspeaker and / or ringer. The linear amplifier in the loudspeaker path can drive loads with a transconductance as low as 50 Ω. Instead of the linear amplifier a high current/voltage driver can be activated in the loudspeaker path to generate the ringing signal.

3.5.3 Reference Voltage

The reference voltage for the A/D and D/A conversion is generated internally, only an external decoupling capacitor has to be connected between Vrefn and Vrefp. The value required is 47 nF.

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3.5.4 Data flow of the B-channel audio samples

The audio samples that are received by the B-channel can be read from the S0_RxReg. To transfer the data to the VBAFEpcm1Reg / VBAFEpcm2Reg three actions have to be done in the fast interrupt handler:

- extract the B-channel from the S0_RxReg
- decompress the A-law or µ-law coded 8 bit data to linear 14 bit PCM values
- add side tone for user comfort (not for open listening / handsfree operation)

After this the 14 bit value can be written into the VBAFEpcmXReg.

In the other direction the 14 bit linear PCM data are read from the VBAFEpcm1Reg. There are also three actions that have to be done in the fast interrupt handler:

- generate value for side tone (not for open listening / handsfree operation)
- compress 14 bit linear to A-law or µ-law
- align data for writing to S0_TxReg

After this the 8 bit value can be written

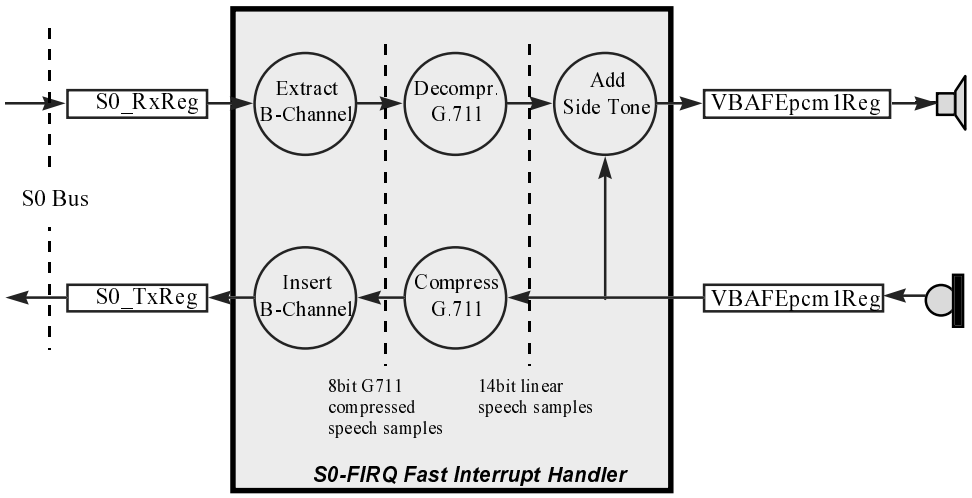

Figure 3-8 B-channel audio handling

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3.6 Analogue Digital Converter

The VIP includes two simple single slope general purpose analogue digital converters (refer to Fig. 10). These ADCs are built with a simple comparator, an internally generated reference and a bi-directional output port. The comparator output is connected to an internal interrupt input of the interrupt controller.
Under CPU control it is possible to measure voltages or resistor values. After the capacitor is charged by the port, the port changes to input and a program can measure the time between start and the occurrence of the comparator interrupt.
The interrupt is issued at the falling edge.

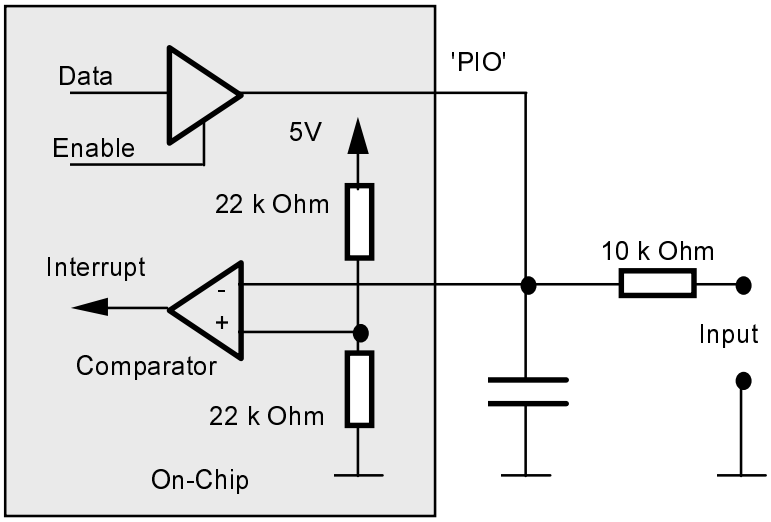

Figure 3-9: Analogue Digital Converter

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3.7 UART

The simple full-duplex serial interface with an interrupt driven 1 byte buffer for each direction. The start bit is active low and the LSB is transmitted first. The even or odd parity generation is done by software. The transmission formats that can be used are 8N1, 7N2, 7E1 or 7O1.
The maskable UART interrupt will be generated on UART transmit buffer empty or UART receive buffer full. UART transmission flags will be generated on UART transmit buffer busy, UART transmit buffer empty, UART receive buffer full or stop bit failure. The start bit can be read back. The a standard request to send signal (/RTS) is generated by the UART.
The baud rates are programmable in 8 steps from 1.2 kBaud to 230.4 kBaud. The baud rate clock depends on the clock used for the ARM core, either the 36,864 MHz or 460 kHz clock. Also a sleep mode (UART and baud rate clocks stopped) for power down is implemented.
The names of the UART signals correspond to the DTE definitions.

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3.8 Serial DSP/CODEC Interface (SDCI)

For communication with other serial devices like CODEC's, DSP's or peripherals, the VIP incorporates a full duplex serial port with a 64 bit serial - parallel converter to drive standard 8 bit telecom or 14 bit linear CODEC's. To achieve greater flexibility several functions of this port are software selectable, like frame sync on the rising or falling edge etc. (see Fig. 11).
The frequency of the clock can be set in eight steps between 512 kHz and 4096 kHz and the data rate respectively between 512 kbit/s and 2048 kbit/s.
The SDCI interface of the VIP can be used in master or in slave mode. In master mode the clocks for the interface are generated inside the VIP and control the other SDCI devices. In slave mode the SDCI interface of the VIP is clocked by an other device.

3.8.1 SDCI Master Mode

In the SDCI master mode the VIP will generate all clocks that are necessary to use the SDCI interface. Additionally two further FSCs can be generated.

In the master mode the VIP can access the first 64 bit of the SDCI frame via the sdci_lswReg and sdci_mswReg. Only at 2048 kHz bit shift clock 4* 64 bit can be accessed.

There are four dedicated pins to transfer data via this interface:

- BSCK --> Bit Clock output
- FSC1 --> Frame Sync1 output
- SDI --> Serial Data input
- SDO --> Serial Data output

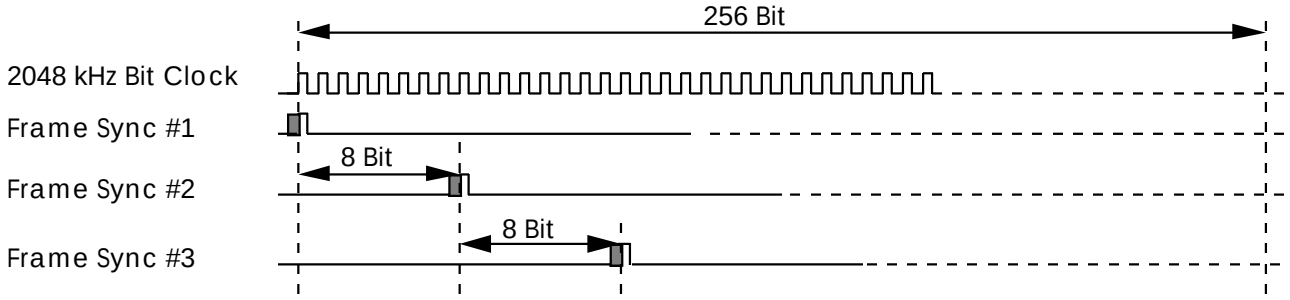

Figure 3-10: sample SDCI Interface Timing in Master Mode at 2048 kHz

Two other I/O pins may be programmed as additional frame sync signals in addition to the four pins mentioned above:

- FSC2 --> additional time slot output
- FSC3 --> additional time slot output.

FSC1 to FSC3 are used to assign one signal channel in order to directly connect up to three devices to the VIP.
In the master mode the timing source for the frame sync signals and for the bit shift clock can be selected out of three VIP internal and one VIP external timing references:

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- SO PLL FSC (8 kHz if S0 is locked, else 8 kHz +5400ppm)
- SO PLL bit clock (8 kHz if S0 is locked, else 8 kHz +5400ppm)
- external high power oscillator of the VIP
- external FSC signal

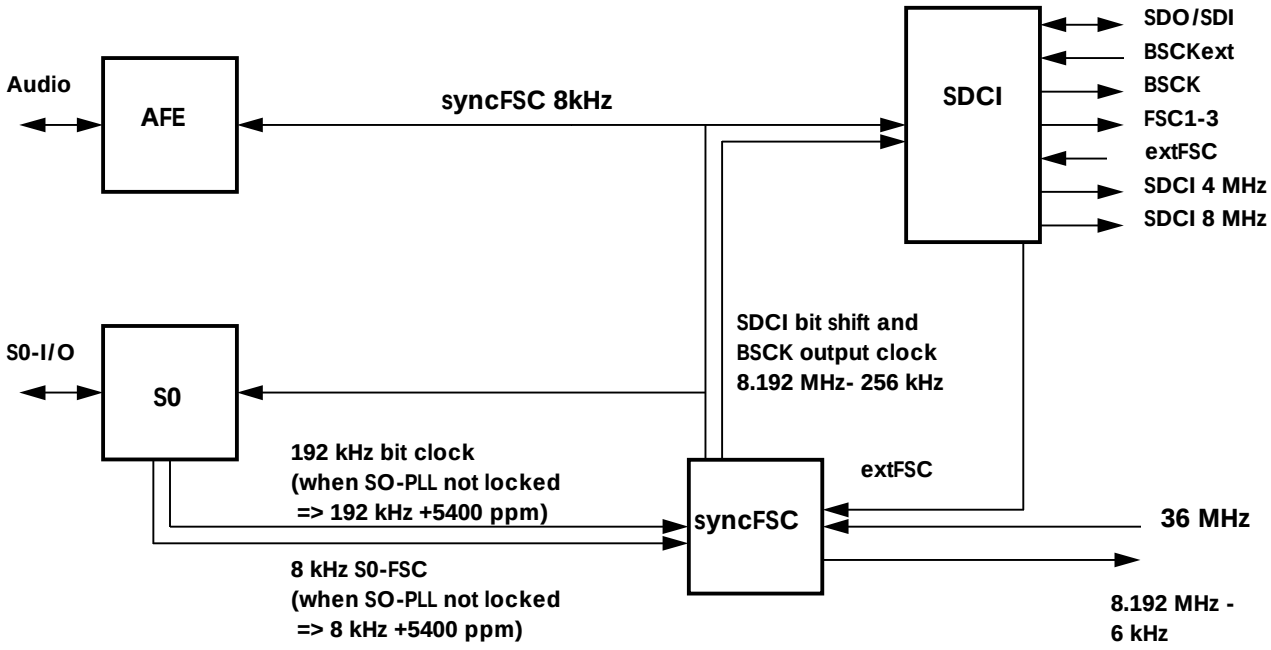

Figure 3-11: SDCI Timing Sources

In master mode the repetitionrate of the FSC1 to FSC3 is always 8 kHz. The distance between FSC1 - FSC2 - FSC3 is always 8 bit. Therefore the number of bytes of the SDCI frame varies with the selected bit rate e.g. Figure 3-11 shows a configuration with a clock of 2048 kHz and a bit rate of 2048 kbit/s. The 'fast IR phase1 of the FSC1' will be issued at the beginning of the frame. The other 'fast IR phaseX of the FSC1' are issued but can only be used when 2048 kHz bit shift clock is used.
If the VIP accesses only the first 64 bit, the SDCI output will be tristate for the remaining frame.

3.8.2 SDCI Slave Mode

In slave mode operation the repetition rate of the external frame sync signal FSC_EXT has to be 32 kHz. Each 32 kHz FSC_EXT frame sync signal generates a fast interrupt. There is no timing relation between the SDCI interface and the S0-interface in slave mode operation.
In the slave mode the SDCI interface is clocked externally. For this mode four pins are used to set up the SDCI interface:

• BSCK	--> Bit Clock	input
• FSC_EXT	--> Frame Sync1	input
• SDI	--> Serial Data	input
• SDO	--> Serial Data	output

FSC_EXT is an I/O pin that has to be programmed as frame sync input.

Each of the four 32 kHz sub-frames of the FSC1 generates a fast interrupt.

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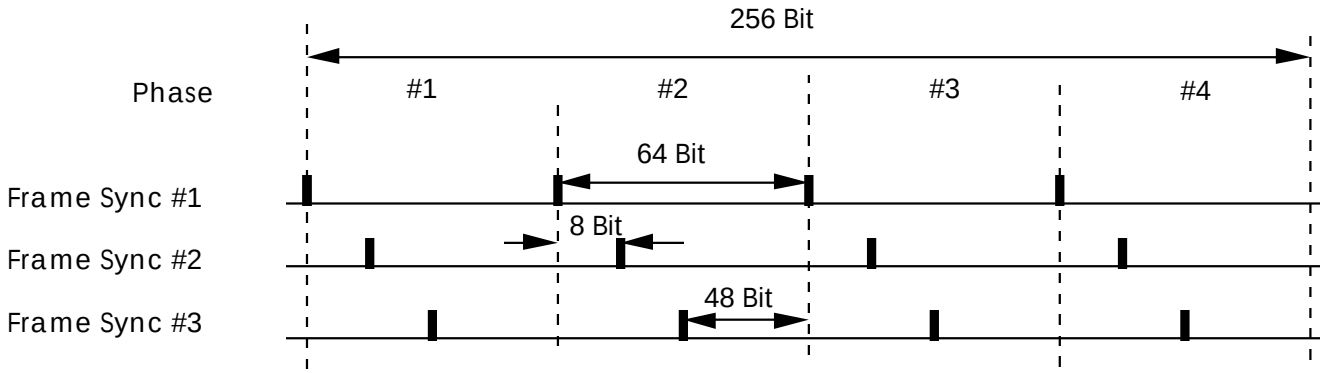

Figure 3-12: SDCI Interface Timing in Slave Mode

3.8.3 SDO Pin

The SDO pin is the serial output of the SDCI data. This pin is an output if the VIP writes data to the output, otherwise it is tristate.
To avoid a floating pin, a pull-up / pull-down resistor should be connected to SDO.

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3.9 Key Pad

The keypad interface consists of 6 inputs with internal pull-down resistors (acting as column lines) that generate an interrupt via an or-gate. The row lines are provided by ports. A key push can generate a maskable interrupt.

The interrupt is issued at the rising edge.

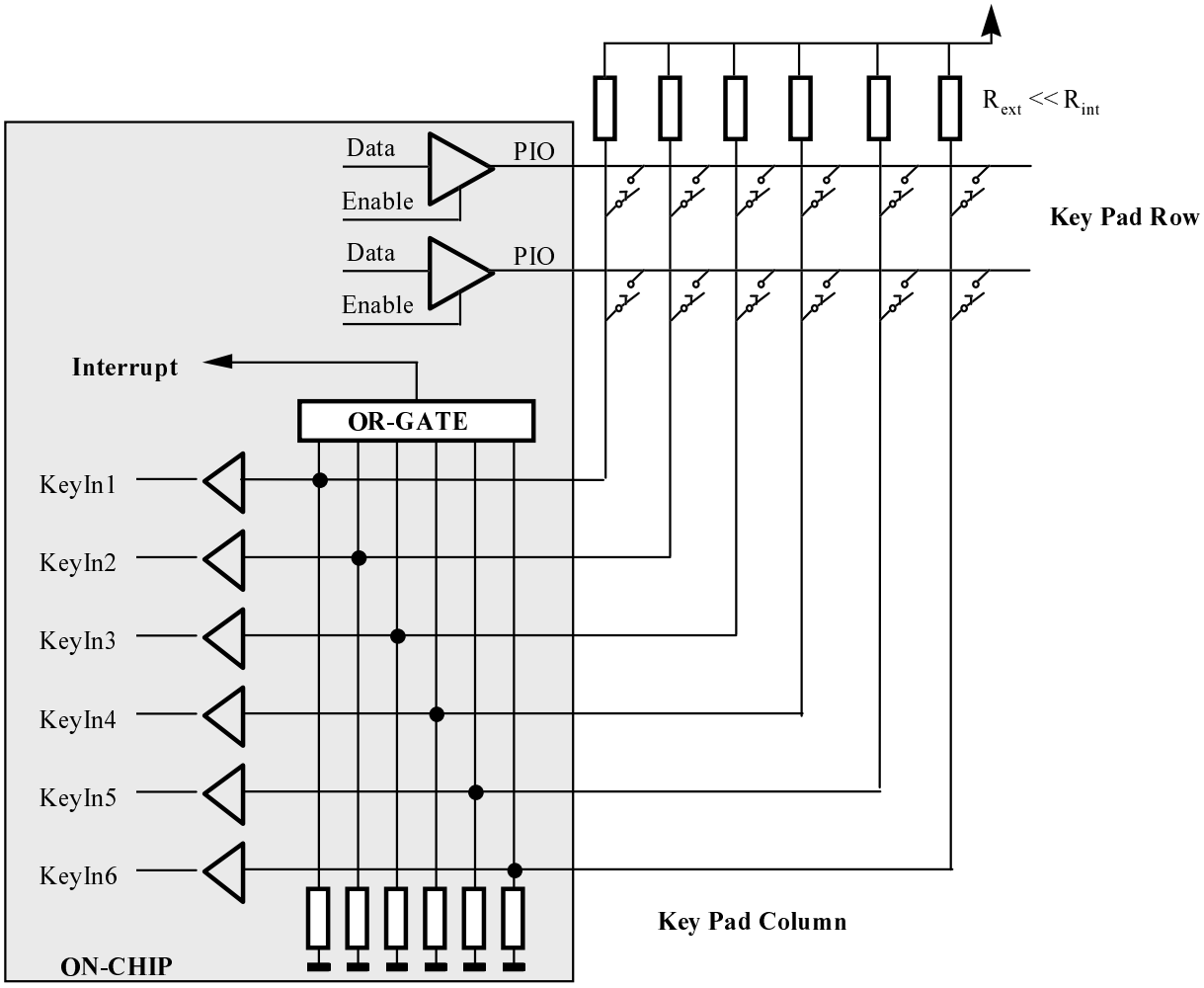

Figure 3-13: Keypad Interface

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3.10 I/O Ports

All ports are bi-directional (except PIO2[10]). The direction of each bit is programmable. All ports can be programmed to have special functions in the various configurations supported by the VIP.
Some functions are not available in the ARM 7 debug mode, because these pins are used to connect the embedded ICE.
Of the 33 I/O ports #1 (PIO1[22:0] and PIO2[9:0]) 3 can be configured to generate an interrupt; two generate a normal interrupt and one a fast interrupt.
Some of the PIO pins have pull-up resistors, some not (check 'Table 5-12: I/O Ports')

Pin #	Signal Name	Type	Function #1	Function #2
100	PIO2 [10]	Output	DAC-output for LCD contrast control; not programmable I/O	
99	PIO2 [9]	Bidirec	I/O port2[9]	SDCI-8 MHz Clock (output) S0-Monitor1 (input) TDO-P (output, ARM7 debug mode)
98	PIO2 [8]	Bidirec	I/O port2[8]	SDCI-4 MHz Clock (output) S0-Monitor0 (input) ECLK (output, ARM7 debug mode)
51	PIO2 [7]	Bidirec	I/O port2[7]	FSC3 (output); additional frame sync for the SDCI interface or
52	PIO2 [6]	Bidirec	I/O port2[6]	FSC2 (output); additional frame sync for the SDCI interface
53	PIO2 [5]	Bidirec	I/O port2[5]	CS16c (output), chip select for 16/32-bit static memory
54	PIO2 [4]	Bidirec	I/O port2[4]	CS16b (output), chip select for 16/32-bit static memory
55	PIO2 [3]	Bidirec	I/O port2[3]	CS16a (output), chip select for 16/32-bit static memory
56	PIO2 [2]	Bidirec	I/O port2[2]	CAS1, column address select #1
57	PIO2 [1]	Bidirec	I/O port2[1]	CAS0, column address select # 0
58	PIO2 [0]	Bidirec	I/O port2[0]	RAS, row address select for DRAM
61	PIO1[22]	Bidirec	I/O port1[22]	SDCI FSC (output); 8 kHz frame sync(syncFSC)
62	PIO1[21]	Bidirec	I/O port1[21]	ADR[22] (output); additional address line FSC_EXT (input); external frame sync for SDCI interface slave mode operation
63	PIO1[20]	Bidirec	I/O port1[20]	ADR[21] (output); additional address line
64	PIO1[19]	Bidirec	I/O port1[19]	UART signal (output); /Request to SEND; frame sync of the S0-DPLL (S0_FSC)
65	PIO1[18]	Bidirec	I/O port1[18]	Data[31] (bidirec); additional data line
66	PIO1[17]	Bidirec	I/O port1[17]	Data[30] (bidirec); additional data line
67	PIO1[16]	Bidirec	I/O port1[16]	Data[29] (bidirec); additional data line
70	PIO1[15]	Bidirec	I/O port1[15]	Data[28] (bidirec); additional data line
71	PIO1[14]	Bidirec	I/O port1[14]	Data[27] (bidirec); additional data line
72	PIO1[13]	Bidirec	I/O port1[13]	Data[26] (bidirec); additional data line
73	PIO1[12]	Bidirec	I/O port1[12]	Data[25] (bidirec); additional data line
74	PIO1[11]	Bidirec	I/O port1[11]	Data[24] (bidirec); additional data line
75	PIO1[10]	Bidirec	I/O port1[10]	Data[23] (bidirec); additional data line
76	PIO1[9]	Bidirec	I/O port1[9]	Data[22] (bidirec); additional data line
77	PIO1[8]	Bidirec	I/O port1[8]	Data[21] (bidirec); additional data line
80	PIO1[7]	Bidirec	I/O port1[7]	Data[20] (bidirec); additional data line
81	PIO1[6]	Bidirec	I/O port1[6]	Data[19] (bidirec); additional data line
82	PIO1[5]	Bidirec	I/O port1[5]	Data[18] (bidirec); additional data line
83	PIO1[4]	Bidirec	I/O port1[4]	Data[17] (bidirec); additional data line
84	PIO1[3]	Bidirec	I/O port1[3]	Data[16] (bidirec); additional data line
85	PIO1[2]	Bidirec	I/O port1[2]	Input with normal interrupt generation
86	PIO1[1]	Bidirec	I/O port1[1]	Input with normal interrupt generation
87	PIO1[0]	Bidirec	I/O port1[0]	Input with fast interrupt generation
105	KEYin[4]	Input	Keypad column[4]	/TRST (input) ARM7 debug mode
106	KEYin[3]	Input	Keypad column[3]	TMS (input) ARM7 debug mode
107	KEYin[2]	Input	Keypad column[2]	TCK (input) ARM7 debug mode
108	KEYin[1]	Input	Keypad column[1]	TDI (input) ARM7 debug mode

Table 3-3: Multifunctional PIN's

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3.11 Clock Oscillators and Watchdog

The VIP includes two oscillators. The 36.864 MHz oscillator based on a third overtone quartz is used in normal operation. The required quartz accuracy is 30 ppm.

Internally the ARM7 can driven directly via the 36.8 MHz frequency or by 1/3 of that frequency (12.288 MHz) to support emergency mode applications. The switch over is controlled by the VBAFEReg[30].

An alternate oscillator with 460 kHz is for power down operation of the whole device. Switch-over between the oscillators is performed by software.

A programmable prescaler scales the CPU clock down to the main operating frequency of all serial interfaces. The crystal frequency is always the CPU clock. Clocks of individual blocks can be stopped for power saving.

A watchdog timer produces a reset signal after 1.28 / 2.56 if no watchdog service has occurred. The watchdog can be stopped e.g. during the initialisation process. The control register of the watchdog and the clock management are protected against faulty writes. Which time-out the watchdog uses is controlled in the sysClockReg. The watchdog can be reset by writing the wdogReg with a special pattern.
A 2.5 ms timer for multitasking and DRAM refresh is available. It repeats automatically and has an individually maskable interrupt. The value of 2.5 ms is calculated for the use with the 36.864 MHz oscillator. The timebase for this timer depends on the clock used for the ARM core.

3.12 LCD-Contrast Control

The VIP includes circuitries to control the contrast of an LCD. An eight-bit digital to analogue converter in combination with a output driver stage generates the required contrast signal for a generic LCD display (see also Figure 3-14).
For normal operation a load-resistor to GND is required. A short between this pin and GND can damage the circuitry in the chip.

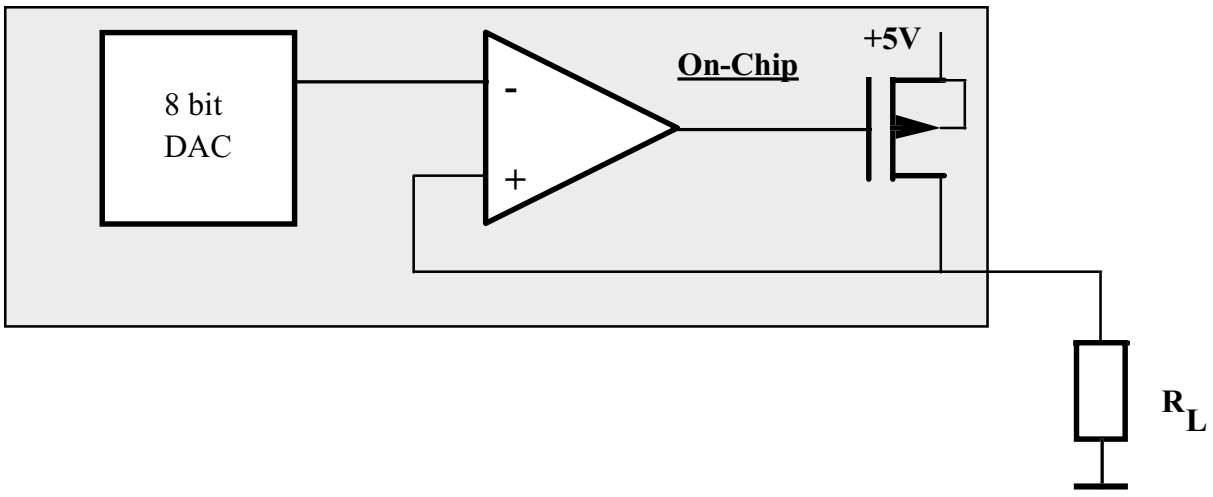

Figure 3-14: LCD-Contrast Control

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3.13 Hardware Configuration

The hardware configuration of the VIP is done by the five ConfigTest pins.

ConfTest pin[5:1]	Boot source	Upper Memory area	SDCI mode	ARM7 debug
00000	CS8boot	16 bit	master	disabled
00001	CS16boot	16 bit	master	disabled
00010	internal	16 bit	master	disabled
00011	CS8boot	16 bit	slave	disabled
00100	CS16boot	16 bit	slave	disabled
00101	internal	16 bit	slave	disabled
00110	CS8boot	32 bit	master	disabled
00111	CS16boot	32 bit	master	disabled
01000	internal	32 bit	master	disabled
01001	CS8boot	32 bit	slave	disabled
01010	CS16boot	32 bit	slave	disabled
01011	internal	32 bit	slave	disabled
01100	CS8boot	16 bit	master	enabled
01101	CS16boot	16 bit	master	enabled
01110	CS16boot	16 bit	slave	enabled
01111	CS16boot	32 bit	master	enabled
10000	all Pad's Tristate			
1xxxxx	Test Mode active			

Table 3-4 ConfTest pins

The boot source determines the memory location from which the first word will be fetched. After this fetch the memory location is as described in chapter 'Memory Interface'.
To receive a working program that runs from an external memory the first instruction in this memory has to be a branch to the start of the initialisation routine. This branch has to be 'hard coded' e.g. DCD 0xEA3FFFFF which equals B 0x01000004. This is a jump to the second word of the CS16boot area.
After reset the PC is set to '0x0' and the jump has to be coded accordingly.

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4. REGISTER DESCRIPTION

4.1 Register Map

# (0.x)	Name	I/O Address (hex)	Function	Page
1	mcrReg	0x1000	Memory control register	36
-	-	0x1004	not used	
-	-	0x1008	not used	
2	wdogReg	0x100C	Watchdog retrigger register	37
3	ticReg	0x1010	Timer interrupt control register	38
4	fiarReg	0x1014	Fast interrupt acknowledge register	39
5	niarReg	0x1018	Normal interrupt acknowledge register	40
6	xinocReg	0x101C	XIN oscillator control register	41
7	configS0_Reg	0x1024	S0 DPLL configuration / status register	42
8	intS0_Reg	0x1028	S0 DPLL interrupt register	49
9	resetS0_Reg	0x102C	S0 DPLL reset register	51
10	UART_Reg	0x1030	UART Rx / TxData register	52
11	UART_statReg	0x1034	UART status register	52
12	D_RxReg	0x1038	D-channel RxData register	53
13	D_TxReg	0x103C	D-channel TxData register	53
14	S0_RxReg	0x1040	S0 RxData register	54
15	S0_TxReg	0x1044	S0 TxData register	55
16	idcReg	0x1048	ISDN control register	56
17	sdci_lswReg	0x104C	Serial DSP / CODEC LSWord Rx / TxData reg.	57
18	sdci_mswReg	0x1050	Serial DSP / CODEC MSWord Rx / TxData reg.	57
19	sdci_cntrReg	0x1054	Serial DSP / CODEC control register	58
20	VBAFEpcm1Reg	0x1058	VBAFE PCM Rx / TxData register #1	59
21	VBAFEReg	0x105C	VBAFE control register	60
22	pio1_statReg	0x1060	PIO status register #1	61
23	pio1_set0Reg	0x1064	PIO data set to zero for register #1	62
24	pio2_statReg	0x1068	PIO status register #2	63
25	pio2_set0Reg	0x106C	PIO data set to zero for register #2	64
26	keypadReg	0x1070	Keypad data register	64
27	pio1_set1Reg	0x1074	PIO data set to one for register #1	62
28	pio2_set1Reg	0x1078	PIO data set to one for register #2	64
29	sysClockReg	0x107C	Clock and baud rate control register	65
30	DAC_Reg	0x1080	LCD contrast control register	67
31	VBAFEpcm2Reg	0x1084	VBAFE PCM RxData register #2	67

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4.2 Register Description

4.2.1 Memory Control Register (mcrReg)

This register programs the four independent wait states areas and the DRAM timing and type selection.

IDB[ ]	Code	Function	Reset Value
31:22	-	Not used	0000 0000 00
21		/CS16c control	0
	0	active low	
	1	active high	
20		/CS16b control	0
	0	active low	
	1	active high	
19		/CS16a control	0
	0	active low	
	1	active high	
18		Fast page mode	0
	0	ON	
	1	OFF	
17:16		DRAM type	01
	00	256 kbit	
	01	1 Mbit	
	1x	4 Mbit	
15:14		Wait state programming DRAM *)	10
15		RAS precharge pulse short/long	
	0	rp time short (2 oscillator clocks, 54.2 ns)	
	1	rp time long (3 oscillator clocks, 81.3 ns)	
14		Sequential wait states, /CAS low time during seq. access	
	0	1 wait state (access-time 54.2 ns, CAS low time 27.1 ns)	
	1	2 wait states (access-time 81.3 ns, CAS low time 54.2 ns)	

*) IDB[15:12] = x100 is not allowed.

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IDB[ ]	Code	Function continue	Reset Value
13:12		Non sequential wait states, /CAS low time during non seq. access	10
	00	3 wait states if rp short (access time 108.5 ns, /CAS low time 27.1 ns) 4 wait states if rp long (access time 135.6 ns, /CAS low time 27.1 ns)	
	01	4 wait states if rp short (access time 135.6 ns, /CAS low time 54.2 ns) 5 wait States if rp long (access time 162.7 ns, /CAS low time 54.2 ns)	
	10	5 wait states if rp short (access time 162.7 ns, /CAS low time 81.3 ns) 6 wait states if rp long (access time 189.8 ns, /CAS low time 81.3 ns)	
	11	6 wait states if rp short (access time 189.8 ns, /CAS low time 108.5 ns) 7 wait states if rp long (access time 217 ns, /CAS low time 108.5 ns)	
		Wait state programming static memory	
11:8		/CS16c	1010
7:4		/CS16boot, /CS16a, /CS16b	1010
3:0		/CS8boot, /CS8	1010
	0000	1 wait state	
	0001	1 wait state	
	0010	2 wait states	
	0011	3 wait states	
	0100	4 wait states	
	0101	5 wait states	
	0110	6 wait states	
	0111	7 wait states	
	1000	8 wait states	
	1001	9 wait states	
	1010	10 wait states	
	1011	17 wait states	
	1100	24 wait states	
	1101	31 wait states	
	1110	38 wait states	
	1111	45 wait states	

4.2.2 Watchdog Retrigger Register (wdogReg)

This is a write only register. Writing this register with the special pattern will reset the watchdog.

IDB[ ]	Code	Function	Reset Value
31:0	0x87654321	reset the watchdog	
	else	no function	

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4.2.3 Timer and Interrupt Control Register (ticReg)

Via this register the interrupt mask bits can be set respectively be reset and the timer and watchdog can be controlled. Also the configuration pins of the VIP are readable by this register.
Register is read & write.

IDB[ ]	Code	Function	Reset Value
31	-	For test only; set to one for normal operation	1
30		Normal IR mask S0 DPLL	1
29		Normal IR mask UART	1
28		Normal IR mask PIO1[2]	1
27		Normal IR mask PIO1[1]	1
26		Normal IR mask Keypad	1
25		Normal IR mask ADC2	1
24		Normal IR mask ADC1	1
23		Normal IR mask 2.5 ms timer	1
22		Normal IR mask D-Channel TxAbort	1
21		Normal IR mask D-Channel TxEmpt	1
20		Normal IR mask D-Channel TxCompl	1
19		Normal IR mask D-Channel RxFull	1
18		Normal IR mask D-Channel RxAbort	1
17		Normal IR mask D-Channel RxSFD (stop flag detected)	1
	1	IR masked	
	0	IR not masked, IR source enabled	
16		Normal IR level/edged triggered programming for PIO1[2]	0
15		Normal IR level/edged triggered programming for PIO1[1]	0
	1	level triggered	
	0	edge triggered	
14		Fast IR mask UART, level triggered	1
13		Fast IR mask for PIO1[0]	1
12		Fast IR mask phase4 of the syncFSC	1
11		Fast IR mask phase3 of the syncFSC	1
10		Fast IR mask phase2 of the syncFSC	1
9		Fast IR mask phase1 of the syncFSC	1
8		Fast IR mask S0 PLL frame sync	1
	1	IR masked	
	0	IR not masked, IR source enabled	
7		Fast IR level/edged triggered programming for PIO1[0]	0
	1	level triggered	
	0	edge triggered	
6		Enable timer & watchdog ***)**	0
	1	Clock for timer & watchdog disabled ****)** (Power down mode)	
	0	Clock for timer & watchdog enabled	
5		Watchdog enable ***) ***)**	1
	1	Watchdog enabled	
	0	Watchdog disabled & reset	
4:0	-	ConfTest[5:1] bit value (VIP chip HW configuration) **read only**	-

***)** These bits are protected against falsely writing.
To set these bits :
1. write 15 (hex) to niarReg
2. set bits as appropriated

The watchdog time is controlled in the sysClockReg

****)** Stops all clocks beside the CPU clock for power down operation.

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***) The time of the watchdog depends on the sysClockReg, bit [19] and on the speed of the ARM core (xinocReg).

4.2.4 Fast Interrupt Acknowledge Register (fiarReg)

The fast interrupt sources are stored in this register. By reading this register the fast interrupt will be acknowledged and the register will be cleared. The Register is read only.

IDB[ ]	CODE	Function	Reset Value
31:7		not defined	undefined
6		Fast IR UART, level triggered	0
5		Fast IR PIO1[0]	0
4		Fast IR phase4 of the FSC1 *)	0
3		Fast IR phase3 of the FSC1 *)	0
2		Fast IR phase2 of the FSC1 *)	0
1		Fast IR phase1 of the FSC1 *)	0
0		Fast IR S0 frame sync	0
	0	no interrupt occurred	
	1	interrupt occurred	

*) Each of the four phases of the SDCI FSC1 signal generates an interrupt.

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4.2.5 Normal Interrupt Acknowledge Register (niarReg)

The normal interrupt sources are stored in this register. The S0 DPLL interrupt source is further decoded by the intS0_Reg. By reading the niarReg the normal interrupt will be acknowledged and the register will be cleared. The register is read only.

IDB[ ]	CODE	Function	Reset Value
31:14		not defined	undefined
13		Normal IR S0 DPLL	0
12		Normal IR UART	0
11		Normal IR PIO1[2]	0
10		Normal IR PIO1[1]	0
9		Normal IR Keypad	0
8		Normal IR ADC2	0
7		Normal IR ADC1	0
6		Normal IR 2.5 ms timer *)	0
5		Normal IR D-Channel TxAbort ***)	0
4		Normal IR D-Channel TxEmpt ***)	0
3		Normal IR D-Channel TxCompl ***)	0
2		Normal IR D-Channel RxFull ***)	0
1		Normal IR D-Channel RxAbort ***)	0
0		Normal IR D-Channel RxSFD (stop flag detected) **) ***)	0
	0	no interrupt occurred	
	1	interrupt occurred	

*) the timer is based on the operation frequency of the ARM core. 2.5 ms is the value for 36.864 MHz operation. For the low power oscillator the time is:
2.5 ms * (36.864 MHz / low power frequency)

**) The position of the frame stop flag in the receive buffer is stored in the idcReg [12:7].

***) these interrupts might occur simultaneously

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4.2.6 XIN Oscillator Switch Control Register (xinocReg)

The XIN oscillator control register is read / write. There are two oscillators in the VIP chip, one is working with the normal operation clock of 36.864 MHz and another low power oscillator with a frequency of 460.8 kHz.

IDB[31:0]	Function (Write Only)	Clock Frequency	Reset Value
00 (hex)	Switch back from the low power oscillator to the 36.864 MHz oscillator. *)	36.864 MHz	00
01 (hex)	Switch over from 36.864 MHz oscillator to the low power oscillator LPxin	460.8 kHz	
03 (hex)	Switch off the 36.864 MHz oscillator; power down mode;	460.8 kHz	
05(hex)	Switch on the 36.864 MHz oscillator power up mode *)	460.8 kHz	

*) A delay of about 3.5 msec is necessary between the commands 'switch on' (05) and 'switch back' (00). Also some delay might be required between 'switch over' (01) and 'switch off' (03)

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4.2.7 S0 DPLL Config. Reg. (configS0_Reg)

The configuration of the S0 DPLL will be done by writing to this register. Reading this register provides information about the actual status of the DPLL.

4.2.7.1 S0 DPLL Config. Reg. (configS0_Reg) write

IDB[ ]	Code	Function	Reset Value
31:28		Phase offset **1)**	0110
	0000	+ 440 ns (Tx Phase delayed)	
	0110	0 ns	
	1111	- 760 ns (Tx Phase advanced)	
27:26		Transmitter slewrate **2)**	01
	00 -> 11	slow -> fast	
25		Filtertype **3)**	0
	0	average	
	1	increment	
24		S0 transmitter control **4)**	0
	0	automatically	
	1	CPU	
23		S0-Tx-framer reset	0
22		S0-Rx-framer reset	0
	1	reset, cleared after reset is executed	
	0	normal operation	
21		Multiframe delayed by one frame	0
	0	off (standard)	
	1	on	
20		Info1 **4)**	0
	0	disabled	
	1	enabled	
19		96 kHz Testsignal **4)**	0
	0	disabled	
	1	enabled	
18		4 kHz Testsignal **4)**	0
	0	disabled	
	1	enabled	
17		Info3 **4)**	0
	0	disabled	
	1	enabled	
16		Multiframe Data source	0
	0	MF bits set by the receiver	
	1	MF bits set by the CPU	
15:14		Receiver zero crossing comparator level **5)**	10
	00	Hysteresis threshold: ± 6.7%	
	01	Hysteresis threshold: ± 10.6%	
	10	Hysteresis threshold: ± 16.8%	
	11	Hysteresis threshold: ± 26.7%	
13:12		Receiver data comparator level **5)**	10
	00	Input data threshold: ± 33%	
	01	Input data threshold: ± 48%	
	10	Input data threshold: ± 69%	
	11	Input data threshold: ± 100%	
11:8		Input filter threshold **3)**	0111
	0000	no filter function	
	0001	1 samples = 0.32 us bit width	
	0111	7 samples = 2.28 us bit width	
	1111	15 samples = 4.88 us bit width	
7:4		Regain counter limit (ML) **6)**	0000
3:0		Lost frame counter limit (NL) **7)**	0000

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1) Phase Offset The nominal offset between the received frame and the transmitted frame is 2 bit. To compensate for external delays in the transmit path - which may arise due to the ESD structure or the transformer - the offset of the transmitted signal relative to the received signal can be programmed. The phase offset gives the offset of the transmitted frame relative to the 2 bit nominal offset. It is programmable between + 440 ns (Tx delayed; IDB[31:28]=0000) to -760 ns (Tx advanced; IDB[31:28]=1111) in 16 steps 80 ns each.

2) Slew Rate The slew rate of the open drain output transistor of the S0 transmitter can be programmed in four steps to adjust the S0 output to the characteristic of the transformer under use. IDB[27:26]=00 will set the output to the lowest slewrate and IDB[27:26]=11 respectively to the highest achievable slewrate.

3) Input Filter The received bit streams at LIP and LIN get oversampled with a 3.072 MHz clock and rated by two identically filters each separately. The filter characteristic can be set by IDB[25] to incremental or average. With the filter characteristic set to incremental, a mark is detected whenever the number of mark-samples equals the threshold set in IDB[11:8]. With the filter characteristic set to average, a mark is detected when ever the number of mark-samples minus the number of the space-samples equals the threshold set in IDB[11:8].

4) Transmitter Control The control of the transmitter can be done automatically or by the CPU (see table below). In the reset state under automatic control, Info1 is transmitted on detection of Info0 (see also Fig. 15). On detection of any signal (InfoX) the controller stops transmitting Info1, and after synchronisation and M=ML (for explanation of M and ML see below) in sync frames it starts to transmit Info3. On the other hand after N=NL (for explanation of N and NL see below) not in sync frames and detection of Info0 it switched back to transmit Info1. Furthermore for test purpose various signal can be transmitted.

Function	IDB [24]	IDB [20]	IDB [19]	IDB [18]	IDB [17]	Reset Value
Transmitter (controlled by N, M-counter)	0	x	x	x	x	00000
Transmitter controlled by CPU	1	x	x	x	x	
Info3 disabled	x	x	x	x	0	
Info3 enabled (controlled by N, M-counter)	0	x	x	x	1	
Info3 active (controlled by CPU)	1	x	x	x	1	
Info1 disabled	x	0	x	x	x	
Info1 enabled (controlled by InfoX)	0	1	x	x	x	
Info1 active (controlled by CPU)	1	1	x	x	x	
Testsignal 4 kHz	1	x	0	1	x	
Testsignal 96 kHz	1	x	1	0	x	
do not use !	1	x	1	1	x	

Table 4-1: S0 Transmitter Control

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5) Input Threshold / input hysteresis

Basically the S0 receiver consists of a low resistance current input stage followed by a zero crossing and a data detection comparator. The threshold of the zero crossing detection and the data detection are relative to the input current and are set by the external serial input resistor. To achieve the 100% input threshold a input current of 10 µA is required. With a 1:2 input transformer the 100% threshold should be 1 V therefore a total differential input resistance of 100 kΩ is required respectively two serial input resistors of 50 kΩ each.

6) Regain Counter (M)

The regain counter count the 'in sync frames' after the S0 DPLL lost sync. If the control is set to automatic (IDB[24]=1) the transmitter get restarted automatically as soon as the regain counter (M) equals the regain counter limit (ML) specified in IDB[7:4] (see also Fig. 15).

Reset of M on: Power on reset
DPLL reset register bit [3]
Detecting of the first not in sync frame

7) Lost Frame Counter (N)

The lost frame counter (N) count the 'not in sync frames' after the S0 DPLL is in sync. If the control is set to automatic (IDB[24]=1) the transmitter get automatically stopped as soon as the lost frame counter (N) equals the lost frame counter limit (NL) specified in IDB[3:0]. The lost frame counter get reset by setting the lost frame counter limit to zero (NL=0) or on detecting of the first in sync frame (see also Figure 4-15).

Reset of N on: Power on reset
DPLL reset register bit [2]
Detecting of in sync frame before reaching the regain counter limit

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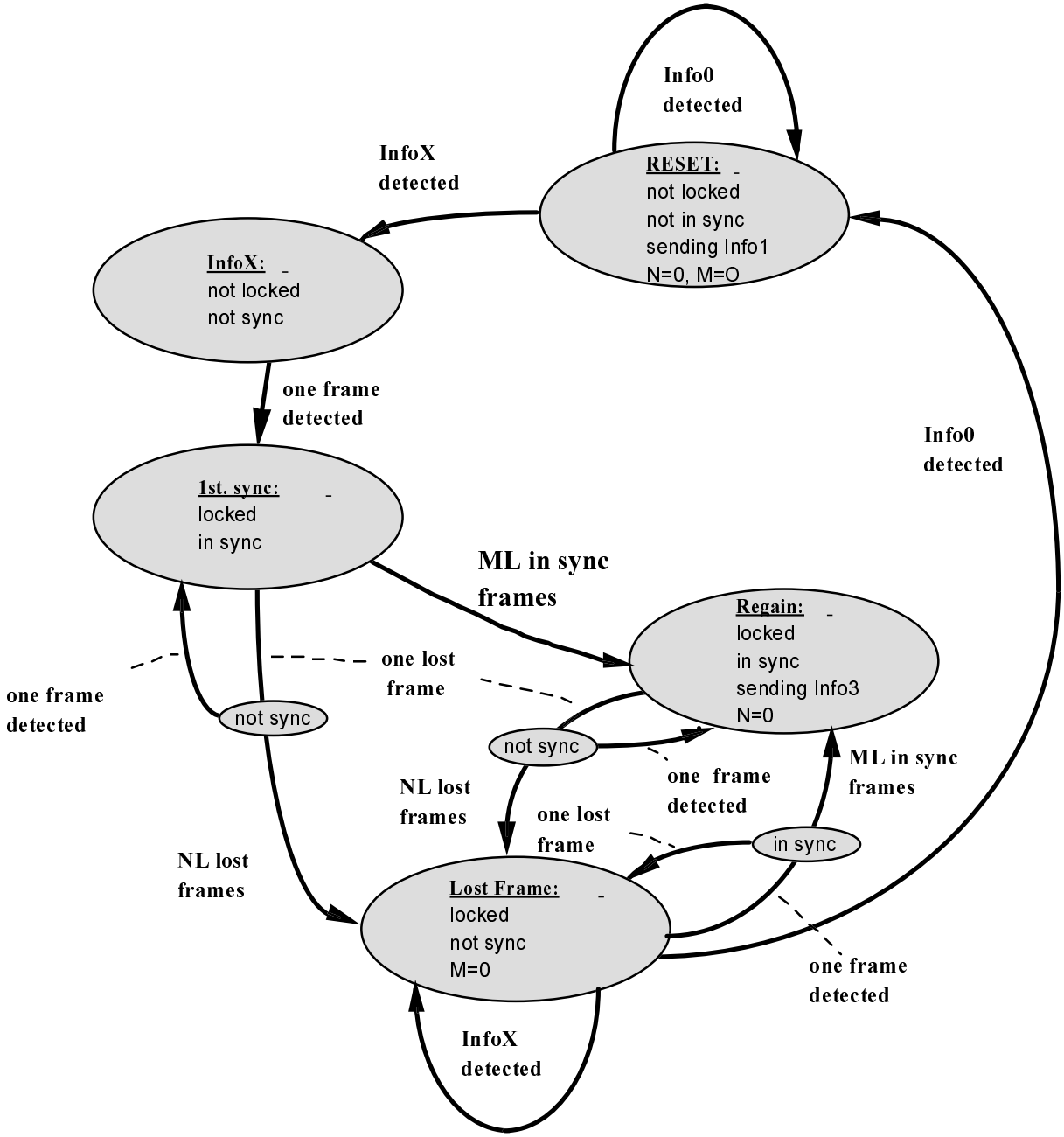

Figure 4-15 : State Diagram of the S0 DPLL (under automatic control)

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In the lost frame state on receiving Info0 the DPLL gets reset automatically. Under automatic control the DPLL can leave the lost frame state only on detecting Info0 or on regaining . As long as the DPLL detects InfoX in the lost frame state it will keep the lost frame state. To resolve this dead lock loop, which can occur due to the jump of the frame position, the DPLL has to be reset by the CPU (configS0_Reg[23:22]).

The DPLL reset will set:	Lock status:	unlocked
	Frame status:	lost frame
	sync status:	not in sync
	Regain counter M:	0
	Lost frame counter:	0
	Echo bit counter:	0

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4.2.7.2 S0 DPLL Config. Reg. (configS0_Reg) read

IDB[ ]	Function				
	Code	**IDB[31] = 0 in intS0_Reg**	**Code**	**IDB[31] = 1 in intS0_Reg**	**1)**
31	MSB	Input filter counter LIP	0		
30			0		
29			MSB	Actual received bit position	**2)**
28	LSB	Input filter counter LIP			
27	MSB	Input filter counter LIN			
26					
25					
24	LSB	Input filter counter LIN	LSB	Actual received bit position	
23:20	MSB:LSB	Echo bit counter			**3)**
19:16	MSB:LSB	Regain counter (M; good frames)			
15:12	MSB:LSB	Lost frame counter (N; bad frames)			
11	-	D-channel collision reset status			**4)**
10	-	Input data serial			
9	-	Last sent D-channel bit			
8	-	Last received Echo Bit			
7		Transmitter active			**5)**
	0	no			
	1	yes			
6		Transmitter enabled			**6)**
	0	no			
	1	yes			
5		Info2 detected			
	0	no			
	1	yes			
4		Info detected			
	0	Info 0 detected			
	1	Info x detected			
3		Lost frames detected			
	0	no			
	1	yes			
2		DPLL locked			**7)**
	0	no			
	1	yes			
1		DPLL sync			**8)**
	0	no			
	1	yes			
0		D-channel collision			
	0	no			
	1	yes			

1) IDB[31:24] The function of IDB[31:24] depends on whether intS0_Reg[31] has been set to one or not.

2) Received bit position This number gives the actual bit position in the receiving frame. Zero indicates the framing bit F.

3) Echo Bit Counter The Echo bit counter counts the number of logical '1' in the echo bit channel. A logical '0' or a D-channel collision resets the counter.

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4) Reset Status Reset of the D-channel collision can only be done at four position of the D-Channel bits in the S0-frame. As long as the reset was requested but not carried out this bit will be one. See also the resetS0_Reg.

5) Transmitter active Indication whether the transmitter actual is transmitting or not.

6) Transmitter enabled Status of the transmitter controlled by the regain / lost frame mechanisms.

7) Locked On detection of the first 'in sync frame' the DPLL reach the 'in locked' status. On detection of Info0 in the lost frame state the DPLL leaves the locked status. In the locked status the DPLL is able to compensate phase offset of ± 80 ns / frame.

8) Sync On detection of the first in sync frame the DPLL set in sync. On detection of the first lost frame the DPLL indicates not in sync.

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4.2.8 S0 Interrupt Register (intS0_Reg)

4.2.8.1 S0 Interrupt Register (intS0_Reg) Read

The S0 DPLL interrupt in the niarReg is further decoded by the intS0_Reg. The S0 interrupts are delta interrupts, only on a status changes a interrupt get generated. Each of the listed sources generate an interrupt if they are enabled. Disabled interrupts still can be read. After reading only the interrupts get cleared which were set at the beginning of the read process. Interrupts which occur during the read process will generate a new interrupt after the read has been finished.

Interrupts which from the functional point of view are mutual exclusive - e.g. 'Info2 detected' and 'Info2 not detected' - can both be active at the same time because they only get cleared on reading.

IDB[ ]	read Function
31-18	not defined
17	1 = Regain counter changed
16	1 = Lost frame counter changed
15	1 = D-channel collision (reset receipt)
14	1 = no D-channel collision
13	1 = DPLL is locked (search not possible)
12	1 = DPLL is not locked (search is enabled)
11	1 = Info2 detected
10	1 = no Info2 detected
9	1 = Transmitter enabled (by automatic)
8	1 = Transmitter disabled (by automatic)
7	1 = DPLL in sync
6	1 = DPLL not in synch
5	1 = receiving bit change from zero to one
4	1 = receiving bit change from one to zero
3	1 = Lost Frame counter N reach limit NL
2	1 = Regain counter M reach limit ML
1	1 = InfoX detected
0	1 = Info0 detected

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4.2.8.2 S0 Interrupt Register (intS0_Reg) Write

This register masks the S0 interrupts. Some of the interrupts source will be masked together, as indicated.

IDB [ ]	write Function		Reset Value
31		set of configS0_Reg[31:24] function:	0
	0	read filter count	
	1	read frame bit count	
30:26		not used	111 11
25		Testmode: stimulus DPLL locked	1
24		Testmode: stimulus Info2	1
23		Testmode: stimulus TX enable	1
22		Testmode: stimulus DPLL in sync	1
21		Testmode: stimulus collision	1
20		Testmode: stimulus zero crossing	1
19		Testmode: stimulus lost frame	1
18		Testmode: stimulus InfoX	1
17		Testmode: stimulus regain counter	1
16		Testmode: stimulus lost frame counter	1
	0	Interrupt enabled	
	1	Interrupt disabled	
15		Interrupt Testmode	0
	0	Normal operation	
	1	enable Interrupt Testmode	
14		for test only, must be set to '0'	0
13:12		S0 receiver modes	00
	00	receiver power down	
	01	receiver stand by *)	
	10	do not use	
	11	receiver active	
11:10		do not use, set to '00' for normal operation	11
9		Regain counter changes	1
8		Lost frame counter changes	1
7		D-channel collision and no D-channel collision	1
6		DPLL locked and DPLL not locked	1
5		Info2 detected / not detected	1
4		Transmitter enabled and disabled	1
3		DPLL in synch and DPLL not in synch	1
2		Zero crossing of the receive signal (wake up)	1
1		Lost frame limit and regain limit reached	1
0		InfoX and Info0 detected / not detected	1
	0	Interrupt enabled	
	1	Interrupt disabled	

*) only the zero crossing detector is active

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4.2.9 S0 DPLL Reset Register (resetS0_Reg) Write

Reset of the DPLL and the corresponding function will be done via this register

IDB[ ]	Function		Reset Value
31-5	not used, set to '0'		0
4	1 = Reset echobit counter	1)	0
3	1 = Reset regain counter (M)		0
2	1 = Reset lost frame counter (N)		0
1	1 = disable DPLL clock variation (fixed division factor 1/64); for test purpose only	2)	0
0	1 = Reset D-channel collision	3)	0

1) Beside the power on reset the echo counter gets reset on D-channel collision, on receiving an echo bit with logical value zero or by setting resetS0_Reg[4]=1.

2) This bit will not be cleared automatically

3) A collision at the D-channel will stop the transmission of the D-channel bits. After detection of a D-channel collision the 'Reset D-channel collision' bit has to be set. This will be executed during the transmission of the next D-bit. That the D-channel controller was reset, is indicated in the configS0_Reg (read) bit [11].

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4.2.10 UART RxTxData Register (UART_Reg)

This register contains the UART data and the start/stop & parity bits in the format 8N1, 7P(arity)1 or 7N2. The start bit and the stop bit are performed in software. The LSB is shifted first.

IDB[ ]	31:10	9	8	7:1	0
	Not used	Stop bit	UART data[7:0] [MSB:LSB]		Start bit
Function	Not used	Stop bit	Parity	UART data[6:0] [MSB:LSB]	Start bit
	Not used	Stop bit	Stop Bit	UART data[6:0] [MSB:LSB]	Start bit

4.2.11 UART Status Register (UART_statReg)

The level triggered UART interrupt in the niarReg and in the fiarReg are further decoded by the UART_statReg. An interrupt is generated when at least one bit changes (0-> 1) (bits 3:2).
Reading the UART_statReg will clear the 'RxBuffer full interrupt flag' and the 'TxBuffer empty interrupt flag'.

The 'Request to Send' signal is reset by reading the UART_Reg.

After receiving the UART 'TxBuffer empty interrupt flag' a new data word must be written in the UART RxTxData register. If an other word should be transmitted, the start bit must be set to '0'.

If the transmission should be stopped the start bit has to be set to '1'. The next byte to be transmitted can be directly written into the RxTxData register with the start bit set to '0'.

There is no status information for 'TxBuffer empty' and 'RxBuffer full'.
The 'TX busy' and 'Read back of the Start Bit' are status bits and show the state of the UART.

IDB[ ]	Code	Function
31:5	-	not used
4	0	Stop bit present
	1	Stop bit missing or static low at UART input
3	0	RxBuffer empty
	1	RxBuffer full interrupt flag
2	0	TxBuffer full
	1	TxBuffer empty interrupt flag
1	0	TX idle
	1	TX busy
0	-	Read back of the Start Bit

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4.2.12 D-channel RxData Register (D_RxReg)

D-channel receive data register is read only. Shift direction is LSB first. It contains max. four D-channel octets excluding the start flag, least significant octet first.

IDB[ ]	31:24	23:16	15:8	7:0
Data Read Only	MSB 4.Byte LSB	MSB 3.Byte LSB	MSB 2.Byte LSB	MSB 1.Byte LSB

The received bytes are shifted from left to right. If less than 4 were received only the left bytes are valid. The number of bytes is indicated in the idcReg[12:7] after an RxSFD (Rx Stop Flag Detected) interrupt occurred.
########

4.2.13 D-channel TxData Register (D_TxReg)

The D-channel transmit data register is write only. Shift direction is LSB first. The register contains max. four D-channel octets excluding the start- and stop flags, least significant octet first.

IDB[ ]	31:24	23:16	15:8	7:0
Data Write Only	MSB 4. Byte LSB	MSB 3. Byte LSB	MSB 2. Byte LSB	MSB 1. Byte LSB

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4.2.14 S0 RxData Register (S0_RxReg)

The 27-bit S0 data read only register contains the B-channels and the S0 bits. Bit[26] shows the actual 4 kHz S0 frame sync. This information is required to distinguish different functions of the same bit position in the corresponding S0 frame part.

The D bits are connected to the D-channel controller but the CPU can read this D bits including the zero-insert and delete bits and the start and stop flags, e.g. in the D-channel transparent mode for test purposes.

IDB[ ]	Function (Read Only)	
31:27	Not Used	
26	4 kHz S0 frame sync	
	= 0	= 1
25	F_L	M
24	B7 MSB	B7 MSB
23	B6	B6
22	B5	B5
21	B4 1.B-channel data	B4 1.B-channel data
20	B3	B3
19	B2	B2
18	B1	B1
17	B0 LSB	B0 LSB
16	E4	E2
15	D1	D1
14	A	Not used
13	FA	Not used
12	N	S
11	B7 MSB	B7 MSB
10	B6	B6
9	B5	B5
8	B4 2.B-channel data	B4 2.B-channel data
7	B3	B3
6	B2	B2
5	B1	B1
4	B0 LSB	B0 LSB
3	E1	E3
2	D2	D2
1	Not used	L
0	Not used	FR

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4.2.15 S0 TxData Register (S0_TxReg)

The 26-bits S0 data write only register contains the B-channels and the S0 bits. If multiframing is set to CPU control in the configS0Reg the multiframing bit is writeable depending on the 4 kHz S0 frame synch (S0_Rx bit[26]).

The D bits are connected to the D-channel controller but the CPU can write these D bits including the zero-insert and delete bits and start and stop flags, e.g. in the D-channel transparent mode for test purposes.

IDB[ ]	Function (Write Only)	
31:26	Not used	
	4 kHz S0 FrameSync S0_RxReg[26]	
	= 0	= 1
25	F_L: set by D-chan. contr.	D_L: set by D-chan. contr.
24	B7 MSB	B7 MSB
23	B6	B6
22	B5	B5
21	B4 1.B-channel data	B4 1.B-channel data
20	B3	B3
19	B2	B2
18	B1	B1
17	B0 LSB	B0 LSB
16	B_L: set by D-chan.-contr.	B_L: set by D-chan. contr.
15	D1	D1
14	D_L: set by D-chan contr.	D_L: set by D-chan. contr.
13	F_A: set by D-chan. contr. or by CPU	Not used
12	F_L: set by D-chan. contr.	Not used
11	B7 MSB	B7 MSB
10	B6	B6
9	B5	B5
8	B4 2.B-channel data	B4 2.B-channel data
7	B3	B3
6	B2	B2
5	B1	B1
4	B0 LSB	B0 LSB
3	B_L: set by D-chan. contr.	B_L: set by D-chan. contr.
2	D2	D2
1	Not used	D_L: set by D-chan. contr.
0	Not used	FR: set by D-chan. contr.

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4.2.16 ISDN Control Register (idcReg)

This register communicates with the D-channel controller and the S0_Rx/TxReg.
The S0 DPLL must be in sync before the D-channel controller can be started. The D-channel receiver must have been enabled before the D-channel transmitter can be started.
The D-channel software reset disables the D-channel transmitter in any CPU mode. Enable of the D-channel transmitter must be done in the fast interrupt mode which is driven from the S0 FSC interrupt source.

IDB[ ]	Code	Function	Reset Value
31:18	-	Not Used	0000 0000 0000 00
17	0	S0_RxReg & S0_TxReg working in normal mode *)	0
	1	Testloop, do not use	
16:13		Echo counter value[3:0], count the 8 kHz S0 FrameSynch's as long as the S0 bus is in the idle state (D-bits == "1") to realise the S0 priority scheme for D-channel TxStart **)	0 000
12:7		D-bit RxBuffer count stored the number of D-bits in ordering of HDLC octets. The last octet can be ignored because it is the stop flag.	0 0000 0
6:4		Frame end control[2:0] for D-Tx octets to send from the D-TxReg buffer (Stop flag generated automatically, not stored as an octet in the D-TxReg)	111
	111	send 4 octets with more followed octets	
	011	send 4 octets followed by a stop flag	
	010	send 3 octets followed by a stop flag	
	001	send 2 octets followed by a stop flag	
	000	send 1 octets followed by a stop flag	
3	0	D-channel controller deactivated. S0 D-bits are transparent for CPU control (for Tx only). **)	1
	1	D-channel controller active, automatic Null Bit_Ins/Del and start/stop-flag generation.	
2	0	D-channel transmission disable ***)	0
	1	D-channel transmission enable, TxStartFlag begin with the next 8 kHz S0 FSC. If a D-collision on the S0 bus happened, the D-channel transmitter automatically stops and the idcReg[2] bit will be reset to "0".	
1	0	D-channel receiver disable ***)	0
	1	D-channel receiver enable. Every higher level RxEvent generates a D-Rx interrupt, see "niarReg".	
0	0	Disable all S0 data shift register and the D-channel controller for Power Down option.	1
	1	Enable D-channel controller ***)	

*) If a B-channel testloop is required, e.g. for layer 1 measurements, this loop has to be implemented in software.

**) This counter is updated only every half frame. Bits [23:20] in the configS0_Reg represent a more precise value.

***) D-channel control

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For a summary of the control of the D-channel controller see the table below.

Function	IDB[3]	IDB[2]	IDB[1]	IDB[0]	Reset Value
D-channel controller power down	x	x	x	0	0000
D-channel controller transparent: D-channel HDLC-frames generated by the CPU	0	x	x	1	
D-channel receiver disabled	1	x	0	1	
D-channel receiver enabled	1	x	1	1	
D-channel transmitter disabled	1	0	x	1	
D-channel transmitter enabled	1	1	x	1	

Table 4-2: D-Channel Control

4.2.17 SDCI LSWord Rx/TxData Register (sdci_lswReg)

This register contains the least significant 32-bit data word of the 64-bit serial DSP/CODEC interface (SDCI). The shift direction is MSB first. The SDCI data register are shadowed and should be read respectively written with the fast interrupt of FSC1 phaseX.

IDB[ ]	31:24	23:16	15:8	7:0
Function	MSB 4.Byte LSB	MSB 3.Byte LSB	MSB 2.Byte LSB	MSB 0.Byte LSB

4.2.18 SDCI MSWord Rx/TxData Register (sdci_mswReg)

This register contains the most significant 32-bit data word of the 64-bit serial DSP/CODEC interface. The shift direction is MSB first. The SDCI data register are shadowed and should be read respectively written with the fast interrupt of FSC1 phaseX.
Byte 8 is the first byte transmitted in the SDCI frame.

IDB[ ]	31:24	23:16	15:8	7:0
Function	MSB 8. Byte LSB	MSB 7. Byte LSB	MSB 6. Byte LSB	MSB 5. Byte LSB

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4.2.19 SDCI Control Register (sdci_cntrReg)

The control register of the SDCI interface. The register is read write.
By hardware wiring of the ConfTest pins SDCI master mode or SDCI slave mode is selected.

IDB[ ]	Code	Function	Reset Value
31:10	-	Not used	0
9:8		special function for SDCI master mode at 2048 kHz bit shift clock	00
	11	access to 4*64 bit, FSC1 generated phase info on FSC2 / 3 phase FSC3 FSC2 1 0 0 2 0 1 3 1 0 4 1 1	
	10	access to 4*64 bit, FSC1 - FSC3 generated	
	0x	access to first 64 bit	
7:5		SDCI bit shift clock frequency select (only master mode) *)	010
	111	do not use	
	110	512 kHz	
	101	768 kHz	
	100	1024 kHz	
	011	1536 kHz	
	010	2048 kHz (see bit [9:8])	
	001	do not use	
	000	do not use	
4		Bit shift clock doubleclocking (only master mode)	0
	0	off	
	1	on	
3	0	Generate late FSC3	0
	1	Generate early FSC3	
2	0	Generate late FSC2	0
	1	Generate early FSC2	
1	0	Generate late FSC1	0
	1	Generate early FSC1	
0		External frame sync FSC (only slave mode)	0
	0	late FSC	
	1	early FSC	

*) The sysClockReg [23:21] bits have to be set to the same value

Definition: Late FSC: The FSC high pulse encloses the rising edge of the first bit clock.
Early FSC: The FSC high pulse encloses the falling edge of the first bit clock.

For the impact on the timing see chapter '**SDCI**' on page 81.

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4.2.20 VBAFE - Rx/TxData Reg. #1 (VBAFEpcm1Reg)

This register contains the 14-bit PCM data the handset-path of the VBAFE.

IDB[ ]	31:14	13:0
Function	Not used	MSB[13] - LSB[0] PCM_Data
Reset Value	0	0

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4.2.21 VBAFE Control Register (VBAFEReg)

This is the VBAFE control register. Register is read / write.

IDB[ ]	Code	Function	Reset Value
31		ringer output control *)	0
	0	powerdown	
	1	enable ringer	
30		clock switch	0
	0	full speed (36,864 M or LP oscillator)	
	1	1/3 speed (incoming clock is divided by 3 for the ARM core)	
29:27		not used, must be set to '000'	00 0
26:24		Volin2[2:0], volume in control bits #2	000
23:22	00 / 11	VBAFE normal mode	00
	01 / 10	Reset the VBAFE digital filter for synchronisation with 8 kHz frame synch "SDCI FSC".	
21:20	00	analogue - analogue loopback & digital - digital loopback	00
	01	normal operation	
	10	do not use	
	11	analogue - digital - digital - analogue loopback	
19		General power control for VBAFE	0
	0	Power up	
	1	Power down	
18	0	Not used for normal operation	0
	1	Must be set for normal operation	
17		micro reference; should be set to "1"	0
	0	Power up	
	1	Power down	
16		no function, can be used by user for storage of one bit	0
15		Amplifier #2 *)	0
14		Amplifier #1	0
	0	Power up	
	1	Power down	
13:11		Pr_cnf[2:0], Preamplifier Configuration Bits	00
	0x0	Normal operation; Vxip & Vxin selected as input	0
	001	Normal operation; Auxip & Auxin selected as input	
	011	Preamp test mode	
	100	Preamp powered down, 7.6 dB attenuation on Vxip & Vxin	
	101	Preamp powered down, 7.6 dB attenuation on Auxip & Auxin	
	110	Preamp powered down, Vxip & Vxin send directly to the input of the sigma-delta; biasing resistor are connected for AC coupled inputs	
	111	Preamp powered down, Vxip & Vxin send directly to the input of the sigma-delta; biasing resistor are disconnected for DC coupled inputs	
10:8		Volin1[2:0], volume in control bits #1 **)	000
7:4		Volout[3:0], volume out control bits for amp #1 **)	0000
3:0		Volout[3:0], volume out control bits for amp #2 (handsfree path) **)	0000

*) either the ringer or the handsfree path (amplifier #2) should be enabled.

) see **Table 5-9 - **Table 5-11** for the values to be used.

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4.2.22 PIO1 Status Register (pio1_statReg)

This is the write only control register for the PIO1[18:0] ports, PIO1[19:23] are controlled by the pio2_statReg.

IDB[ ]	Code	Function Write Only	Reset Value
31:25	-	not used	-
24		Control bit for PIO1[18], 1 = Output, 0 = Input	0
23		Control bit for PIO1[17], 1 = Output, 0 = Input	0
22		Control bit for PIO1[16], 1 = Output, 0 = Input	0
21		Control bit for PIO1[15], 1 = Output, 0 = Input	0
20		Control bit for PIO1[14], 1 = Output, 0 = Input	0
19		Control bit for PIO1[13], 1 = Output, 0 = Input	0
18		Control bit for PIO1[12], 1 = Output, 0 = Input	0
17		Control bit for PIO1[11], 1 = Output, 0 = Input	0
16		Control bit for PIO1[10], 1 = Output, 0 = Input	0
15		Control bit for PIO1[9], 1 = Output, 0 = Input	0
14		Control bit for PIO1[8], 1 = Output, 0 = Input	0
13		Control bit for PIO1[7], 1 = Output, 0 = Input	0
12		Control bit for PIO1[6], 1 = Output, 0 = Input	0
11		Control bit for PIO1[5], 1 = Output, 0 = Input	0
10		Control bit for PIO1[4], 1 = Output, 0 = Input	0
9		Control bit for PIO1[3], 1 = Output, 0 = Input	0
8:6		Control bits for PIO1[2], as input generates normal extINT #2	0 00
5:3		Control bits for PIO1[1], as input generates normal extINT #1	00 0
2:0		Control bits for PIO1[0], as input generates fast extINT	000
	000	Input, interrupt low active	
	001	Input, interrupt high active	
	01x	no function	
	1xx	Output	

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4.2.23 PIO1 Data1 Register (pio1_set1Reg)

This register sets the output of the PIO1[ ] to one if a one is written into the corresponding bit position. Writing a zero to this register does not have any effect. Reading this register gives the input value of the corresponding PIO1's. Reset value is zero.

IDB[ ]	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIO1[ ]	-	-	-	-	-	-	-	-	-	22	21	20	19	18	17	16

IDB[ ]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIO1[ ]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

4.2.24 PIO1 Data0 Register (pio1_set0Reg)

This register sets the output of the PIO1[ ] to zero if a one is written into the corresponding bit position. Writing a zero to this register does not have any effect. Reading this register gives the input value of the corresponding PIO1's. Reset value is one.

IDB[ ]	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIO1[ ]	-	-	-	-	-	-	-	-	-	22	21	20	19	18	17	16

IDB[ ]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIO1[ ]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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4.2.25 PIO2 Status Register (pio2_statReg)

Control register for the PIO1[22:19] and for the PIO2[9:0]. PIO2[10] is not programmable and is the output of the D / A-converter to be used e.g. for the control of the LCD contrast.
The register is write only.

IDB[ ]	Code	Function	Reset Value
31:29	-	Not Used	000
28		Control bit for PIO1[19] multifunction output	0
	0	Multifunction output PIO1[19] is UART request to Send /RTS	
	1	Multifunction output PIO1[19] is S0_DPLL frame sync	
27:26		Control bits for PIO2[9]	00
	10	S0-Monitor1, input	
	11	SDCI-8 MHz clock, output	
	-	TDO-P output pin of the debug interface (in ARM7 debug mode) *)	
25:24		Control bits for PIO2[8]	00
	10	S0-Monitor0, input	
	11	SDCI-4 MHz clock, output	
	-	ECLK output pin of the debug interface (in ARM7 debug mode) *)	
23:22		Control bits for PIO1[22], Multifunction output is SDCI FSC 8 kHz	00
21:20		Control bits for PIO1[21], Multifunction output is address line A[22] Multifunction input is ext. frame synch for the SDCI **)	00
19:18		Control bits for PIO1[20], Multifunction output is address line A[21]	00
17:16		Control bits for PIO1[19], Multifunction output depends on bit [28]	00
15:14		Control bits for PIO2 [7], Multifunction output is FSC3 of the SDCI	00
13:12		Control bits for PIO2 [6], Multifunction output is FSC2 of the SDCI	00
11:10		Control bits for PIO2 [5], Multifunction output is /CS16c	00
9:8		Control bits for PIO2 [4], Multifunction output is /CS16b	00
7:6		Control bits for PIO2 [3], Multifunction output is /CS16a	00
5:4		Control bits for PIO2 [2], Multifunction output is /CAS1	00
3:2		Control bits for PIO2 [1], Multifunction output is /CAS0	00
1:0		Control bits for PIO2[0], Multifunction output is /RAS	00
	00	Input	
	01	Output	
	1x	Multifunction active	

*) This function is selected by the external ConfTest pins.
**) For usage as ext. frame synch input IDB[21:20] has to be set to [00].

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4.2.26 PIO2 Data1 Register (pio2_set1Reg)

This register sets the output of the PIO2[ ] to one if a one is written in to the corresponding bit position and in parallel the corresponding bit in pio2_set0Reg[ ] is reset to zero. Writing a zero to this register does not have any effect. Reading this register gives the input value of the corresponding PIO2's. Reset value is zero.

IDB[ ]	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIO2[ ]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

IDB[ ]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIO2[ ]	-	-	-	-	-	-	9	8	7	6	5	4	3	2	1	0

4.2.27 PIO2 Data0 Register (pio2_set0Reg)

This register sets the output of the PIO2[ ] to zero if a one is written into the corresponding bit position and in parallel the corresponding bit in pio2_set1Reg[ ] is reset to zero. Writing a zero to this register does not have any effect Reading this register gives the input value of the corresponding PIO2's. Reset value is one.

IDB[ ]	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIO2[ ]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

IDB[ ]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIO2[ ]	-	-	-	-	-	-	9	8	7	6	5	4	3	2	1	0

4.2.28 Key Pad Data Register (keypadReg)

With the keypad register the KEYin[6:1] pins can be read on D[5:0]. If any "high" signal occurred on the KEYin-lines a keypad normal interrupt will be generated. This interrupt is intended to be used as a wake-up signal only.

IDB[ ]	31:6	5:0
Function	Not used	KEYin[6:1]

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4.2.29 Clock Control Register (sysClockReg)

4.2.29.1 Clock Control Register (sysClockReg) Write

The clock system combines the clock divider for the 36.864 MHz clock, the UART baudrate generator with power down option and the syncFSC generator.

The switch over between the 36.864 MHz oscillator and the 460.8 kHz oscillator as a baudrate source and the on / off-switch of the clock divider is done clock synchronously on the falling edge of the clock.

The BSCK and the SDCI clocks and the three SDCI FSC signals are synchronous with the syncFSC. The reference signal for the syncFSC generation can be selected out of four possible sources. The reference source selection for syncFSC can be controlled by the CPU or by the automatic.

IDB[ ]	Code	write Function	Reset Value
31:28	-	Not used, must be set to '0'	0000
27		syncFSC reference source select if S0_PLL is locked	0
	0	S0_ FSC is reference source	
	1	S0 bit clock is reference source	
26:24		BSCK output clock frequency select	010
	111	do not use	
	110	512 kHz	
	101	768 kHz	
	100	1024 kHz	
	011	1536 kHz	
	010	2048 kHz	
	001	4096 kHz	
	000	do not use	
23:21		SDCI bit shift clock frequency select *)	010
	111	do not use	
	110	512 kHz	
	101	768 kHz	
	100	1024 kHz	
	011	1536 kHz	
	010	2048 kHz	
	001	do not use	
	000	do not use	
20		UART baudrate clock source select	0
	0	Clock source is 36.864 MHz oscillator	
	1	Clock source is 460.8 kHz oscillator	
19		Value for watch dog **)	0
	0	Watch dog timer is 2.56 s	
	1	Watch dog timer is 1.28 s	
18		8192 kHz clock inverting / non-inverting	0
	0	non-inverted	
	1	inverted	
17		4096 kHz clock inverting / non-inverting	0
	0	non-inverted	
	1	inverted	
16:15		for test only	0 0
14	0	clock divider active	0
	1	power down of the clock divider	
13:9		for test only	00 000
8		Reference for syncFSC controlled by CPU or automatic	0
	0	as set in IDB[7:6]	
	1	as set in IDB[7:6] when S0_PLL is unlocked as set in IDB[27] when S0_PLL is locked	

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IDB[ ]	Code	write Function			Reset Value
7:6		Reference source for syncFSC			00
	11	S0 bit clock (192 kHz) when S0_PLL is locked S0 bit clock (192 kHz + 5400 ppm) when S0_PLL is not locked			
	10	external FSC (max. 1 MHz)			
	01	S0_FSC (8 kHz) when S0_PLL is locked: ***) S0_FSC (8 kHz + 5400 ppm) when S0_PLL is not locked			
	00	8 kHz based on CPU clock; not in sync with S0			
5:4		for test only			00
3:0		UART baudrate control			1100
		baudrate / kBaud	clock / kHz	Clock source for clock divider	
	0000	1.2	9.6		
	1000	2.4	19.2	from low power oscillator (460.8 kHz)	
	0100	4.8	38.4	IDB[20]= 1	
	1100	9.6	76.8	&	
	0010	19.2	153.6	xinocReg set to low power oscillator	
	1010			from low power oscillator (460.8 kHz)	
	to	0	0	IDB[20]= 1	
	1111			UART powered down	
	0000	1.2	9.6		
	1000	2.4	19.2	from normal oscillator (36.864 MHz)	
	0100	4.8	38.4	IDB[20]= 0	
	1100	9.6	76.8	&	
	0010	19.2	153.6	xinocReg set to normal oscillator	
	1010	38.4	307.2		
	0110	57.6	460.8		
	1110	115.2	921.6		
	xxx1	230.4	1843.2		

*) The sdci_cntrReg [7:5] bits have to be set to the same value
**) Watchdog time depends on clock for the ARM core. Values given, are for 36.864 MHz operation.
***) In this mode the SDCI frame is synchronised to the S0 bus.

Clock System Control Register (sysClockReg) Read
By reading the sysClockReg the CPU can generate various timer based on the frequencies listed. Reading the bits [14:4], the read value can be interpreted as a binary coded real time clock.

IDB[ ]	Read Function
31:15	undefined (value may change)
14	Clock output 6 kHz
13	Clock output 12 kHz
12	Clock output 24 kHz
11	Clock output 48 kHz
10	Clock output 96 kHz
9	Clock output 192 kHz
8	Clock output 384 kHz
7	Clock output 768 kHz
6	Clock output 1536 kHz
5	Clock output 3072 kHz
4	Clock output 6144 kHz
3	LSB of the UART baudrate setting
2	UART baudrate setting
1	UART baudrate setting
0	MSB of the UART baudrate setting

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4.2.30 LCD Contrast Control Register (DAC_Reg)

With this register the output of the DAC e.g. to be used for the LCD contrast control will be set. In conjunction with the external load IDB[7:0]= FF hex give a high output. In the power down mode the output is in the high impedance state.

IDB[ ]	31:9	8	7:0
Function	Not used	1 =: power on 0 =: power down	MSB : LSB

4.2.31 VBAFE - RxData Reg. #2 (VBAFEpcm2Reg)

This register contains the 14-bit PCM data for the loudspeaker path the of the VBAFE.

IDB[ ]	31:14	13:0
Function (write only)	Not used	MSB[13] - LSB[0] PCM_Data
Reset Value	0	0

Writing the VBAFEpcm2Reg only will not transfer the data to the DAC. To make sure that the data are transferred to the DAC the VBAFEpcm1Reg has to be written just after writing the VBAFEpcm2reg.

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5. PHYSICAL PARAMETER

5.1 Maximum Ratings

This device may not operate under conditions outside the maximum ratings. Once the conditions are returned to within the specified maximum ratings or the power is recycled, the module will recover with no damage or degradation.

Input Signals	-0.5 V to VDD + 0.5 V
Supply Voltage	4.5 to 5.5 V
Junction Temperature	0ºC to +125ºC

5.2 Absolute Maximum Ratings

This device may be irreparably damaged under conditions outside the specified absolute maximum rating range.

Input Signals	-0.5 to 7.0 V
Supply Voltage	-0.5 to 7.0 V
Storage Temperature	-65ºC to +150ºC
Max. Junction Temperature	< +125ºC

5.3 Operating Temperature Range

Minimum Ambient Temperature	0ºC
Maximum Ambient Temperature	70ºC

5.4 Package

Package Type	Metric Quad Flat Pack
Pin Count	160
Lead Pitch	0.65 mm (typical)
Infrared reflow	
Maximum solder temperature	235ºC
Maximum solder duration	10 sec.
Vapor-phase reflow	
Maximum solder temperature	215ºC
Maximum solder duration	30 sec.

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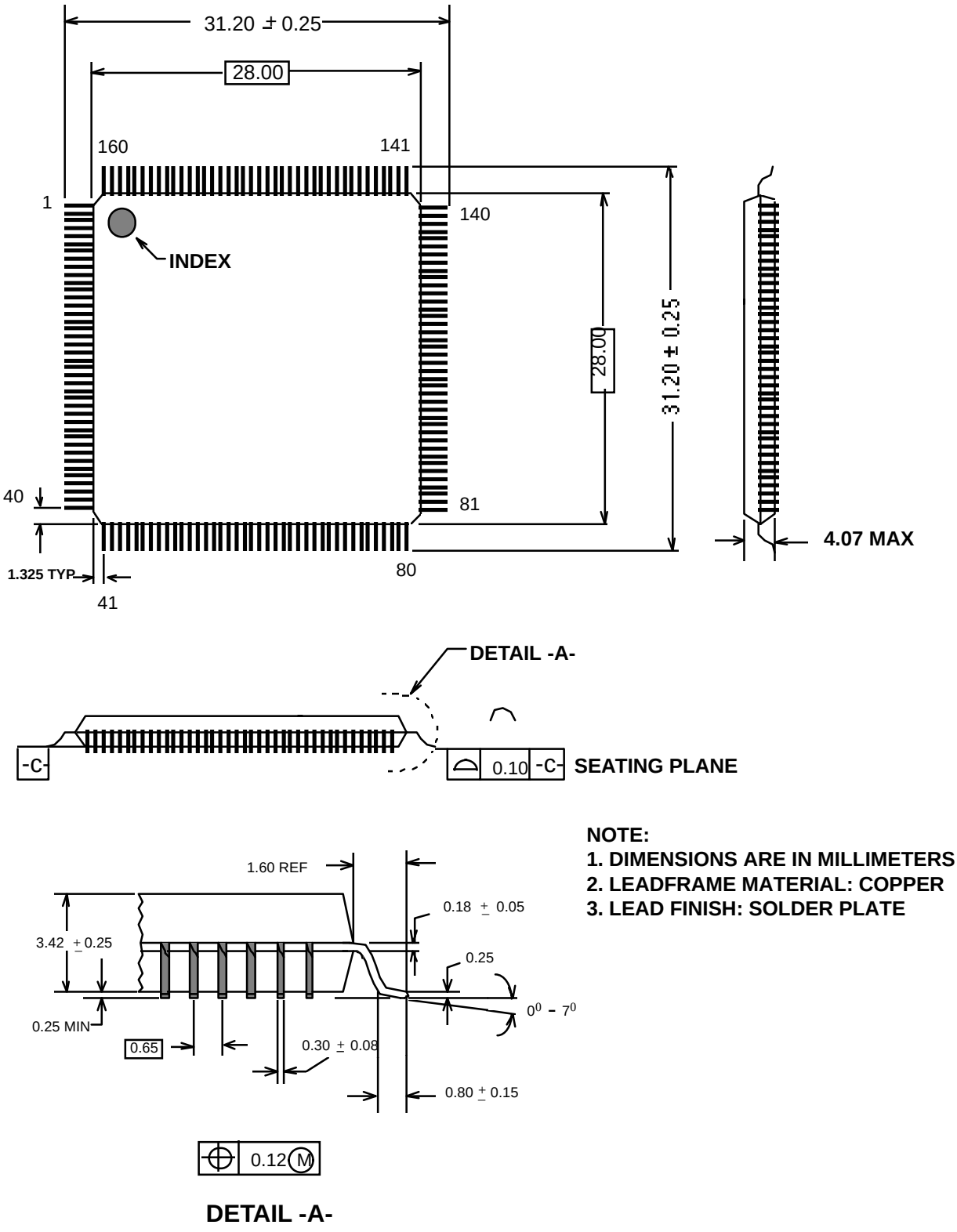
5.4.1 Package Outline



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. LEADFRAME MATERIAL: COPPER
3. LEAD FINISH: SOLDER PLATE

Figure 5-1: Package Outline

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5.5 Power Specification

Parameter	VDD=5V	VDD=5.25V	Comment
Deactivated [State F3]	11 mW	12 mW	f = 460 kHz [1]
Deactivated [State F3]	220 mW	240 mW	f = 36.864 MHz; TE in " local action" [2]
Activated [State F7]	270 mW	297 mW	f = 36.864 MHz; one loudspeaker and one microphone amplifier are activated [3]
Activated [State F7]	238 mW	261 mW	f = 36.864 MHz; UART with 19.2 kBaud / s is activated [4]
Activated [State F7]	235 mW	260 mW	f = 36.864 MHz; SDCI is activated [5]
Activated [State F7]	273 mW	300 mW	f = 36.864 MHz; one loudspeaker, one microphone amplifier and the UART with 19.2 kBaud / s are activated [6]

Table 5-1: Power Specification

[1] S0 receiver standby, timers active, all PIOs configured as inputs (high)

[2] S0 receiver standby, timers active, all PIOs configured as inputs (high)

[3] int. RAM utilized 4%, S0 active, D-channel controller active, one path of the VBAFE active, clock tree active, timers active, all PIOs configured as inputs (high)

[4] int. RAM utilized 4%, S0 active, D-channel controller active, clock tree active, timers active, UART active, all PIOs configured as inputs (high)

[5] int. RAM utilized 4%, S0 active, D-channel controller active, clock tree active, timers active, SDCI active, all PIOs configured as inputs (high)

[6] int. RAM utilized 4%, S0 active, D-channel controller active, one path of the VBAFE active, clock tree active, timers active, UART active, all PIOs configured as inputs (high)

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5.6 S0 Interface

5.6.1 SO Transmitter

Parameter	Min.	Max.	Unit	Comment
Nominal frequency	192 ± 100 ppm		kHz	
Output current	7.5	-	mA	
Output on voltage	-	100	mV	
Timing extraction jitter	-7	+7	%	of one bit period
Output delay	-760	440	ns	relative to input phase programmable in 16 steps
Output pulse width	4.7	5.7	µs	
Total input to output phase deviation	-7	+15	%	of one bit period

Table 5-2: Parameter of the S0-Transmitter

5.6.2 SO Receiver

Parameter	Min.	Max.	Unit	Comment
Input transformer ratio	1:2		-	recommended ratio
Input threshold	± 4.0	± 6.0	µA	100 % value
Input threshold	± 1.6	± 5.0	µA	nominal adj. range
Zero-crossing detection hysteresis	± 0.3	± 1.3	µA	nominal adj. range
Input current		100	µA	
Common mode voltage	0	5	V	
Internal resistance (typical)	300		W	
capacitor Cref - GND (typical)	1…10		nF	decoupling cap.
capacitor Ref - GND (typical)	220		nF	decoupling cap.

Table 5-3: Parameter of the S0-Receiver

5.6.3 SO PLL

Parameter	Min.	Max.	Unit	Comment
Acquisition time	-	100	ms	-
Phase compensation	-	± 80	ns / frame	S0 PLL locked
Phase compensation	-	1280	ns / frame	S0 PLL not locked
Bit length filter threshold	0.32	4.88	µs	programmable in 16 steps

Table 5-4: Parameter of the S0-PLL

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5.7 VBAFE

Parameter	Min.	Typ.	Max.	Unit
Transmit Absolute Level Nominal 0 dBm0 input level measured with preamplifier bypassed (@ 1020 Hz), differentially between Vxip & Vxin.		308		mVrms
Transmit Peak Input Level 3.14 dBm0 or code ±8192 on 14-bit linear with preamplifier bypassed , differentially between Vxip & Vxin.		625		mVpk
Transmit Absolute Gain Variations	-0.50		0.50	dB
Receive Absolute Levels 1) Nominal 0 dBm0 output level when 0 dB attenuation is programmed through push-pull amplifier (@ 1020 Hz)		0.774		Vrms
Receive Peak Output Level 1) 3.14 dBm0 is code ±8192 on 14-bit linear PCM input		1.572		Vpk
Receive Absolute Gain Variations	-0.50		0.50	dB
Input impedance (differential)	2.7		4.1	kΩ
Output Impedance	1			Ω
decoupling capacitor (Vrefn - Vrefp)		1		µF

Table 5-5: VBAFE Absolute Parameter

1) Measured using attenuation step no. 2.

Parameter	Min.	Typ.	Max.	Unit
Transmit Gain relative to 1020 Hz (at 0 dBm0)				
f = 60 Hz			-23	
f = 200 Hz	-3.0		-0.20	dB
f = 300 Hz to 3000 Hz	-0.20		0.20	
f = 3300 Hz	-0.30		0.20	
f = 3400 Hz	-0.80		0	
f = 4000 Hz			-14	
Receive Gain relative to 1020 Hz (at 0 dBm0)				
f =0 Hz to 3000 Hz	-0.20		0.20	
f = 3300 Hz	-0.30		0.20	dB
f = 3400 Hz	-0.80		0	
f = 4000 Hz			-14	
Transmit Gain Variations with level (1020 Hz sine wave relative to -10 dBm0)				
-10 dBm0 to -40 dBm0	-0.20		0.20	
-40 dBm0 to -50 dBm0	-0.40		0.40	dB
-50 dBm0 to -55 dBm0	-0.80		0.20	
Receive Gain Variations with level (1020 Hz sine wave relative to -10 dBm0)				
-10 dBm0 to -40 dBm0	-0.20		0.20	
-40 dBm0 to -50 dBm0	-0.40		0.40	dB
-50 dBm0 to -55 dBm0	-0.80		0.20	

Table 5-6: VBAFE Frequency Response

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Parameter	Min.	Typ.	Max.	Unit
Signal to Distortion (sinusoidal test method) for Transmit or Receive Half-channel				
Level = 3.0 dBm0	30			dBp
0 dBm0 to -30 dBm0	33			
40 dBm0	28			
55 dBm0	14			
Single Frequency Distortion (2nd & 3rd Harmonics half-channel input: 0 dBm0 at 1020 Hz)	-50			dBm0
Inter Modulation Distortion (loop with 2 freq. in the range 300 Hz to 3400 Hz)		TBD		

Table 5-7: AFE Distortion Characteristic

Parameter	Min.	Typ.	Max.	Unit
Transmit Noise P Message Weighted				
VXIP & VXIN shorted together		-68	-65	dBm0p
Receive noise P message weighted (PCM code equal positive Zero)		-78	-75	dBVrms
Spurious Out-of-Band Signals (loop around 0 dBm0 300-3400 Hz)				
4600 Hz to 7600 Hz			-35	dB
7600 Hz to 8400 Hz			-40	
8400 Hz to 100 000 Hz			-35	
Transmit Absolute Group Delay (0 dBm0 1600 Hz)		TBD		
Transmit Differential Delay (relative to 1600 Hz)				
500 Hz to 600 Hz		TBD		
600 Hz to 1000 Hz		TBD		
1000 Hz to 2600 Hz		TBD		
2600 Hz to 2800 Hz		TBD		
Receive Absolute Group Delay (0 dBm0 1600 Hz)		TBD		
Receive Differential Delay (relative to 1600 Hz)				
500 Hz to 600 Hz		TBD		
600 Hz to 1000 Hz		TBD		
1000 Hz to 2600 Hz		TBD		
2600 Hz o 2800 Hz		TBD		

Table 5-8: VBAFE Noise Characteristic

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Step number VOLIN#1 (2:0)	Level at mic. input giving 0 dBm0 (PCM code = ± 5706) (@VOLIN#2=000)	
	mV_{rms}	Transmit Gain *) dBVrms
0	30.51	30.3
1	21.94	33.3
2	15.35	36.3
3	10.89	39.3
4	7.72	42.3
5	5.48	45.3
6	3.88	48.3
7	2.75	51.3

Table 5-9: Microphone Preamplifier Gain#1

Step number VOLIN#2 (2:0)	Transmit Gain *) /dB
0	0
1	- 0.5
2	-1.0
3	-1.5
4	-2.0
5	-2.5
6	-2.5
7	-2.5

Table 5-10: Microphone Preamplifier Gain#2

*) The total gain for of the transmit path is the sum out of gain #1 and gain #2.

Output	output current/ mA	gain control *)	max. output level V_{rms}/V_{peak}	Receive Gain dBVrms/dBm0
150 Ω electrodynamic or 600 Ω / 1000 pF (handset path)	17	16 steps 2 dB / step	1.76 / 2.49	+1.6 to -28.4
50 Ω electrodynamic (handsfree path)	17	16 steps 2 dB / step	1.76 / 2.49	+1.6 to -28.4
50 Ω electrodynamic (ringer) **)	75	n.a.	n.a. / 3.8	n.a.

Table 5-11: Speaker Interface

*) The max. output level is reached with the output gain control in the VBAFEReg (IDB[7:4] or IDB[3:0]) set to [0000].

**) The ringer generates a square wave output signal. Frequency and amplitude is controlled by Pulse Width Modulation which has to be performed by the CPU.

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5.8 Ports

Pin Number	Signal Name	Type
3-10,13-20, 156-160	ADR[20:0]	Output, drive strength #2
23-30, 33-40	D[15:0]	Bidirec, drive strength #2, with pull-up
43	Xin	36.864 MHz quartz
44	Xout	36.864 MHz quartz
47	XinLP	460 kHz quartz
48	XoutLP	460 kHz quartz
49	UART_SIN	Input
50	UART_SOUT	Output, drive strength #1
65-67, 70-77, 80-84	PIO1[18:3]	Bidirec, drive strength #2, with pull-up
51-58, 61-64, 85-87, 98-99	PIO1[22:19, 2:0] PIO2[9:0]	Bidirec, drive strength #2, without pull-up
100	PIO2[10]	Output, LCD contrast control
103-108	KEYin[6:1]	Input, with pull-down
109-113	ConfTest[5:1]	Input, schmitt trigger, with pull-down
140	/Reset	Schmitt-Trigger-Input, power on reset
141	FSC1	Output, drive strength #2
142	BSCK	Bidirec, drive strength #2
143	SDO	Output, tristate, drive strength #2
144	SDI	Input
147	/WR0	Output, drive strength #2
148	/WR1	Output, drive strength #2
149	/RDio	Output, drive strength #2
150	/RD	Output, drive strength #2
151	/CS16boot	Output, drive strength #2
152	/CS8	Output, drive strength #2
153	/CS8boot	Output, drive strength #2

Table 5-12: I/O Ports

5.8.1 DC Characteristic of the Digital I/O's

Parameter	Min.	Max.	Conditions
Input threshold	2.1 V	2.9 V	5 V, 25 C
Schmitt trigger input high threshold	3.1 V	4.0 V	5 V, 25 C
Schmitt trigger input low threshold	1.1 V	1.8 V	5 V, 25 C
Output low level	-	VSS + 0.1 V	4.5 V; IOL = 0.6 mA
Output high level	VDD - 0.1V	-	4.5 V; IOH = 0.6 mA
Output DC drive strength #1	2.3 mA	8.9 mA	VDS = 0.4 V
Output DC drive strength #2	6.9 mA	26.7 mA	VDS = 0.4 V
Input capacitance		7 pF	
Pull-down current	40 µA	100 µA	only for I/O with pull-up
Pull-up current	50 µA	120 µA	only for I/O with pull-down

Table 5-13: DC Characteristic of the Digital I/O's

5.8.2 AC Characteristic of the Digital I/O's

Parameter	Min.	Max.
Output edge rate drive strength #1	0.18 ns/VpF	0.04 ns/Vpf
Output edge rate drive strength #2	0.06 ns/VpF	0.01 ns/Vpf
Pulse width for level triggered interrupts	300 ns	
Pulse width for edge triggered interrupts	60 ns	
UART clock tolerance	± 100 ppm	± 5%

Table 5-14: AC Characteristic of the Digital I/O's

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5.8.3 Characteristic of the Analogue to Digital Converters

Parameter	Min.	Max.	Comments
Comparator threshold	2.23 V	2.78 V	
Input capacitance		7 pF	
Voltage measuring range	0-2 V	3 - 30 V	with external R, C and one PIO
Resistance measuring range	1kΩ	10 kΩ	with external R, C and one PIO
Voltage threshold measuring range	0 V	30 V	with two external R

Table 5-15: Characteristic of the ADC

5.8.4 Characteristic of the Oscillators

Parameter	Low power oscillator	36 MHz oscillator
Frequency	460 -3648 kHz	36.864 MHz
Frequency tolerance	± 5 %	± 30 ppm
Input capacitance (typical)	7 pF	8 pF
Output capacitance(typical)	7 pF	7 pF

Table 5-16: Oscillator Characteristic

5.8.5 Characteristic of the Power-On Reset

Parameter	Min.	Max.	Comments
Threshold	1.9 V	2.7V	reset active when VDD < threshold
Delay active -> inactive	40 µsec	170 µsec	VDD: 0 V-> threshold reset active -> reset inactive
Delay inactive -> active	20 ns	300 ns	VDD: 5V -> threshold reset inactive -> reset active

Table 5-17: Power-On Reset Characteristic

5.8.6 Characteristic of the LCD Contrast Control

Parameter	Min.	Max.	Comments
Output voltage	0.5	4.9V	@ VDD = 5 V
Load	10 kΩ		vs. VSS

Table 5-18: LCD Contrast Control Characteristic

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5.9 Memory Interface

For the AC and DC characteristic of the memory signals see 5.9. The drive strength of the memory output signals is #2. Delays are measured against the 50% output voltage with 100 pF load.

5.9.1 ROM/RAM Memory Single Write

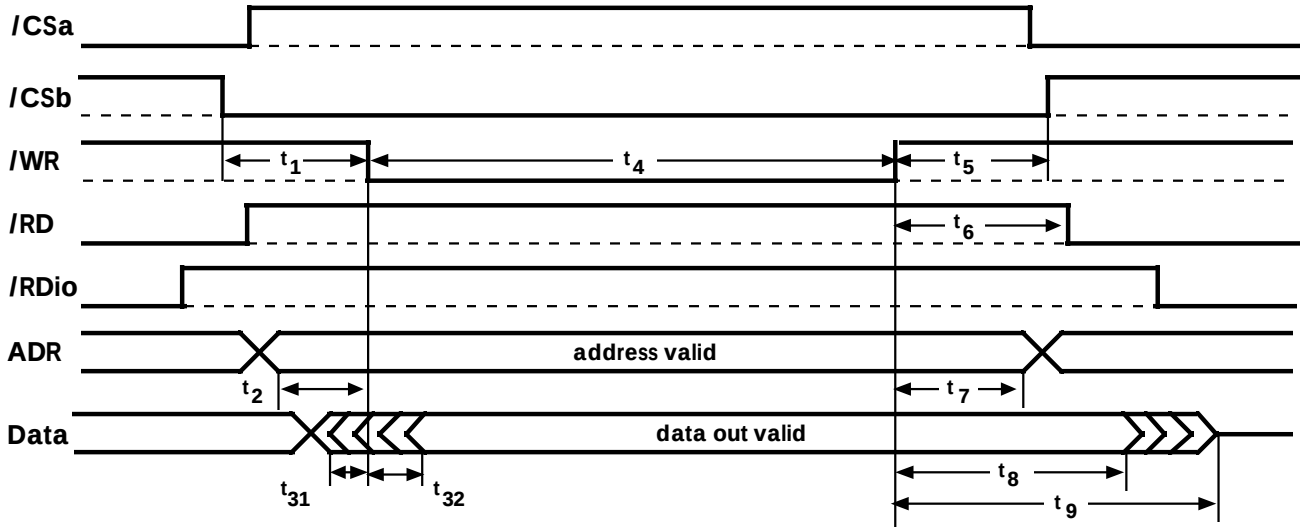

Figure 5-2: ROM/RAM Write Timing Diagram

	Description	min. [ns]	max. [ns]
t_1	/CS active to /WR active	12	14
t_2	address valid to /WR active (address setup)	13	14
t_{31}	data valid to /WR active (data setup)	0	5
t_{32}	data valid to /WR active (data setup)	0	10
t_4	/WR active	28 + 27.1 * #(WS-1)	30 + 27.1 * #(WS-1)
t_5	/WR inactive to /CS inactive	12	13
t_6	/WR inactive to /RD active	14	18
t_7	/WR inactive to address invalid (address hold)	11	13
t_8	/WR inactive to data invalid (data hold)	13	16
t_9	/WR invalid to data HiZ	-	13

Table 5-19: ROM/RAM Write Timing

Note: /CSb is the chip select active for this access. /CSa may be any other chip select. WS: wait state

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5.9.2 ROM/RAM Memory Single Read

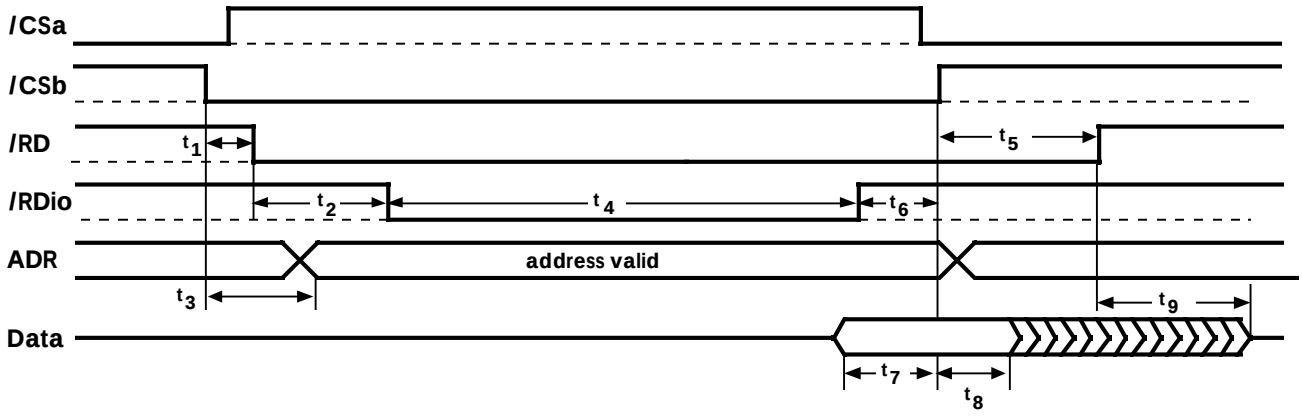

Figure 5-3: ROM/RAM Read Timing Diagram

	Description	min. [ns]	max. [ns]
t_1	/CS active to /RD active	0	3
t_2	/RD to /RDio	26	27
t_3	/CS active to address valid	0	3
t_4	/RDio active	14 + 27 * #(WS-1)	16 + 27 * #(WS-1)
t_5	/CS inactive to /RD inactive	3	7
t_6	/RDio inactive to /CS inactive	11	14
t_7	data-in valid to ADR (data setup)	7	—
t_8	ADR to data-in invalid (data hold)	8	—
t_9	/RD high to data-in Hi-Z	-	13

Table 5-20: ROM/RAM Read Timing

Note: /CSb is the chip select active for this access. /CSa may be any other chip select. WS: wait state

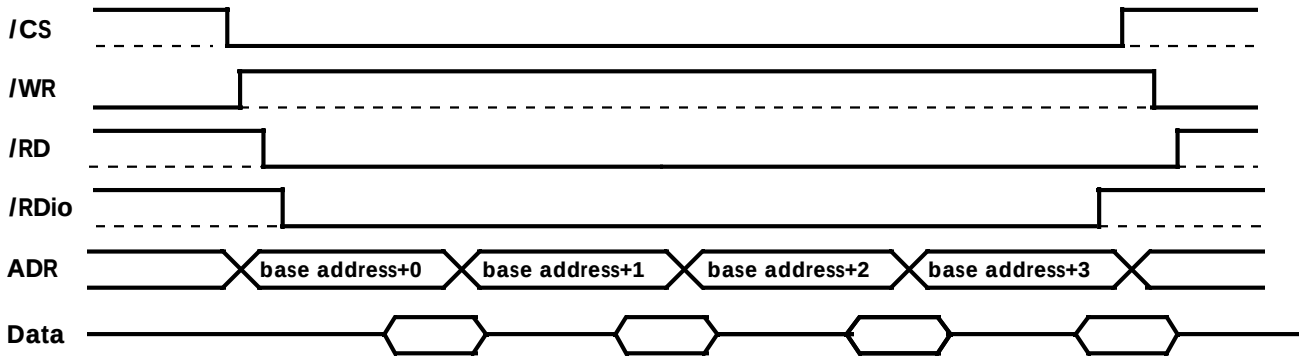

Figure 5-4: ROM/RAM Sequential Read Timing Diagram

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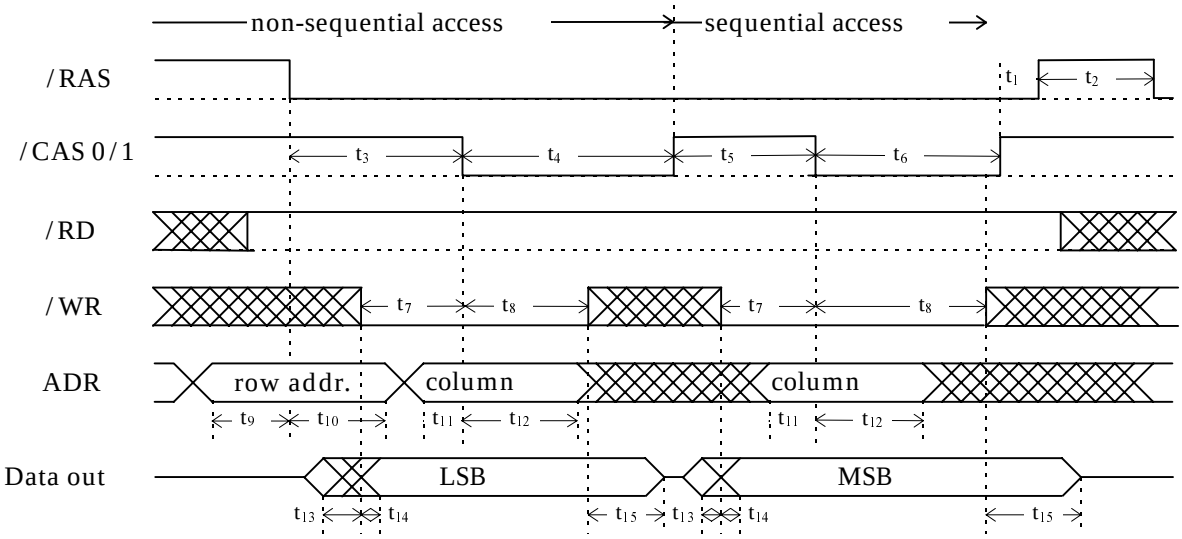
5.9.3 DRAM Write



if the access is 16 bit wide, the address do not change and the second data written is also the LSB

t_2 depends on the settings of mcrReg[15]
t_6 depends on the settings of mcrReg[14]
t_4 depends on the settings of mcrReg[13:12]

Figure 5-5: DRAM Write Timing Diagram

	Description	min. [ns]	max. [ns]
t_1	/RAS hold time	-	4
t_2	/RAS high duration	54 *)	-
t_3	delay between /RAS low & /CAS low	27	31
t_4	/CAS pulse duration (non seq. access)	28 **)	30 **)
t_5	/CAS high duration	24	-
t_6	/CAS pulse duration (seq. access)	28 **)	30 **)
t_7	delay between /WR low & /CAS low	13	14
t_8	hold time after /CAS low	14 **)	17 **)
t_9	setup time row address	11	13
t_{10}	hold time row address	16	18
t_{11}	setup time column address	11	13
t_{12}	hold time column address	16	18
t_{13}	data valid to /WR active (data setup)	0	5
t_{14}	data valid to /WR active (data setup)	0	10
t_{15}	/WR inactive to data invalid (data hold)	13	16

Table 5-21: DRAM Write Timing

Note: Squared addressing with nine to eleven addresses are supported. Always early write cycle.
For 16 bit operation: CAS0 is used for D[7:0] and CAS1 for D[15:8].
For 32 bit operation: A[1] = 0 => CAS0 = D[7:0], CAS1 = D[15:8].
A[1] = 1 => CAS0 = D[23:16], CAS1 = D[31:24]

*) *Short or long RAS precharge pulse software selectable.*

**) *For one wait state, add 1-3 wait states if required.*

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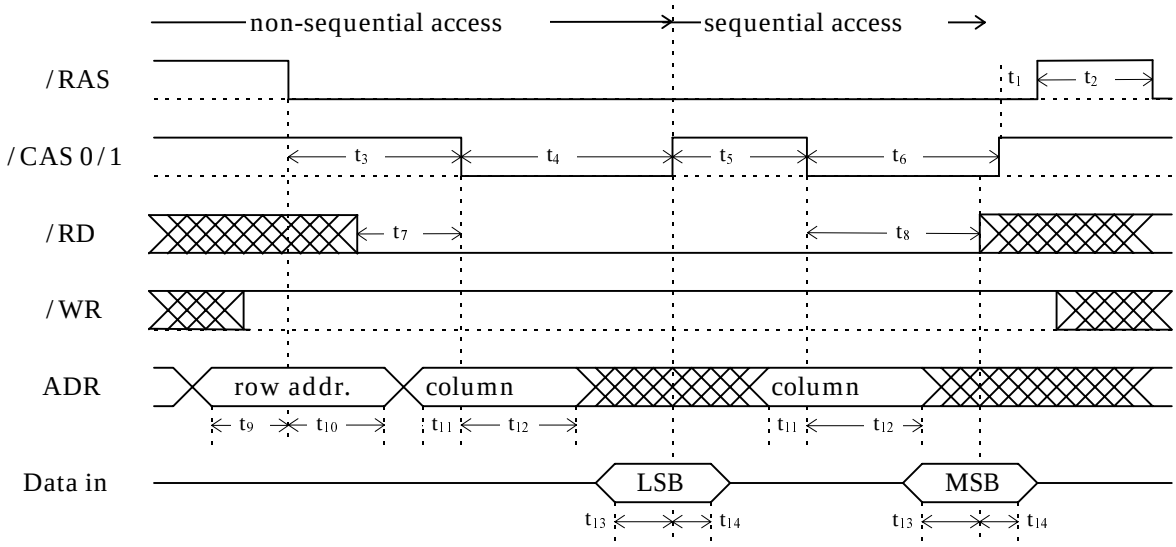
5.9.4 DRAM Read



if the access is 16 bit wide, the address do not change and the second data read is also the LSB

t_2 depends on the settings of mcrReg[15]
t_6 depends on the settings of mcrReg[14]
t_4 depends on the settings of mcrReg[13:12]

Figure 5-6: DRAM Read Timing Diagram

	Description	min. [ns]	max. [ns]
t_1	/RAS hold time	-	4
t_2	/RAS high duration	54 *)	-
t_3	delay between /RAS low & /CAS low	27	31
t_4	/CAS pulse duration (non-seq. access)	28 **)	30 **)
t_5	/CAS high duration	24	-
t_6	/CAS pulse duration (seq. access)	28 **)	30 **)
t_7	delay between /RD low & /CAS low	13	14
t_8	/RD hold time after /CAS low	28 **)	30 **)
t_9	setup time row address	11	13
t_{10}	hold time row address	16	18
t_{11}	setup time column address	11	13
t_{12}	hold time column address	16	18
t_{13}	setup time data	7	-
t_{14}	hold time data	8	-

Table 5-22: DRAM Read Timing

*) Short or long RAS precharge pulse software selectable.
**) For one wait state, add 1-3 wait states if required.

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5.10 SDCI

In the transmit direction the contents of the shadow register will be loaded to the output shift register with the first bit of the 64 bit frame and with the rising edge of the BSCK. In the receive direction the contents of the receive data register will be loaded to the shadow register on receiving of the 64th bit and with the falling edge of the BSCK.

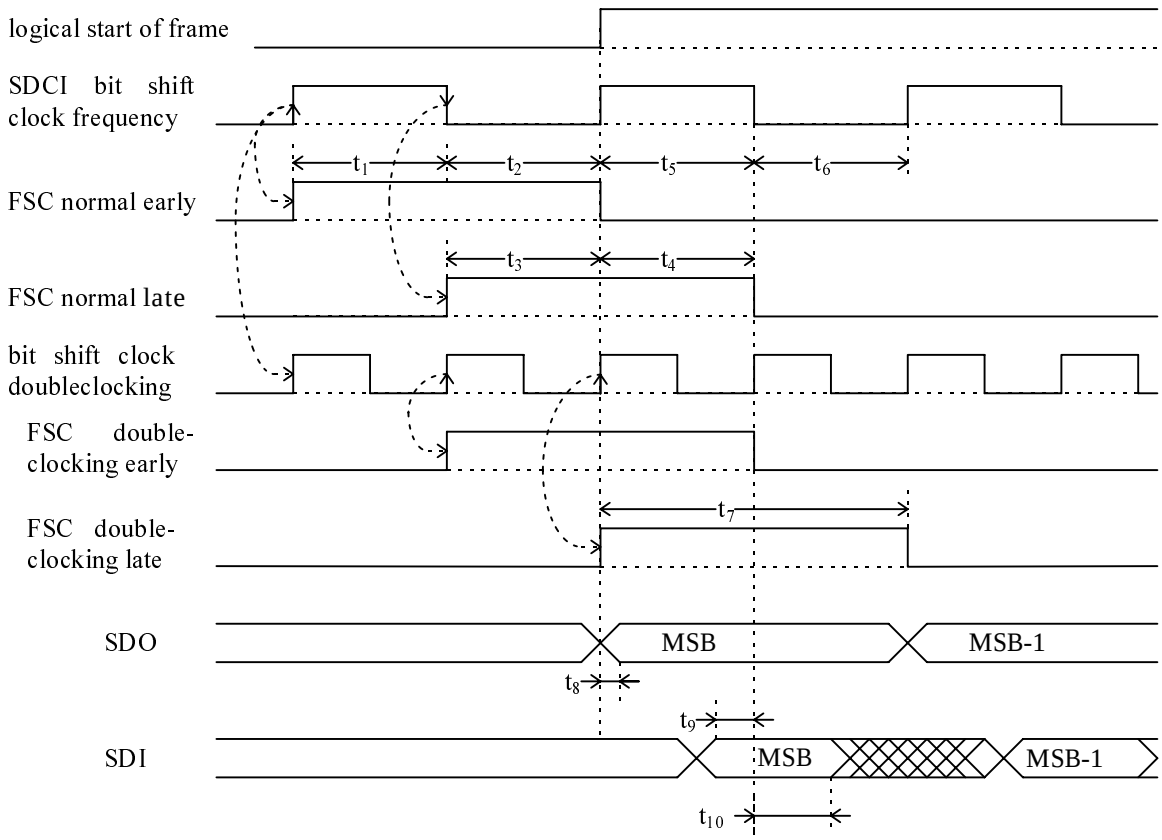

Figure 5-7: SDCI Timing Diagram

	min. [ns]	max. [ns]
t_1	235	240
t_2	245	246
t_3	245	245
t_4	236	242
t_5	236	242

	min. [ns]	max. [ns]
t_6	241	247
t_7	482	494
t_8	-	5
t_9	10	-
t_{10}	5	-

Table 5-23: SDCI Timing

The values given are for a BSCK frequency of 2048 kHz and a SDCI bit shift clock frequency of 2048 kHz. The times for all other frequencies can be calculated accordingly.
The bit shift clock frequency has to be set in the sysClockReg and sdci_cntrReg to the same value.

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6. DEVELOPMENT ENVIRONMENT

6.1 Software Development Tools

6.1.1 JumpStart

The JumpStart ARM development package version 3.1 comes in a box with software on CD-ROM and user manuals. JumpStart supports two different operating systems (platforms): UNIX (Sun / HP) and Windows (PC).

The UNIX version is available for SUN OS and HP OS. The part number is VY86CGUI-U (-UD for demo version).

The Windows version is available for Windows 3.1 / 95 OS. The part number is VY86CGUI-W (-WD for demo version).

The demo versions are valid for a test period of 45 days.
Supported Software

Code-Development Tools
- ANSI C Compiler (supports also thumb code generation and pcc option)
- Linker
- C runtime libraries
- Macro Assembler (supports also thumb code generation)
- Graphical project manager (SUN OS, HP-UX, IBM-AIX, Windows)
- Help-Hypertext Linked Manuals (SUN OS, HP-UX, and IBM-AIX)
- Editor

System Debugging tools
- Command line debugger
- Graphical Debugger-Mixed-Mode C and Assembly (SUN OS, HP-UX, IBM-AIX, and Windows) Execution Environment
- Instruction set emulator

6.1.1.1 Contribution Software

- uC / OS
- HP 1650 / 1660 disassembler
- JPEG software
- Helios OS runtime example
- ARM60 JTAG BSDL file (Genrad Tester)

Note: *The minimum configuration for the UNIX tools is SUN2 performance or better, SUN OS 4.1, 100MB of open disk space for JumpStart installation, and a CD-ROM drive.*

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6.1.2 Operating Systems

6.1.2.1 uC/OS

Attributes:

- Basic tasking libraries
- no file system management
- Jean Labbrosse book (ISBN-no: 0-13-031352-1)
- available Internet address: darkstar.cygnus.com directory/pub/embedded file name "ucos-arm.tar.gz"

6.1.2.2 Accelerated Technology Nucleus/ Nucleus PLUS

Nucleus is intended for software developers who write ONE Multi-Threaded routine. No porting support is included.

Attributes:

- Real-Time, Multi-Threaded Tasking Library (Kernel)
- Priority-Based, Pre-Emptive/Non Pre-Emptive
- Time slicing
- complete source code
- no royalties

6.1.2.3 Helios Realtime Operating System

Helios is intended for software developers who want to write multiple programs (tasks, each of which are multi-threaded) that can be executed on the same system. Porting support is included with Royalties.

Kernel Attributes:

- Real-Time, Multitasking, Multi-Threaded Operating System
- Kernel implements 60 functions and is expandable to support multiple tasks
- Priority-Based, Pre-Emptive/Non Pre-Emptive
- Time slicing
- Complete Source Code
- runs on the PID board

Nucleus Attributes:

- Includes Kernel above and adds libraries to support multiple tasks (system library, server library, loader and processor manager)
- 210 functions
- Optional Attributes:
- X servers and libraries
- TCP/IP (ethernet) libraries and services
- BSD 4.4 fast filing system (disk file system)

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6.2 Development Platforms

6.2.1 Evaluation System

Available on request is an evaluation board (part number: VNSEV80000-3). The evaluation system consists of the following parts:

- The evaluation board equipped with the VIP and its peripherals
- Handset with rest and integrated loudspeaker for loudhearing
- Standard alphanumerical LC-display with two lines, 40 characters each
- Separate power supply.

Equipped with demonstration software, the system implements the functionality of a standard ISDN voice terminal.
The evaluation board itself comprises the following major building blocks:

- VIP as the core
- Universal asynchronous serial interface (V.24)
- High-speed parallel data interface connectable to standard bi-directional PC printer ports
- Alphanumerical 2 x 40 character LC-display connected to the VIP via a parallel interface
- Keyboard matrix consisting of 4 rows and 3 columns ('0' to '9', '#', '*')
- softkeys to implement a menu-driven user interface
- Mbit, 16 bit wide Flash-EPROM, loadable from the serial interface
- Mbit, 8 bit wide static RAM
- Mbit, 16 bit wide DRAM
- Interface circuitry for S0 and handset
- HP logic analyser compatible connectors for all I/O signals and memory busses
- JTAG interface to allow debugging using the embedded ICE

Together with the also available software development tools for the embedded ARM controller, the JTAG interface and the hardware driver this evaluation board is a easily to use plug and play development platform for your ISDN application.
The software described in chapter 'ISDN Software' on page 89, can be used on this board.

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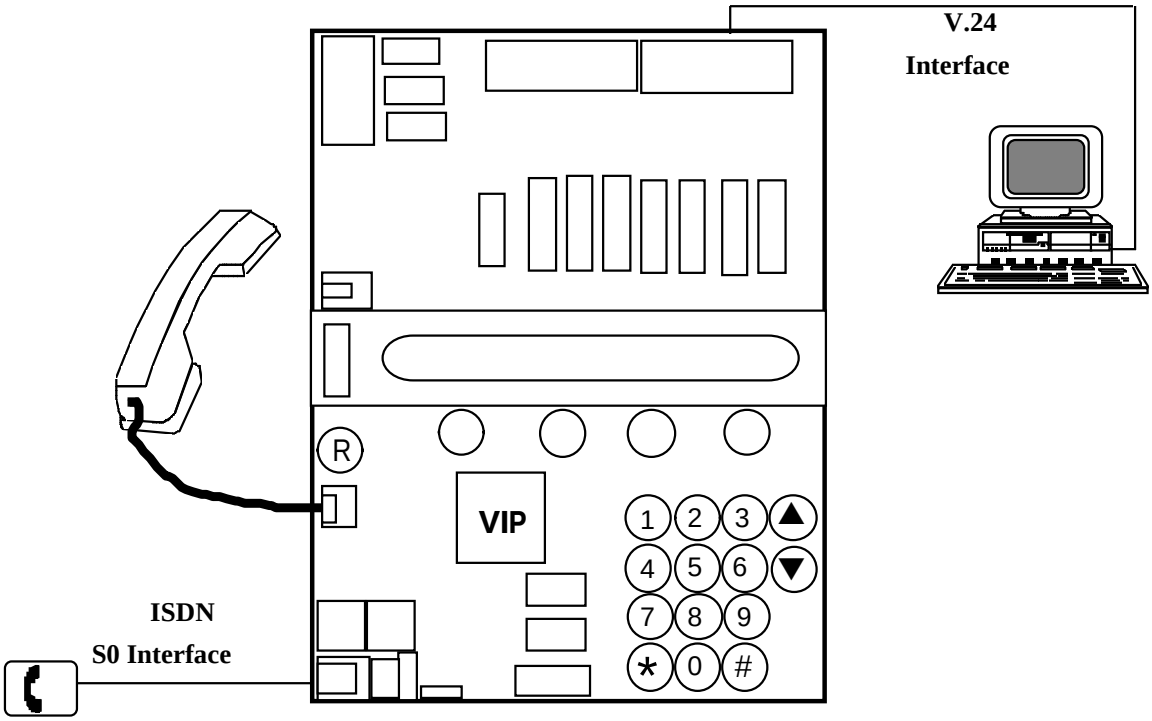

Figure 6-1: Evaluation System

6.2.1.1 Documents

The following VIP related documents are available or will be released soon:

- Jump Start specification
- ARM specification
- VIP evaluation board user manual
- VIP software development guide
- VIP library user guide

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6.2.2 PID - Board

Attributes:

- ARM7TDMI based
- kBytes fast SRAM
- up to 512 kByte of EPROM or FLASH, 8 or 16 bit wide debug monitor & remote debugger Interface
- Up to 16 Mbytes DRAM in two standard SIMM sockets
- Cache & memory management unit
- Two serial one parallel port
- Two PCMCIA slots
- Advanced Peripheral Bus (APB)
- Logic analyser port
- Part number: VY86PID-7TDMI

6.2.3 PIE - Board

Attributes:

- ARM7TDMI based
- Plug in compatible RS232 interface
- interface to logic analyser / custom add-ons
- 512 kBytes of program / data DRAM
- 128 kBytes EPROM w. debug monitor & self test firmware
- Part number: VY86PIE-7TDMI

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6.3 On-Chip Debug

The ARM debug architecture solves the debugging problem:

- ICE-like functionality via source level debugger interface
- Complete system independence so no porting is required
- Full system visibility, but doesn't use system resources
- Reuse boundary scan serial link for communications so no extra hardware required
- Can breakpoint ROM code, and has efficient watchpoint support
- Allows ROMless booting (take control after Reset)
- Complete support for the ANSI C library without any ROM or RAM allowing easy application development.

With the ARM7TDMI and the symbolic Debugger ARMsd the ICEbreaker can be used to have a high performance In Circuit debugger for ARM microprocessors. Therefore it is necessary to have the EmbeddedICE Interface (sometimes also called EmbeddedICE) which translates via a serial or parallel cable sent ARMsd commands in JTAG commands. For a configuration see the Figure 6-2.

EmbeddedICE is a JTAG based debugging environment for ARM microprocessors. EmbeddedICE provides the interface between ARM's source level symbolic debugger, ARMsd, and an ARM microprocessor embedded within any ASIC. The ARMsd debugger is available for PC compatible and Sun workstation platforms.

EmbeddedICE provides real time address and data dependent breakpoints, single stepping, full access and control of the ARM CPU, and full access to the ASIC system - full memory access (read and write) and full I/O system access (read and write). EmbeddedICE also allows the embedded microprocessor to access the host system peripherals, for instance screen display, keyboard input and disk drive storage.

Although EmbeddedICE provides a full complement of in Circuit Emulation facilities, it is one of the most cost effective ICE systems available for any microprocessor system.

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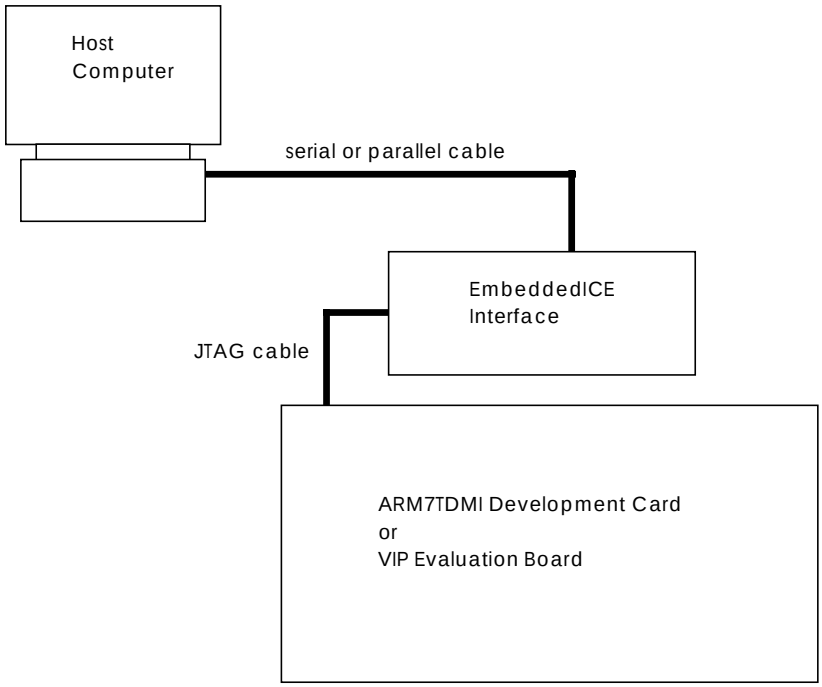

Figure 6-2: Embedded ICE Configuration

EmbeddedICE supports:

- Full symbolic source level debugging, for seamless visibility from user level application code through to on-chip hardware.
- address and / or data dependent hardware breakpoints, allow ROM breakpoints
- Infinite address dependent software breakpoints
- kBytes per second software download
- Serial and Parallel connections to host computer
- ROMless booting (for full ROMulator functionality)
- Full host system access including screen, keyboard and storage
- Reuse of boundary scan pins means no pin count overhead
- No target resources required (no use of system memory or other hardware)
- Part number: VY86BLKICE

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6.4 ISDN Software

VIP applications exist as one or more processes executing within a small multi-tasking operating system. The figure below shows the general architecture.

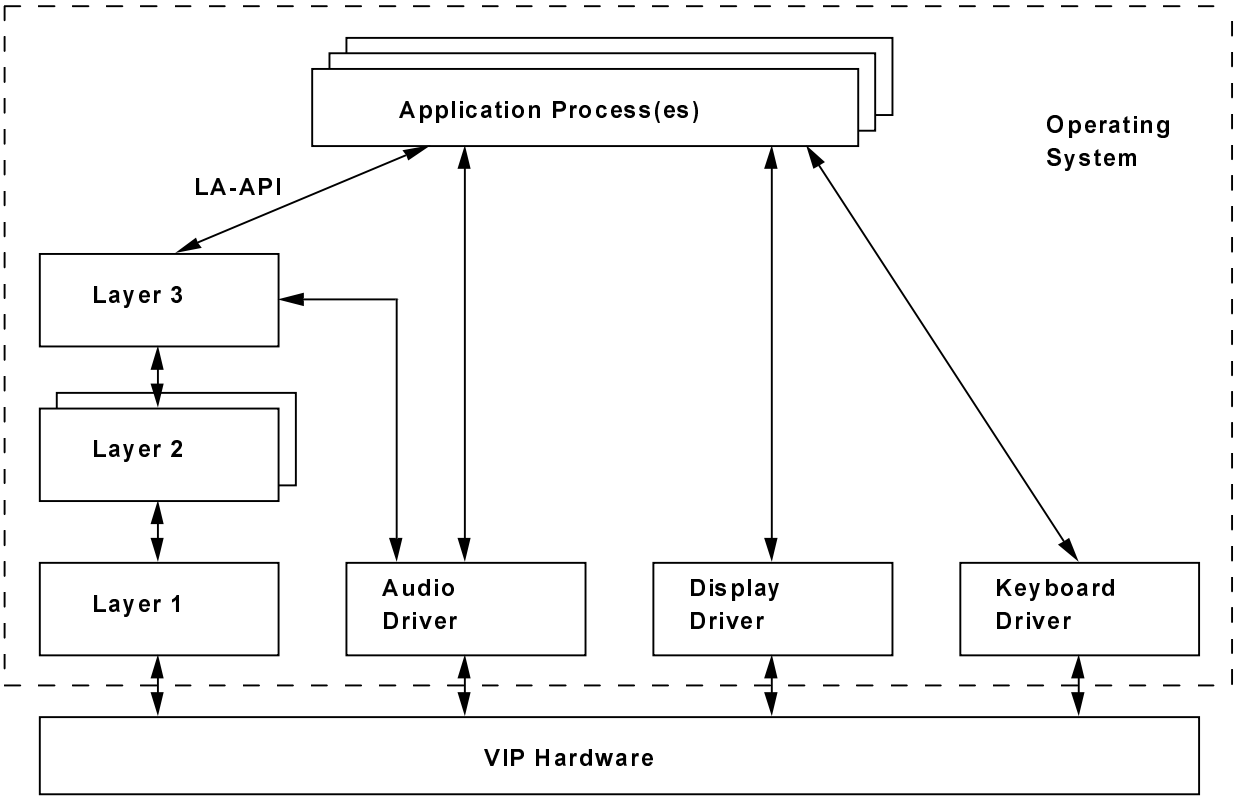

Figure 6-3: Software Model

Layer 1 Process
The Layer 1 Process is the D-channel interface to the VIP hardware. It includes the Layer 1 state machine and sending / receiving of D-channel data. The Layer 1 is implemented according to ITU recommendation I.430.

Layer 2 Processes
The Layer 2, consisting of two processes, one for TEI management the other for the state machine, implements the Link Access Procedure (LAPD) on the D-Channel. LAPD is responsible for conveying information (I frames) between layer 3 entities across the ISDN user-network interface. The layer 2 is compliant with ITU recommendation Q.921.

Layer 3 Process
The Layer 3 process is an implementation of the DSS-1 protocol. Its main function is to provide the call control part of the LA-API interface. It is also responsible for the connection / disconnection of B-channels to the programmed audio interface (handset).
The Layer 1-3 processes and operating system are part of the VIP library. All other processes including the audio, display and keyboard drivers belong to the application. A complete sample system including one application process and sample hardware drivers is included on the distribution disk.
Available together with the VIP are low level drivers for the hardware dependent parts of the VIP, e.g. to support load and store commands for the VIP internal register.

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7. TABLES AND FIGURES INDEX

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