General Description

The Multichannel Network Interface Controller for HDLC (MUNICH32, PEB 20320) is a multichannel protocol controller which handles up to 32 data channels of a full-duplex PCM highway. It performs layer-2 HDLC formatting/deformatting or transparent modes of the DMI protocol, passing on data to an external memory shared with one or more processors.

The MUNICH32 is compatible with the LAPD ISDN (Integrated Services Digital Network) protocol specified by CCITT as well as with HDLC, SDLC, LAPB DMI protocols. It provides any rate adaptation for time-slot transmission data rates from 64 kbit/s, 56 kbit/s down to 8 kbit/s as well as the concatenation of any time-slots to data channels supporting ISDN superchannels.

The MUNICH32 can be used in a wide area of communication applications, e.g. in gateways with fractional T1 interface, I/O multiplexers, central office switches or for the connection of a digital PBX to a host computer or as a central D-channel handler for 32 ISDN basic-access D-channels. Up to four MUNICH32s can be connected to one PCM highway to implement a controller for 128 D-channels.

The PEB 20320 operates in the temperature range 0 to 70 °C, the PEF 20320 in the range -40 to 85 °C.

Features

Serial Interface

- Up to 32 independent communication channels
- Serial multiplexed (full-duplex) input/output for 2048-, 4096-,1544- or 1536-kbit/s PCM highways

Dynamic Programmable Channel Allocation

- Compatible with T1/DS1 24-channel and CEPT 32-channel PCM byte format
- Concatenation of any, not necessarily consecutive, time-slot to superchannels independently for receive and transmit direction
- Support of H0, H11, H12 ISDN channels
- Subchannelling on each time-slot possible

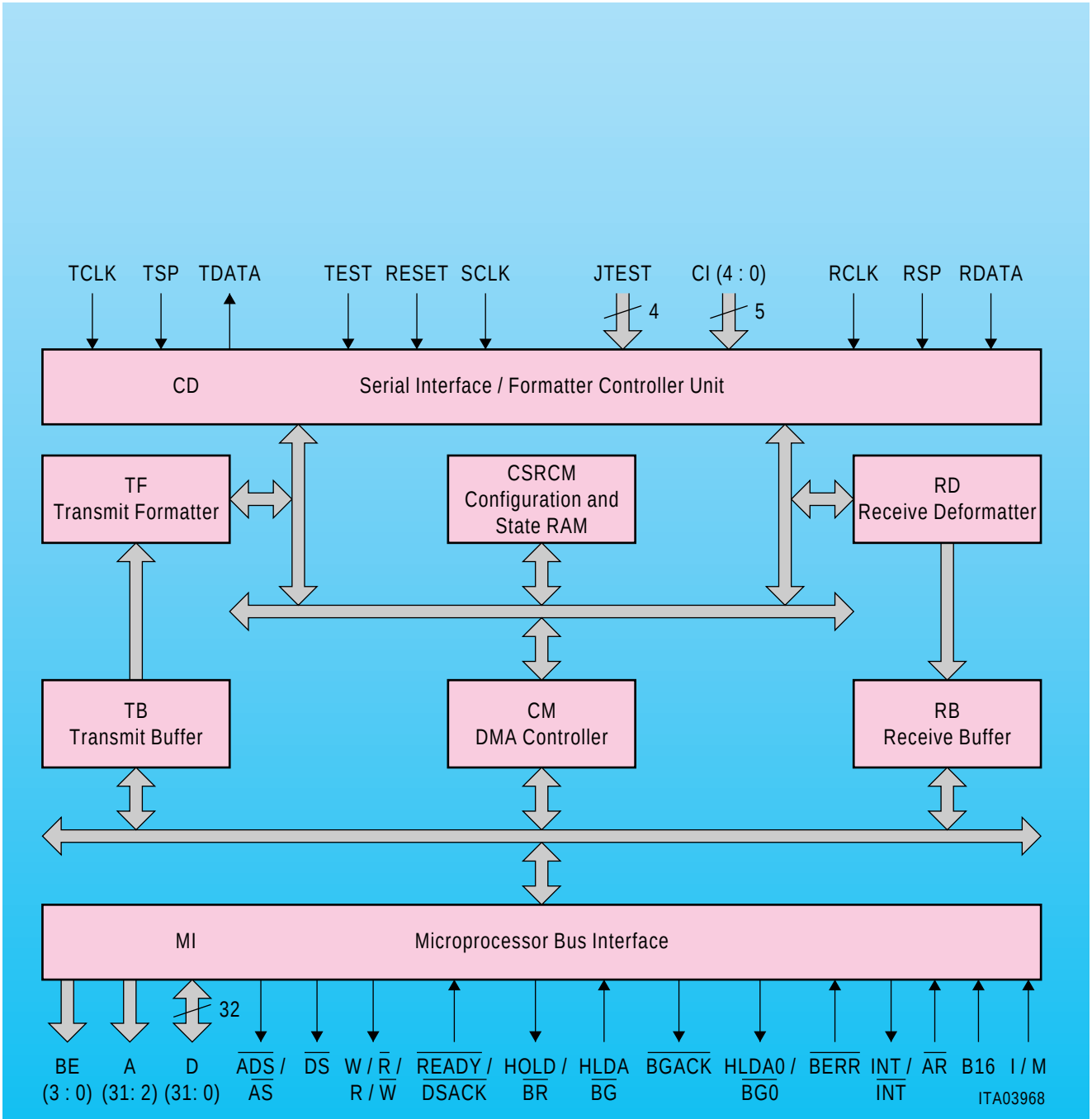
Type	Package
PEB 20320-H	P-MQFP-160-1 (SMD)
PEF 20320-H	P-MQFP-160-1 (SMD)

Bit Processor Functions (adjustable for each channel)

- Transparent mode or HDLC protocol selectable
- Automatic flag detection and transmission
- Shared opening and closing flags
- Zero-bit insertion and deletion
- Flag stuffing and flag adjustment for rate adaption
- Detection of interframe-time-fill change
- Channel inversion
- CRC generation and checking (16 or 32 bits)
- Transparent CRC option
- Error detection (abort, long frame, short frame, data under and overflow) as well as ABORT/IDLE generation and transmission
- V.110, X.30 80-bit framing, network data rate up to 38.4 kbit/s

Processor Interface

- On-chip 64 channel DMA controller with buffer chaining capability
- Compatible with Motorola 68020 processor family and Intel 32-bit processor (80386)
- 32-bit data and 32-bit address buses (4-GByte RAM addressable)
- Interrupt-circular buffer with variable size
- Maskable interrupts for each channel
- Burst cycles of up to 16 long words in the generic case are possible
- General on-chip receive and transmit data buffer; the buffer size is 256 bytes each
- Loop mode, complete loop as well as single channel loop
- JTAG-boundary scan test



Block Diagram