SIEMENS

Memory Time Switch Small (MTSS)

PEB 2046
PEF 2046

Preliminary Data

CMOS IC

Type	Ordering Code	Package
PEB 2046 C	Q67100-H6103	C-DIP-40
PEB 2046 N	Q67100-H6104	PL-CC-44 (SMD)
PEB 2046 P	Q67100-H6105	P-DIP-40
PEF 2046 C	Q67100-H6106	C-DIP-40
PEF 2046 N	Q67100-H6107	PL-CC-40 (SMD)
PEF 2046 P	Q67100-H6108	P-DIP-40

The Siemens memory time switch PEx 2046 is a monolithic CMOS circuit connecting any of 256 incoming PCM channels to any of 256 outgoing PCM channels. The on-chip connection memory is accessed via the 8 bit µP interface.

The PEx 2046 is fabricated using the advanced CMOS technology from Siemens and is mounted in a C-DIP-40, P-DIP-40 or a PL-CC-44 package. Inputs and outputs are TTL-compatible.

The PEB 2046 works with either a 8192 kHz clock or a 4096 kHz clock. Henceforth, the respective clock periods are referred to as t_{CP8} and t_{CP4}.

The bits of a time slot are numbered 0 through 7. Bit 0 of a time slot is the first bit to be received or transmitted by the MTSC, bit 7 the last.

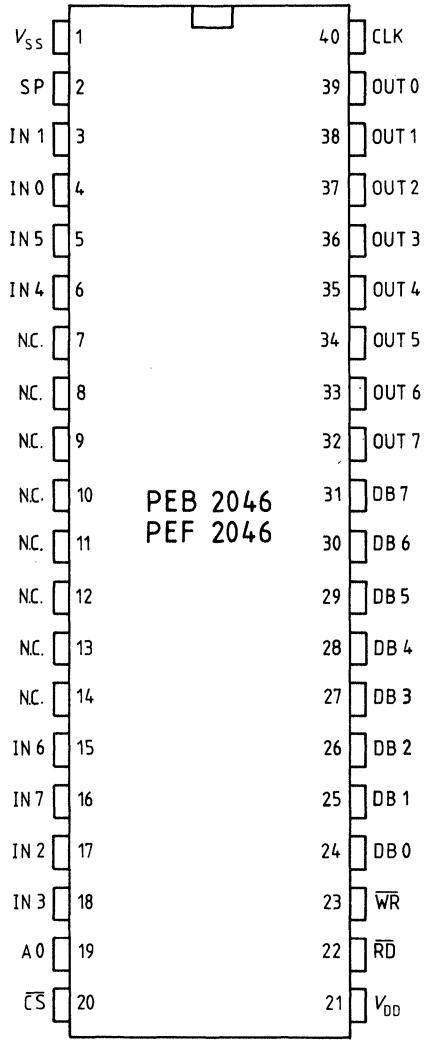
The components PEB 2046 and PEF 2046 are functionally identical. The difference between the two types lies in the temperature range. The PEB 2046 operates in the temperature range 0 to 70 °C, the PEF 2046 in the range −40 to +85 °C.

Features

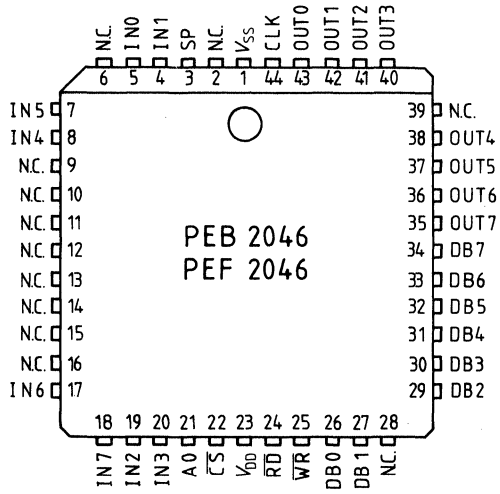
- Time/space switch for 2048 kbit/s PCM systems
- Switching of up to 256 incoming PCM channels to up to 256 outgoing PCM channels
- 8 input and 8 output PCM lines
- Configurable for a 4096 and 8192 kHz device clock
- Tristate function for further expansion and tandem operation
- 8 bit µP interface
- Single +5 V power supply
- Advanced low power CMOS technology

Pin Configuration
(top view)

P-DIP-40



PL-CC-44



Pin Definitions and Functions

P-DIP Pin No.	PL-CC Pin No.	Symbol	Input (I) Output (O)	Function
1	1	V_{SS}	I	**Ground** (0V)
2	3	SP	I	**Synchronization Pulse:** The PEx 2046 is synchronized relative to the PCM system via this line.
3	4	IN1	I	**PCM Input Ports:** Serial data is received at these lines at standard TTL levels.
4	5	IN0	I	
5	7	IN5	I	
6	8	IN4	I	
15	17	IN6	I	
16	18	IN7	I	
17	19	IN2	I	
18	20	IN3	I	
19	21	AO	I	**Address 0:** When high, the indirect register access mechanism is enabled. If A0 is logical 0 the mode and status registers can be written to and read respectively.
20	22	$\overline{CS}$	I	**Chip Select:** A low level selects the PEx 2046 for a register access operation.
21	23	V_{DD}	I	**Supply Voltage:** 5 V ± 5%.
22	24	$\overline{RD}$	I	**Read:** This signal indicates a read operation and is internally sampled only if $\overline{CS}$ is active. The MTSC puts data from the selected internal register on the data bus with the falling edge of $\overline{RD}$. $\overline{RD}$ is active low.
23	25	$\overline{WR}$	I	**Write:** This signal initiates a write operation. The $\overline{WR}$ input is internally sampled only if $\overline{CS}$ is active. In this case the MTSC loads an internal register with data from the data bus at the rising edge of $\overline{WR}$. $\overline{WR}$ is active low.
24	26	DB0	I/O	**Data Bus:** The data bus is used for communication between the MTSC and a processor.
25	27	DB1	I/O	
26	29	DB2	I/O	
27	30	DB3	I/O	
28	31	DB4	I/O	
29	32	DB5	I/O	
30	33	DB6	I/O	
31	34	DB7	I/O	

Pin Definitions and Functions (cont'd)

P-DIP Pin No.	PL-CC Pin No.	Symbol	Input (I) Output (O)	Function
32	35	OUT7	0	**PCM Output Port:** Serial data is sent by these lines at standard CMOS or TTL levels. These pins can be tristated.
33	36	OUT6	0	
34	37	OUT5	0	
35	38	OUT4	0	
36	40	OUT3	0	
37	41	OUT2	0	
38	42	OUT1	0	
39	43	OUT0	0	
40	44	CLK	I	**Clock:** 4096 or 8192 kHz device clock

Functional Description

The PEx 2046 is a memory time switch device. It can connect any of 256 PCM input channels to any of 256 output channels.

The input information of a complete frame is stored in the on-chip 2 kbit speech memory SM. **(see figure 1)**. The incoming 256 channels of 8 bits each are written in sequence into fixed positions in the SM. This is controlled by the input counter in the timing control block with a 8 kHz repetition rate.

For outputting, the connection memory (CM) is read in sequence. Each location in CM points to a location in the speech memory. The byte in this speech memory location is read into the current output time slot. The read access of the CM is controlled by the output counter which also resides in the timing control block.

Hence the CM needs to be programmed beforehand for the desired connection. The CM address corresponds to one particular output time slot and line number. The contents of this CM address points to a particular input time slot and line number (now resident in the SM).

Figure 1
Block Diagram of the PEx 2046

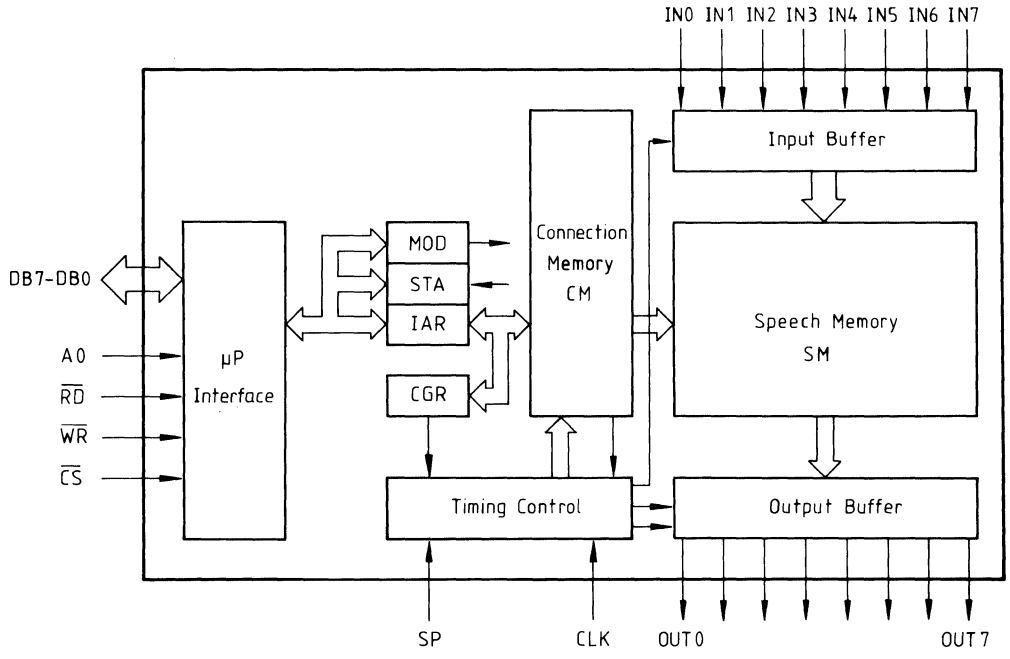
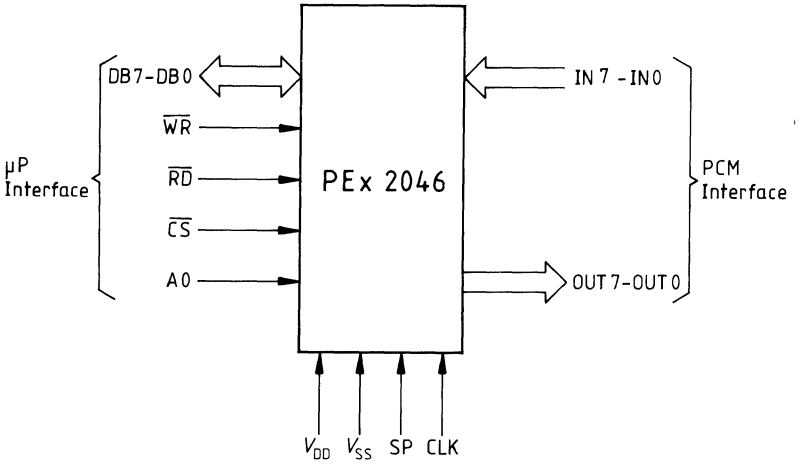


Figure 2
Functional Symbol for the Standard Configuration



Operational Description

Power Up

Upon power up the PEx 2046 is set to its initial state. The mode and configuration register bits are all set to logical 1. The status register **B**-bit is undefined, the **Z**-bit contains logical 0, the **R**-bit is undefined.

This state is also reached by pulling the $\overline{WR}$ and $\overline{RD}$ signals to logical 0 at the same time, (software reset). For the software the state of $\overline{CS}$ is of no significance.

Initialization Procedure

After power up a few internal signal and clocks need to be initialized. This is done with the initialization sequence. To give all signals and clocks a defined value the MTSC must encounter three falling and two rising edges of the SP signal. The resulting SP pulses may be of any length allowed in normal operation, the time interval between the two SP pulses may be of any length down to 250 nsec.

With all signals being defined, the CM needs to be reset. To do that a logical 0 is written into **MOD:RC. STA:B** is set. The resulting CM reset is finished after at most 250 µsec and is indicated by the status register **B**-bit being logical 0. Changing the pulse shaping factor N during CM reset may result in a CM reset time longer than 250 µs.

To prepare the PEx 2046 for programming the CM, the **RI**-bit in the mode register must be reset. Note that one mode register access can serve to reset both **RC** and **RI** bits as well as configuring to chip (i.e. selecting operating mode etc.).

Figure 3
Initializing the PEx 2046 for a 8192-kHz-Device Clock

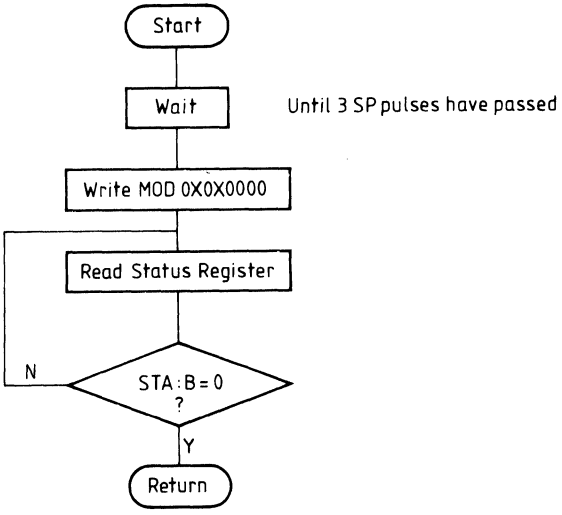
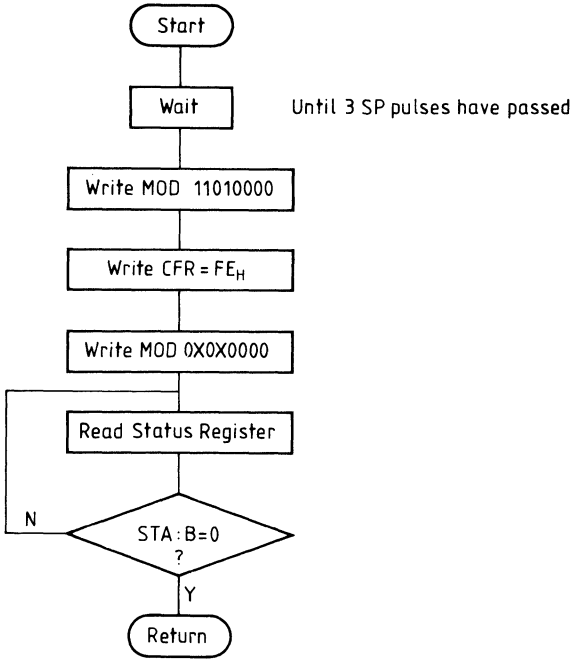


Figure 4
Initializing the PEx 2046 for a 4096-kHz-Device Clock



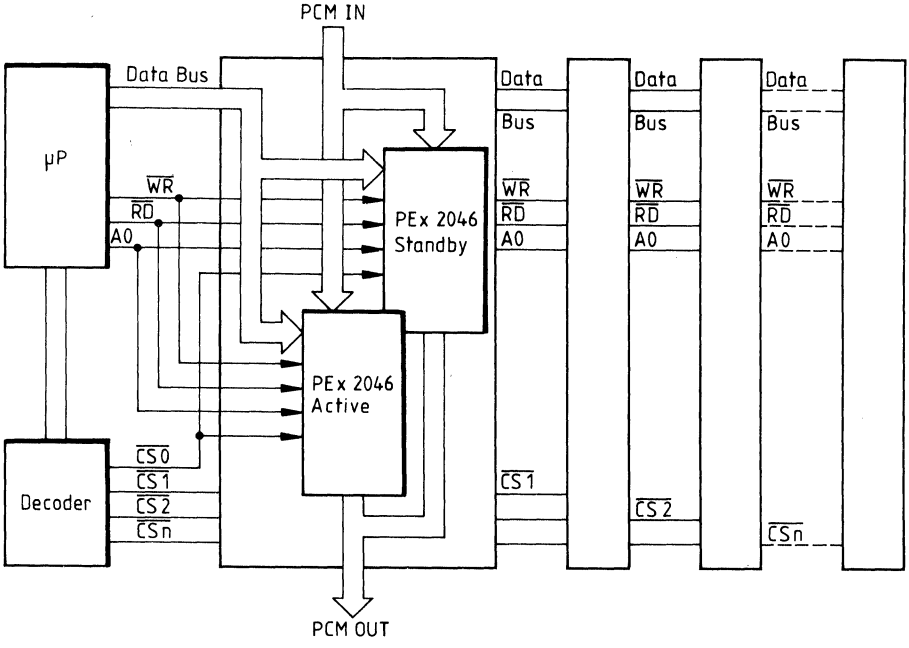
Operation with a 4096-kHz-Device Clock

In order for the MTSC to operate with a 4096-kHz-device clock the **CPS**-bit in the **CFR** register needs to be reset. This has to be done before the CM reset and needs up to 1.8 µs. Please keep in mind, **MOD:RI** has to be reset prior to performing an indirect register access. For a flow chart of this process refer to **figure 4.**

Standby Mode

With **MOD:SB** being logical 1 the PEx 2046 works as a backup device in redundant systems. It can be accessed via the µP interface and works internally like an active device. However, the outputs are high impedance. If the **SB**-bit is reset the outputs are switched to low impedance for the programmed active channels and this MTSC can take over from another device which has been recognized as being faulty. **See figure 5.**

Figure 5
Device Setup in Redundant Systems



Detailed Register Description

The following registers may be accessed:

Table 1
Addressing the Direct Registers

Address A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The chapters in this section cover the registers in detail.

Mode Register (MOD)

Access: write on address 0

DB 7							DB 0
RC	TE	RI	SB	MI1	MI0	MO1	MO0

Value after power up: FF_H

RC **R**eset **C**onnection memory; writing a zero to this bit causes the complete connection memory to be overwritten with 200_H (tristate). During this time **STA:B** is set. The maximum time for resetting the connection memory is 250 µs.

TE: **T**ristate **E**nable; this bit determines which tristating scheme is activated.

TE = 1: If the speech memory address written into the connection memory is S8 – S0 = 0, the output channel is tristated.

TE = 0: The S9 bit written into the connection memory is interpreted as a validity bit: S9 = 0 enables the programmed connection, S9 = 1 tristates the output.

Note: If TE = 1, time slot 0 of the logical input line 0 cannot be used for switching.

RI: **R**eset **I**ndirect access mechanism; setting this bit resets the indirect access mechanism. RI has to be cleared before writing/reading IAR after reset.

SB: **S**tand **B**y; by selecting SB = 1 all outputs are tristated. The connection memory works normally. The PEx 2045 can be activated immediately by resetting SB.

Table 2
Input and Output Pin Arrangement

Input Pin Arrangement

Pin-No. P-DIP	Pin-No. PL-CC	8x2 Mbit/s
3	4	IN 1
4	5	IN 0
5	7	IN 5
6	8	IN 4
15	17	IN 6
16	17	IN 7
17	19	IN 2
18	20	IN 3

Output Pin Arrangement

Pin-No. P-DIP	Pin-No. PL-CC	8x2 Mbit/s
32	35	OUT 7
33	36	OUT 6
34	37	OUT 5
35	38	OUT 4
36	40	OUT 3
37	41	OUT 2
38	42	OUT 1
39	43	OUT 0

Status Register (STA)

Access: read at address 0

DB 7							DB 0
B	Z	R	0	0	0	0	0

B **B**usy: the chip is busy resetting the connection memory (B = 1). B is undefined after power up and logical 0 after the device initialization.

Note: The maximum time for resetting the connection memory is 250 µs.

Z incomplete instruction; a three byte indirect instruction is not completed (Z = 1). Z is 0 after power up.

Note: Z is reset and the indirect access is cancelled by setting **MOD:RI** or resetting **MOD:RC**

R initialization **R**equest. The connection memory has to be reset due to loss of data (R = 1). The R bit is set after power failure or inappropriate clocking and reset when the connection memory reset is finished. R is undefined after power up and logical 0 after the device initialization.

Indirect Access Register (IAR)

(Read or Write Operation with Address A0 = 1)

An indirect access is performed by reading/writing three consecutive bytes (first byte = control byte, second byte = data byte, third byte = address byte) to/from IAR. The structure is shown in **table 3.**

Table 3

The 3 Bytes of the Indirect Access

Bit 7							Bit 0	
0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The control byte bits K1, K0, C1 and C0 together with the address byte determine the type of access being performed according to **table 4.**

Table 4

Encoding the Different Types of Indirect Accesses

K1	K0	C1	C0	Address Byte	Type of Access	
0	0	D9	D8	CM-Address	Read	CM
1	0	D9	D8	CM-Address	Write	CM
0	1	D9	D8	CM-Address	Write	CM
1	1	0	0	FE_H	Write	CFR
1	1	0	1	FE_H	Read	CFR

Connection Memory Access

For a connection memory access the control byte bits C1 and C0 contain the data bits D9 and D8, respectively. D9 is the validity bit which together with D8 and the data byte D7-D0 is written to the CM address IA7-IA0.

The function of the validity bit is controlled by **STA:TE**. D8-D0 and IA7-IA0 contain the information for the logical line and time-slot numbers of the programmed connection, D8-D0 for the inputs, IA7-IA0 for the outputs. **Table 5** shows the programming of these bits.

Standard Configuration

Table 5
Time Slot and Line Programming

2 Mbit/s input lines	Bit	D3	to	D0	Logical line number
	Bit	D8	to	D4	Time slot number
	Bit	D9			Valididy bit
2 Mbit/s output lines	Bit	IA2	to	IA0	Line number
	Bit	IA7	to	IA0	Time slot number

Configuration Register Access (CFR)

Access: read or write at indirect address FE_H

For a read access the bit 0 of the control byte must be set to logical 1 and for a write access to logical 0.

Value after power up or software reset: FF_H

DB 7							DB 0
1	1	1	1	1	1	1	CPS

CPS.. **C**lock **P**eriod **S**elect: device clock is set to 8192 kHz (logical 1) or 4096 kHz (logical 0)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEB 2046	T_A	0 to 70	°C
Storage temperature PEB 2046	T_{stg}	−65 to 125	°C
Ambient temperature under bias PEF 2046	T_A	−40 to 85	°C
Storage temperature PEF 2046	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V

DC Characteristics

Ambient temperature under bias range; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V	
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2\ mA$
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} −0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$
Operational power supply current	I_{CC}		10	mA	$V_{DD} = 5$ V, inputs at 0 V or V_{DD}, no output loads.
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	$0\ V < V_{IN} < V_{DD}$ to 0 V $0\ V < V_{OUT} < V_{DD}$ to 0 V

Capacitances

$T_A = 25\,°C$, $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

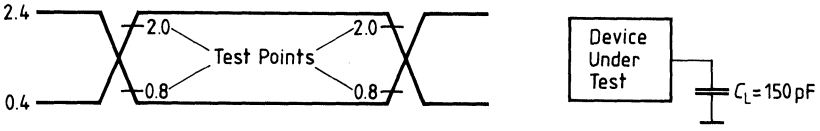
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
I/O capacitance	C_{IO}		20	pF
Output capacitance	C_{OUT}		15	pF

AC Characteristics

Ambient temperature under bias range, $V_{DD} = 5\ V \pm 5\%$

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

Figure 5
I/O Waveform for AC Tests



µP Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address stable before $\overline{RD}$	t_{AR}	0		ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ width	t_{RR}	90		ns
$\overline{RD}$ to data valid	t_{RD}		90	ns
Address stable to data valid	t_{AD}		90	ns
Data float after $\overline{RD}$	t_{DF}	5	25	ns
Read cycle time	t_{RCY}	160		ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold time	t_{WA}	0		ns
$\overline{WR}$ width	t_{WW}	60		ns
Data setup time	t_{DW}	5		ns
Data hold time	t_{WD}	15		ns
Write cycle time	t_{WCY}	160		ns

Figure 6
µP Read Cycle

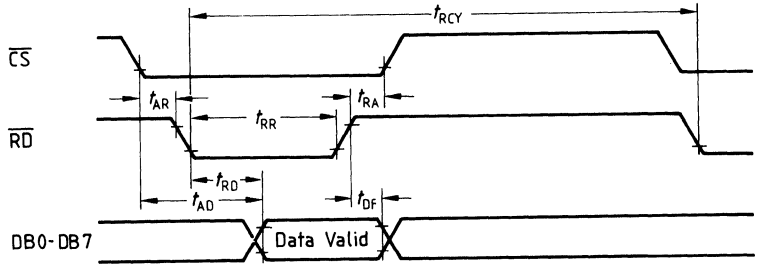
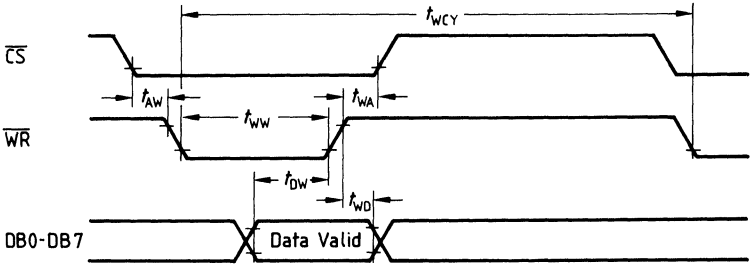


Figure 7
µP Write Cycle



PCM Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCM input setup	t_S	0		ns
PCM input hold	t_H	30		ns
PEB 2046 output delay	t_D		45	ns
PEF 2046 output delay	t_D		50	ns

Clock and Synchronization Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock period 8 MHz high	$t_{CP8\,H}$	40		ns
Clock period 8 MHz low	$t_{CP8\,L}$	48		ns
Clock period 8 MHz	t_{CP8}	120		ns
Synchronization pulse setup 8 MHz	t_{SS8}	10	$t_{CP8}-20$	ns
Synchronization pulse delay 8 MHz	t_{SH8}	0	$t_{CP8}-20$	ns
Clock period 4 MHz high	$t_{CP4\,H}$	90		ns
Clock period 4 MHz low	$t_{CP4\,L}$	90		ns
Clock period 4 MHz	t_{CP4}	240		ns
Synchronization pulse setup 4 MHz	t_{SS4}	10	$t_{CP4}-30$	ns
Synchronization pulse delay 4 MHz	t_{SH4}	30	$t_{CP4}-10$	ns

Figure 8
PCM Line Timing with a 8-MHz-Device Clock

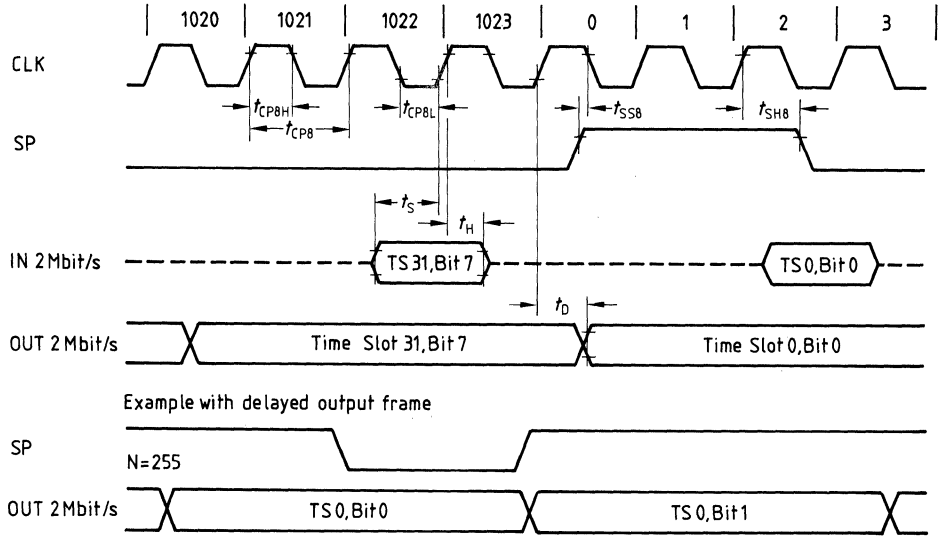
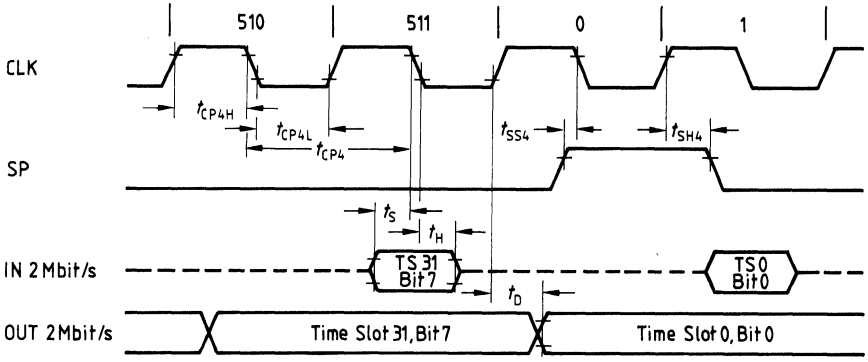


Figure 9
PCM Line Timing with a 4-MHz Device Clock



Busy Time

Table 6
Busy Time

Operation	Max. Values	Unit
Indirect register access	900	ns
Connection memory reset	250	µs