SIEMENS

ISDN Communication Controller (ICC) PEB 2070

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2070-C	Q67100-H8328	C-DIP-24
PEB 2070-N	Q67100-H8394	PL-CC-28 (SMD)
PEB 2070-P	Q67100-H2953	P-DIP-24

The transmission and protocol functions in an ISDN basic access can all be implemented using the CMOS circuits of the ISDN Oriented Modular (IOM® -1) chip set. While three chips, the S Bus interface Circuit SBC (PEB 2080), the ISDN Echo Cancellation circuit IEC (PEB 2090) and the ISDN Burst Controller IBC (PEB 2095) perform the transmission functions in different applications (S- and U-Interface), the ISDN Communication Controller ICC (PEB 2070) acts as the D-channel-link-access protocol controller.

The IOM architecture makes possible a wide range of configurations for the basic access, using the basic devices. These configurations essentially differ in the implementation of the layer-1 OSI functions, while the layer-2 functions are provided by the ICC for all configurations.

In addition to that, the PEB 2070 provides the interface to B-channel sources in the terminal and to a peripheral board controller (PEB 2050, 51, 52 etc.) at the exchange.

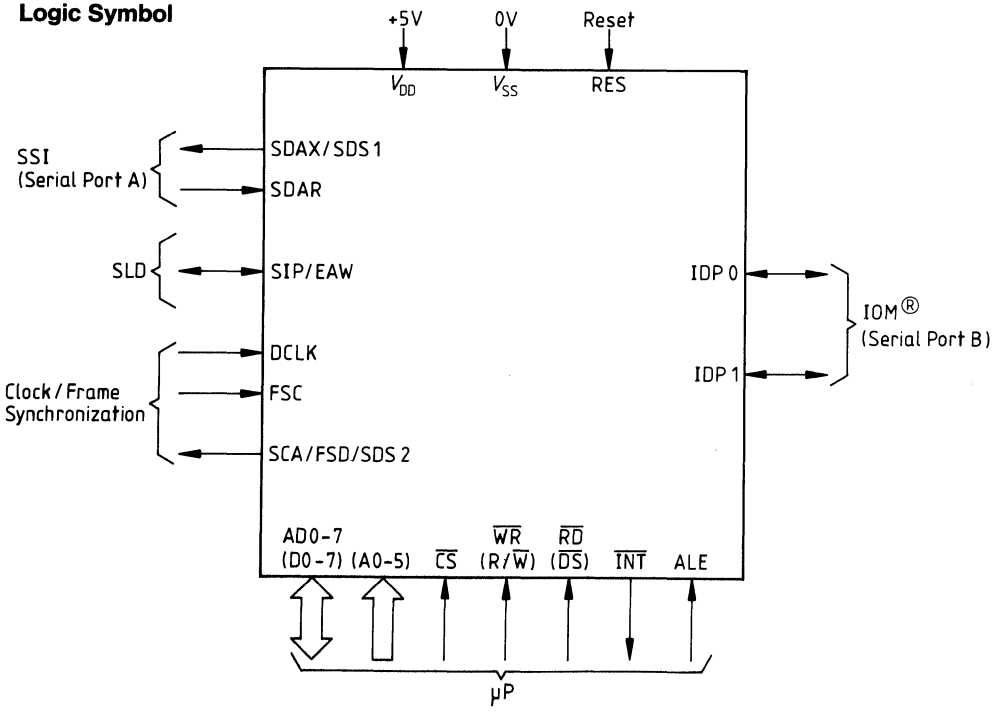
The HDLC packets of the ISDN D channel are handled by the ICC which transfers them to the associated microcontroller. The ICC has on-chip buffer memories (64 bytes per direction) for the temporary storage of data packets. Because of the overlapping I/O operations the maximum length of the D-channel packets is not limited. In one of its operating modes the device offers high level support of layer-2 functions of the LAPD protocol.

A side from ISDN applications, the ICC can be used as a general purpose communication controller in all applications calling for LAPD, LAPB or other HDLC/SDLC based protocols.

Features

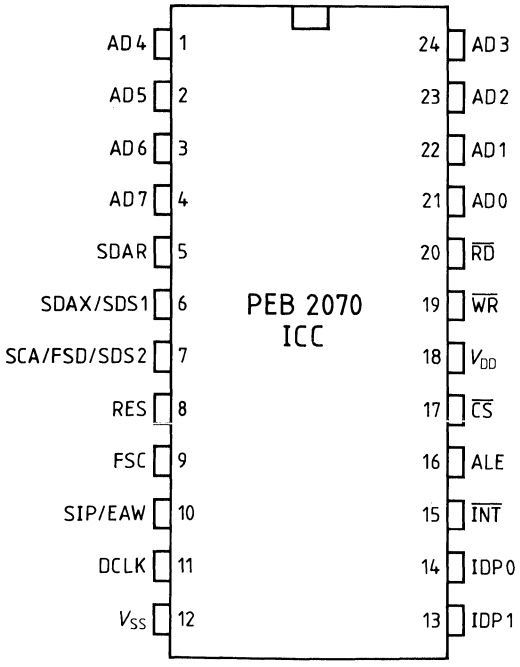
- Support of LAPD protocol
- Different types of operating modes for increased flexibility
- FIFO buffer (2 x 64 bytes) for efficient transfer of data packets
- Serial Interfaces: IOM-1, SLD, SSI
  IOM-2
- General purpose HDLC communication interface
- Implementation of IOM-1/IOM-2 monitor and C/I channel protocol to control layer-1 and peripheral devices
- D-channel access with contention resolution mechanism
- µP access to B channels and intercommunication channels
- B-channel switching
- Watchdog timer
- Test loops
- Advanced CMOS technology
- Low power consumption: active : 17 mW (IOM-2)
  : 8 mW (IOM-1)
  standby : 3 mW

Logic Symbol

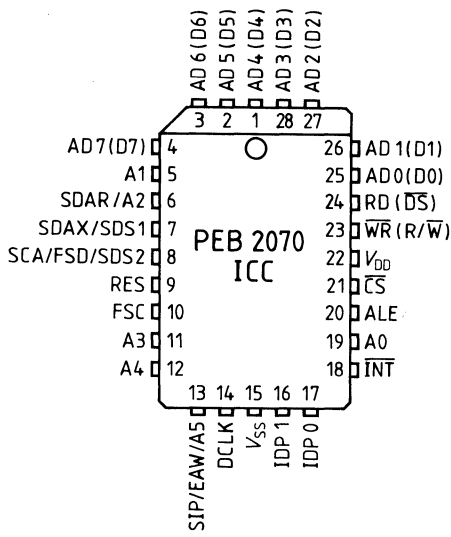


Pin Configuration
(top view)

P-DIP-24



PL-CC-28



Pin Definitions and Functions

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
21	25	AD0/D0	I/O	**Multiplexed Bus Mode:** Address/Data bus. Transfers addresses from the µP system to the ICC and data between the µP system and the ICC. **Non Multiplexed Bus Mode:** Data bus. Transfers data between the µP system and the ICC.
22	26	AD1/D1	I/O	
23	27	AD2/D2	I/O	
24	28	AD3/D3	I/O	
1	1	AD4/D4	I/O	
2	2	AD5/D5	I/O	
3	3	AD6/D6	I/O	
4	4	AD7/D7	I/O	
17	21	$\overline{CS}$	I	**Chip Select.** A "Low" on this line selects the ICC for a read/write operation.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
–	23	R/$\overline{W}$	I	**Read/Write.** When "High", identifies a vaild µP access as a read operation. When "Low", identifies a valid µP access as a write operation (Motorola bus mode).
19	23	$\overline{WR}$	I	Write. This signal indicates a write operation (Siemens/Intel bus mode).
–	24	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
20	24	$\overline{RD}$	I	Read. This signal indicates a read operation (Siemens/Intel bus mode).
15	18	$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the ICC request an interrupt. It is an open drain output.
16	20	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address bus (Multiplexed bus type only).
7	8	SCA	O	**Serial Clock Port A,** IOM-1 timimg mode. A 128-kHz-data clock signal for serial port A (SSI).
7	8	FSD	O	**Frame Sync Delayed,** IOM-1 timing mode 1. An 8-kHz-synchronization signal, delayed by 1/8 of a frame, for IOM-1 is supplied. In this mode a minimal round-trip delay for B1 and B2 channels is guaranteed.
7	8	SDS2	O	**Serial Data Strobe 2,** IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 takes on the function of SDS2 until a write access to SPCR is made.
8	9	RES	I/O	**Reset.** A "High" on this input forces the ICC into reset state. The minimum pulse length is four clock periods. If the terminal specific functions are enabled, the ICC may also supply a reset signal.

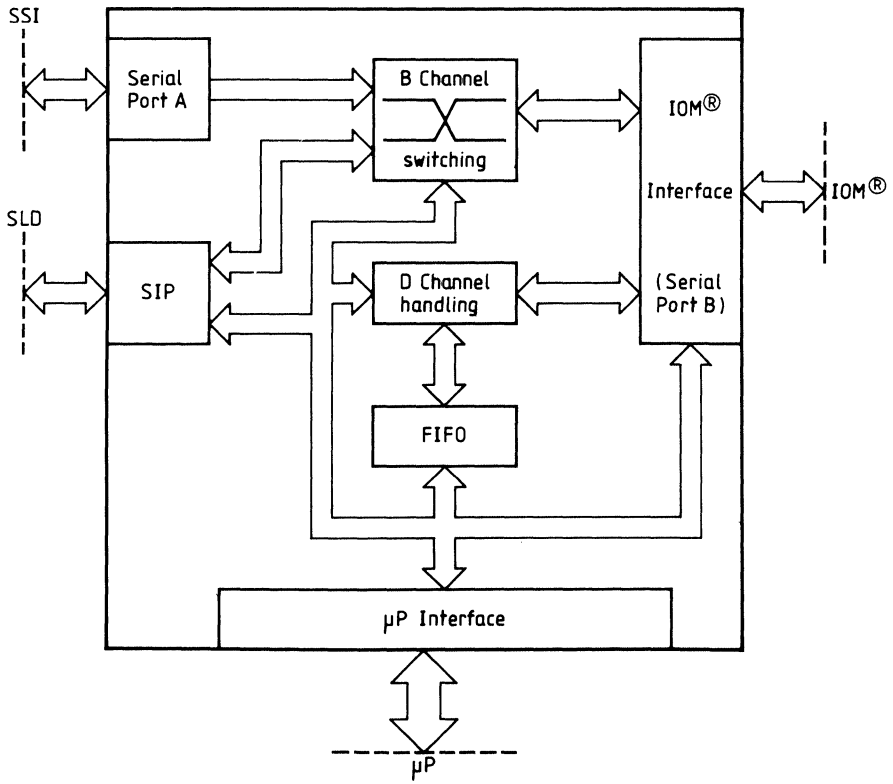
Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
9	10	FSC	I	**Frame Sync.** Input synchronization signal. IOM-2 mode: Indicates the beginning of IOM frame. IOM-2 mode: Indicates the beginning of IOM and, if TSF = 0, frame (timing mode 0). Indicates the beginning of SLD frame (timing mode 1). HDLC mode: Strobe signal of programmable polarity
11	14	DCLK	I	**Data Clock.** IOM modes: Clock of frequency equal to twice the data rate on the IOM interface. HDLC mode: Clock of frequency equal to the data rate on serial port B.
	19	A0	I	**Address** bit 0 (Non-multiplexed bus type).
	5	A1	I	**Address** bit 1 (Non-multiplexed bus type).
	6	A2	I	**Address** bit 2 (Non-multiplexed bus type).
6	6	SDAR	I	**Serial Data Port Receive.** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open-drain/ open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
	11	A3	I	**Address** bit 3 (Non-multiplexed bus type).
	12	A4	I	**Address** bit 4 (Non-multiplexed bus type).
	13	A5	I	**Address** bit 5 (Non-multiplexed bus type).
10	13	SIP	I/O	SLD Interface Port, IOM-1 mode. This line transmits and receives serial data at standard TTL or CMOS levels.
10	13	EAW	I	**External Awake** (terminal specific function). If a falling edge on this input is detected, the ICC generates an interrupt and, if enabled, a reset pulse.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
6	7	SDAX	0	**Serial Data Port A** transmit, IOM-1 mode. Transmit data is shifted out via this pin at standard TTL or CMOS levels.
6	7	SDS1	0	**Serial Data Strobe** 1, IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SDAX/SDS1 takes on the function of SDS1 until a write access to SPCR is made.
12	15	V_{SS}	–	Ground (0 V)
18	22	V_{DD}	–	Power supply (5 V ± 5%)
14 13	17 16	IDP0 IDP1	I/O I/O	**IOM Data Port 0, 1**

Block Diagram



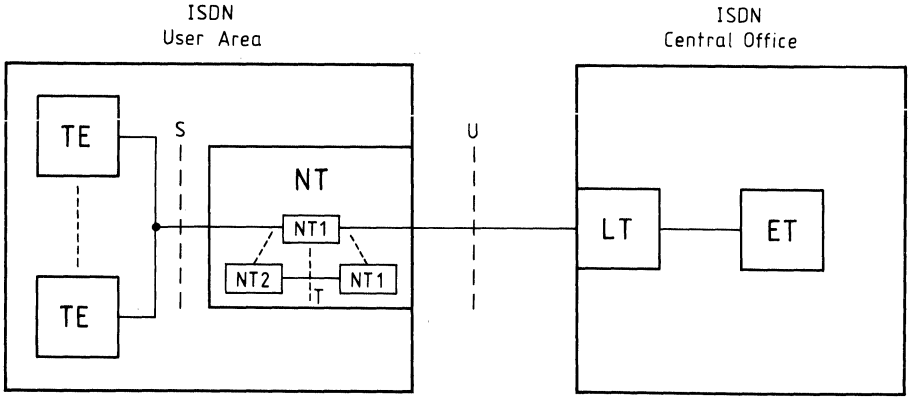
System Integration

ISDN Applications

The reference model for the ISDN basic access according to CCITT I series recommendations consists of

- an exchange and trunk line termination in the central office (ET, LT)
- a remote network termination in the user area (NT)
- a two-wire loop (U interface) between NT and LT
- a four-wire link (S interface) which connects subscriber terminals and the NT in the user area as depicted in **figure 1.**

Figure 1
ISDN Subscriber Basic Access Architecture

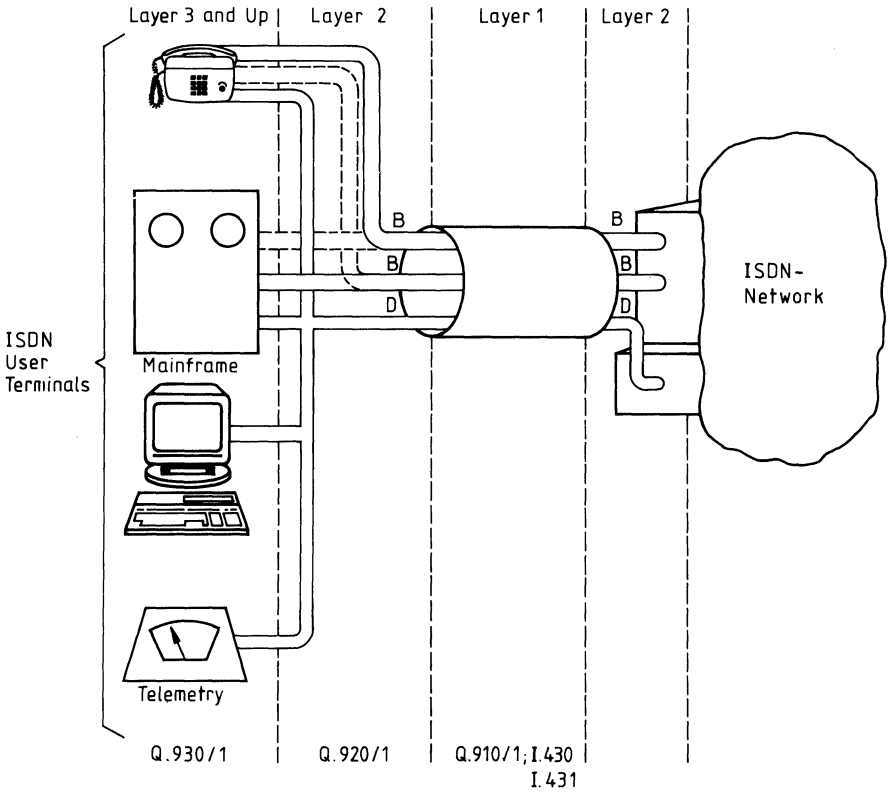


The NT equipment serves as a converter between the U interface at the exchange and the S interface at the subscriber premises. The NT may consist of either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. The NT1 is a direct transformation between layer-1 of S and layer-1 of U. NT2 may include higher level functions like multiplexing and switching as in a PBX.

In terms of channels the ISDN access consists of:

- a number of 64 kbit/s bearer channels (n x B)
  e.g. n = 2 for basic rate ISDN access
  n = 30 or 23 for primary rate ISDN access;
- and a signaling channel (D), either 16 (basic rate) or 64 (primary rate) kbit/s.

Figure 2
ISDN Basic Access Channel Structure



The B channels are used for end-to-end circuit switched digital connections between communicating stations.

The D channel is used to carry signaling and data via protocols defined by the CCITT. These protocols cover the network services layers of the open system interconnection model (layers 1-3). At layer-2, the data link layer, an HDLC type protocol is employed, the Link Access Procedure on the D channel LAPD (CCITT Rec. Q.920/1).

The ISDN communication controller PEB 2070 can be used in all ISDN applications involving establishment and maintenance of a data link connection in either the D channel or B channel. It also provides the interface to layer-1 functions controlled via the IOM which links the ICC to any transceiver or peripheral device. Depending on the interface mode, the ICC supports three serial interfaces and offers switching functions and µP access to voice/data channels.

The applications comprise:

- Use as a signaling controller for the D channel
- Access to the D channel for data transmission
- Source/sink for secured B channel data

and the target equipment include:

- ISDN terminal
- ISDN PBX (NT2) and Central Office (ET) line card
- ISDN packet switches
- "Intelligent" NT1.

Terminal Applications

The concept of the ISDN basic access is based on two circuit-switched 64-kbit/s B channels and a message oriented 16-kbit/s D channel for packetized data, signaling and telemetry information.

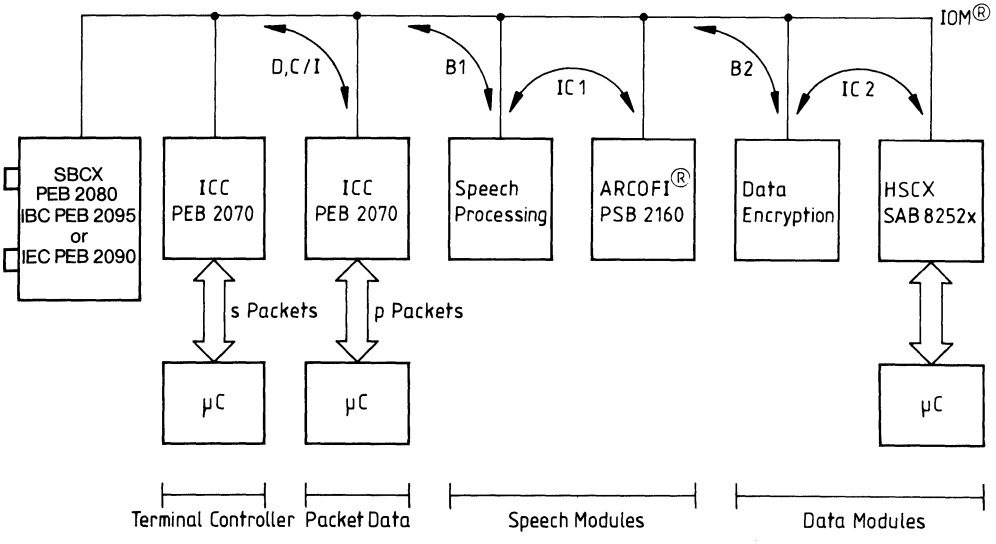
Figure 3 shows an example of an integrated **multifunctional ISDN** terminal using the ICC. The transceiver provides the layer-1 connection to the transmission line, either an S or a U interface, and is connected to the ICC and other, peripheral modules via the IOM interface.

The D channel, containing signaling data and packet switched data, is processed by the ICC LAPD controller and routed via a parallel µP interface to the terminal processor. The high level support of the LAPD protocol which is implemented by the ICC allows the use of a low cost processor in cost sensitive applications.

The IOM interface is used to connect diverse voice/data application modules:

- sources/sinks for the D channel
- sources/sinks for the B1 and B2 channels.

Figure 3
Example of ISDN Voice/Data Terminal



Different D channel services (for different SAPI's) can be simply implemented by connecting an additional ICC in parallel to the first one, for instance for transmitting p-packets in the D channel.

Up to eight ICCs may thus be connected to the D and C/I (Command/Indication) channels. The ICCs handle contention autonomously.

Data transfers between the terminal controller and the different modules are done with the help of the IOM monitor channel protocol. Each voice/data module can be accessed by an individual address. The same protocol enables the control of terminal modules that do not have an associated microcontroller (such as the Audio Ringing Codec Filter ARCOFI®: PSB 2160) and the programming of intercommunication inside the terminal. Two intercommunication channels IC1 and IC2 allow a 2 x 64 kbit/s transfer rate between voice/data modules.

In the example above **(figure 3)**, one ICC is used for data packets in the D channel. A voice processor is connected to a programmable digital signal processing codec filter via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication, B2 for data communication.

The ICC ensures full upward compatibility with IOM-1 devices. It provides the additional strobe, clock and data lines for connecting standard combos or data devices via IOM, or serial SLD and SSI interfaces. The strobe signals and the switching of B channels is programmable.

Line Card Applications

An example of the use of the ICC on an **ISDN LT + ET line card** (decentralized architecture) is shown in **figure 4.**

The transceivers (ISDN Echo Cancellation Circuit IEC: PEB 2090) are connected to an Extended PCM interface Controller (EPIC PEB 2055) via an IOM interface.

This interface carries the control and data for up to eight subscribers using time division multiplexing. The ICCs are connected in parallel on IOM, one ICC per subscriber.

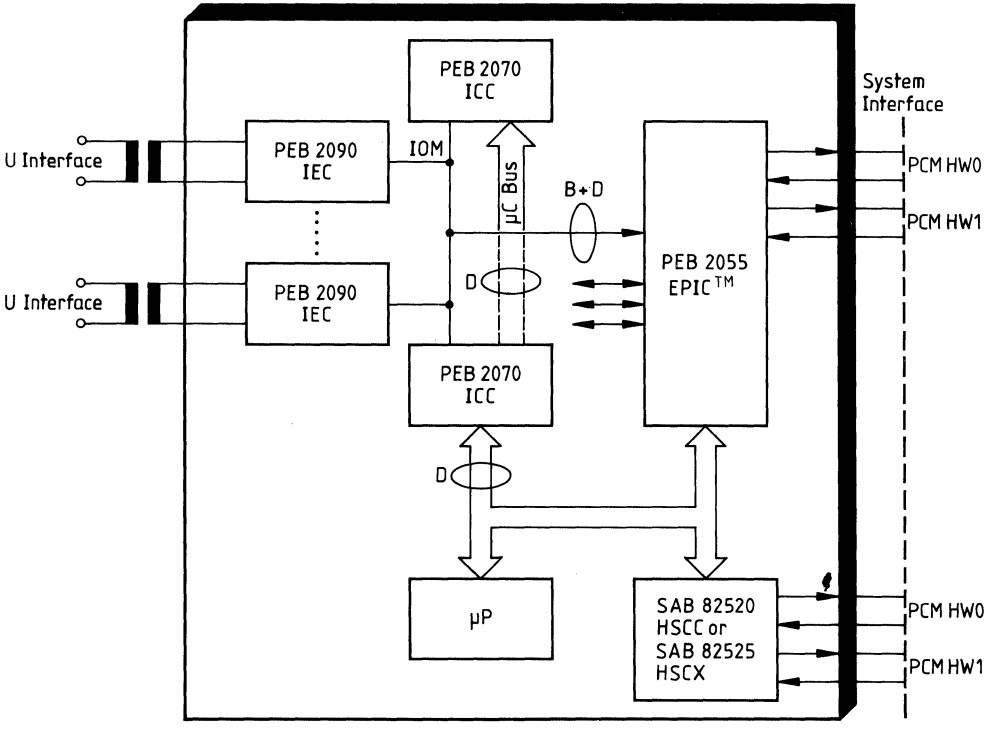
The EPIC performs dynamic B and D channel assignment on the PCM highways. Since this component supports four IOM interfaces, up to 32 subscribers may be accommodated.

Other Applications

If programmed in non-ISDN mode, the ICC serial port B operates as an HDLC communication link without IOM frame structure. This allows the use of the ICC as a general purpose communication controller. The valid HDLC data is marked by a strobe signal on serial port B. Examples of the use of the ICC are: X.25 packet controllers, terminal adaptors, and packet transmission e.g. in primary rate/DMI systems.

Figure 4

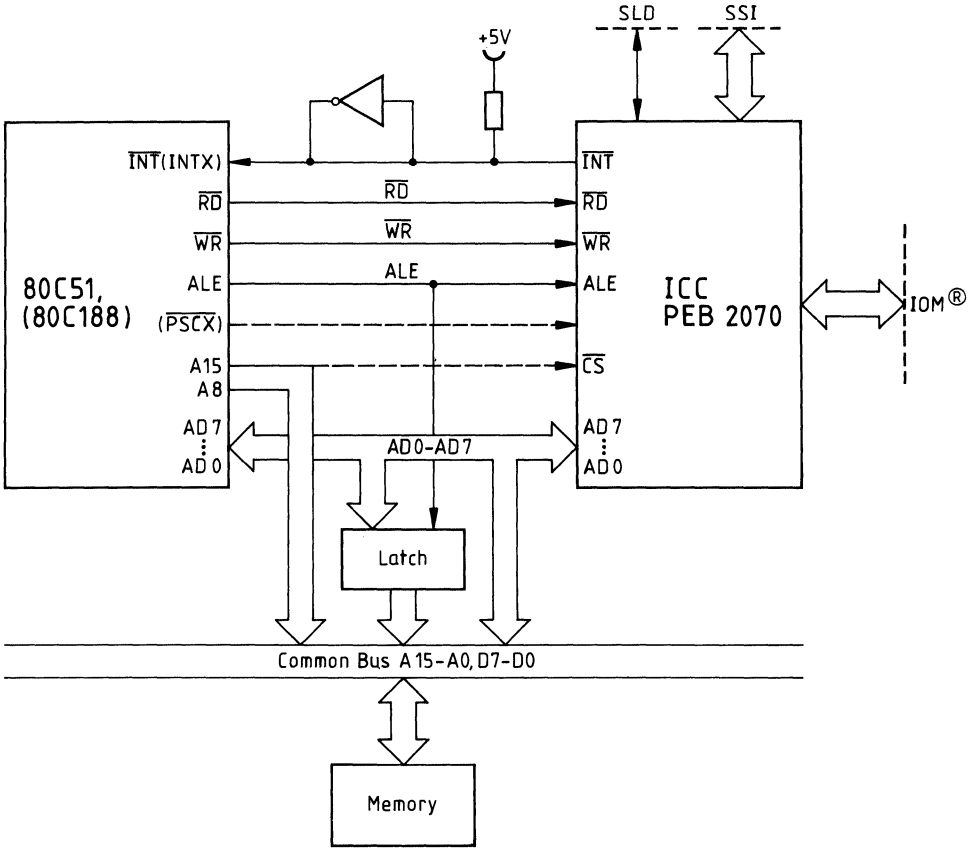
ISDN Line Card Implementation



Microprocessor Environment

The ICC is especially suitable for cost-sensitive applications with single-chip microcontrollers (e.g. 8048, 8031, 8051). However, due to its programmable micro interface and non-critical bus timing, it fits perfectly into almost any 8-bit microprocessor system environment. The microcontroller interface can be selected to be either of the Motorola type (with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$), of the Siemens/Intel non-multiplexed bus type (with control signals CS, WR, RD) or of the Siemens/Intel multiplexed address/data bus type ($\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE).

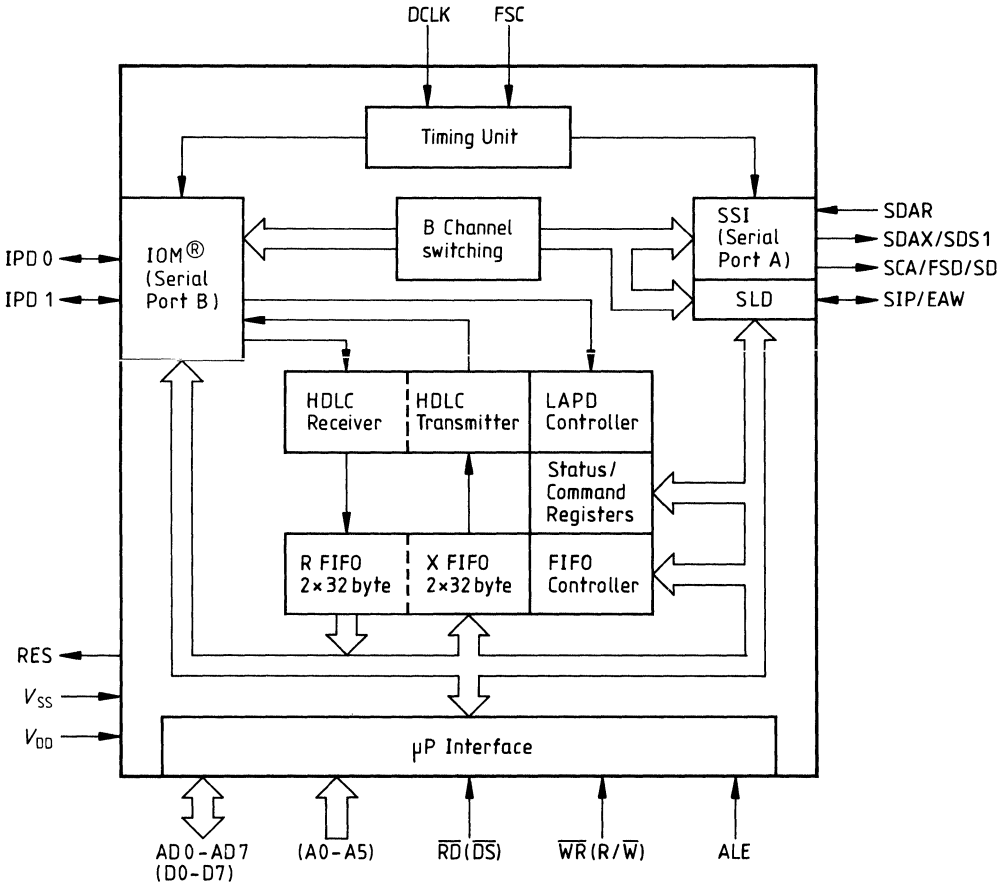
Figure 5
Example of ICC Microcontroller Environment



Functional Description

General Functions and Device Architecture

Figure 6
Architecture of the ICC



The functional block diagram in **figure 6** shows the ICC to consist of:

- serial interface logic for the IOM, SLD and SSI interfaces with B channel switching capabilities
- logic necessery to handle the D channel messages (layer 2).

The latter consists of an HDLC receiver and an HDLC transmitter together with 64-byte deep FIFO's for efficient transfer of the messages to/from the user's CPU.

In a special HDLC controller operating mode, the auto mode, the ICC processes protocol handshakes (I- and S-frames) of the LAPD (Link Access Procedure on the D channel) autonomously.

Control and monitor functions as well as data transfers between the user's CPU and the D and B channels are performed by the 8-bit parallel µP interface logic.

The IOM interface logic allows interaction between layer-1 and layer-2 functions. It implements D-channel collision resolution for connecting other layer-2 devices to the IOM interface, and the C/I and monitor channel protocols (IOM-1/IOM-2) to control peripheral devices.

The timing unit is responsible for the system clock and frame synchronization.

Serial Interface Modes

The PEB 2070 can be used in different modes of operation:

- IOM-1 Mode
- IOM-2 Mode
- HDLC Controller Mode.

These modes are selected via bit IMS (Interface Mode Select) in ADF2 register and bits DIM 2-0 (Digital Interface Mode) in MODE register. **See table 1.**

Table 1

Interface Modes

IMS	DIM2	Mode
0	0	IOM-1 Mode
	1	HDLC Mode
1	X	IOM-2 Mode

IOM 1 Mode (IMS = 0, DIM2 = 0)

Serial Port B is used as the IOM-1 interface, which connects the ICC to a layer-1 component.

The HDLC controller is always connected to the D channel of IOM-1 interface.

Two additional serial interfaces are available in this mode, the Synchronous Serial Interface SSI (serial port A) and the Subscriber Line Datalink (SLD) interface.

The SSI is used especially in ISDN terminal applications for the connection of B channel sources/sinks. It is available if timing mode 0 (bit SPM = 0, SPCR register) is programmed.

The SLD is used:

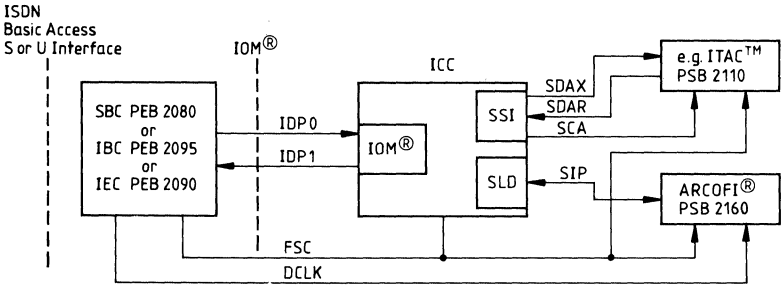
- in ISDN terminal applications for the connection of SLD compatible B channel devices
- in line card applications for the connection of a peripheral line board controller (e.g. PEB 2050).

The connections of the serial interfaces in both terminal and exchange applications are shown in **figure 7**.

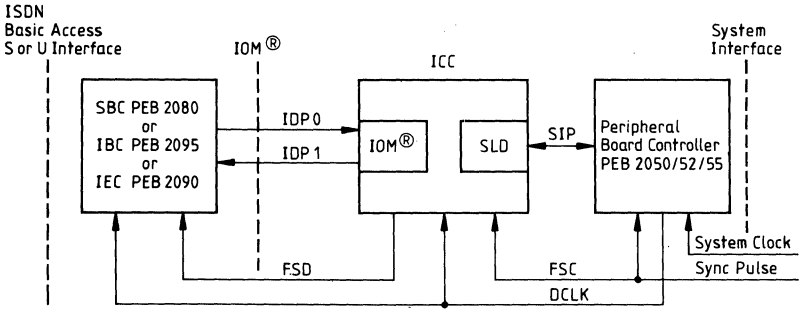
The SSI interface is only available in timing mode 0 (SPM = 0). Timing mode 1 (SPM = 1) is only applicable in exchange applications **(figure 7b)** and is used to minimize the B channel round-trip delay time for the SLD interface. Refer to section **ISDN Oriented Modular Interface.**

Figure 7

ICC Interface in IOM-1 Mode



(a) Timing Mode 0 (SPM = 0)



(b) Timing Mode 1 (SMP = 1)

The characteristics of the IOM interface are determined by bits DIM1, 0 as shown in **table 2.**

Table 2

IOM-1 Interface Mode Characteristics

DIM1	DIM0	Characteristics
0	0	Monitor channel upstream is used for TIC bus access.
0	1	Monitor channel upstream is used for TIC bus access. Bit 3 of monitor channel downstream is evaluated to control D-channel transmissions.
1	0	Monitor channel is used for TIC bus access and for data transfer.
1	1	Monitor channel is used for TIC bus access, for data transfer and for D-channel access control.

IOM-2 Mode (IMS = 1)

Serial port B is operated as an IOM-2 interface for the connection of layer-1 devices, and as a general purpose backplane bus in terminal equipment. The auxiliary serial SSI and SLD interfaces are not available in this case.

The functions carried out by the IOM are determined by bits SPM (terminal mode/non terminal mode) and DIM2-0, as shown in **table 3**.

Table 3

IOM-2 Interface Mode Characteristics

DIM2	DIM1	DIM0	Characteristics
HDLC in D channel:			Last octet of IOM channel 2 is used for TIC bus access.
0	0	0	Applicable in terminal mode (SPM = 0).
0	0	1	Last octet of IOM channel 2 is used for TIC bus access, bit 5 of last octet is evaluated to control D-channel transmission. Applicable in terminal mode (SPM = 0).
0	1	0	No TIC bus access and no S bus D-channel access control. Applicable in terminal and non-terminal mode.
0	1	1	Bit 5 of last octet is evaluated to control D-channel transmission. Applicable in terminal mode (SPM = 0).
HDLC in B or IC channel:			No transmission/reception in D channel.
1	1	0	HDLC channel selected by D1C2-0.

Note: In IOM-2 terminal mode (SPM = 0, 12-byte IOM-2 frame), all DIM2-0 combinations are meaningful. When IOM-2 non-terminal mode is programmed (SPM = 1), the only meaningful combination is "10".

HDLC Controller Mode (IMS = 0, DIM2 = 1)

In this case serial port B has no fixed frame structure, but is used as a serial HDLC port. The valid HDLC data is marked by a strobe signal input via pin FSC. The data rate is determined by the clock input DCL (maximum 4096 Mbit/s). The characteristics of the serial port B are determined by bits DIM1, 0 as shown in **table 4**.

Table 4
HDLC Mode Characteristics

DIM1	DIM0	Characteristics
0	0	reserved
0	1	FSC strobe active low
1	0	FSC strobe active high
1	1	FSC strobe ignored

Interfaces

The ICC serves three different user-oriented interface types:

- parallel processor interface to higher layer functions
- IOM interface: between layer 1 and layer 2, and as a universal backplane for terminals
- SSI and SLD interfaces for B channel sources and destinations (in IOM-1 mode only).

µP Interface

The ICC is programmed via an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 (18) lines and is directly compatible with multiplexed and non-multiplexed microcontroller interfaces (Siemens/Intel or Motorola type buses). The microprocessor interface signals are summarized in **table 5**.

Table 5

µP Interface of the ICC

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
21	25	AD0/D0	I/O	**Multiplexed Bus Mode:** Address/Data bus.
22	26	AD1/D1	I/O	Transfers addresses from the µP system to
23	27	AD2/D2	I/O	the ICC and data between the µP system
24	28	AD3/D3	I/O	and the ICC.
1	1	AD4/D4	I/O	Non-Multiplexed Bus Mode: Data bus.
2	2	AD5/D5	I/O	Transfers data between the µP system and
3	3	AD6/D6	I/O	the ICC.
4	4	AD7/D7	I/O	
17	21	$\overline{CS}$	I	**Chip Select.** A 0 ("low") on this line selects the ICC for a read/write operation.
–	23	R/$\overline{W}$	I	**Read/Write.** At 1 ("high"), identifies a valid µP access as a read operation. At 0, identifies a valid µP access as a write operation (Motorola bus mode).
19	23	$\overline{WR}$	I	Write. This signal indicates a write operation (Siemens/Intel bus mode).
–	24	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
20	24	$\overline{RD}$	I	Read. This signal indicates a read operation (Siemens/Intel bus mode).
15	18	$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the ICC requests an interrupt. It is an open drain output.
16	20	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address bus (Multiplexed bus type only).
	19	A0	I	Address bit 0 (Non-multiplexed bus type).
	5	A1	I	Address bit 1 (Non-multiplexed bus type).
	6	A2	I	Address bit 2 (Non-multiplexed bus type).
	11	A3	I	Address bit 3 (Non-multiplexed bus type).
	12	A4	I	Address bit 4 (Non-multiplexed bus type).
	13	A5	I	Address bit 5 (Non-multiplexed bus type).

ISDN Oriented Modular (IOM-1) Interface

IOM-1

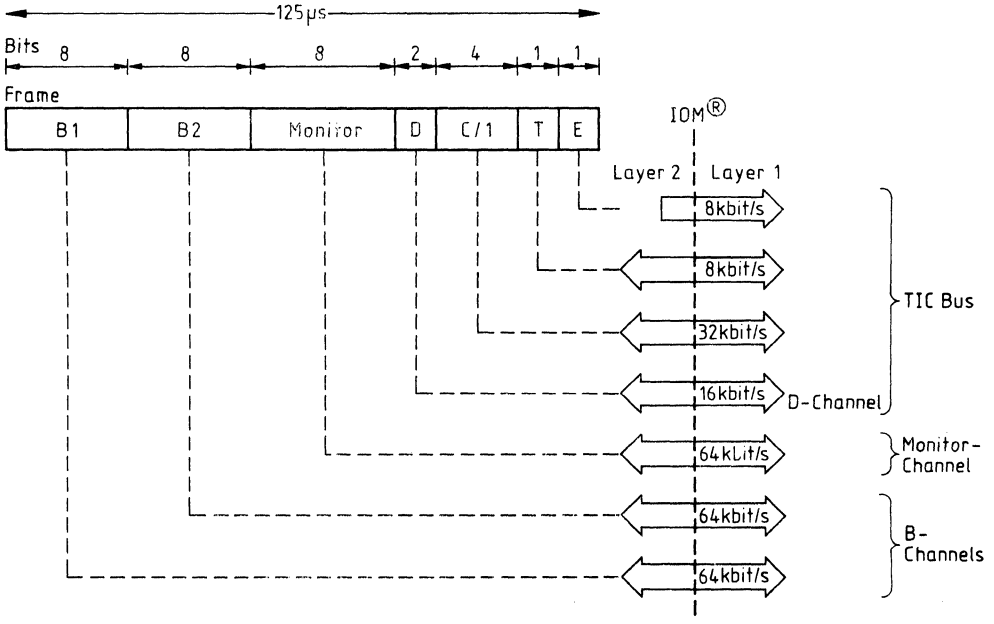
This interface consists of one data line per direction (IOM Data Ports 0 and 1: IDP0,1). Three additional signals define the data clock (DCL) and the frame synchronization (FSC/FSD) at this interface. The data clock has a frequency of 512 kHz (twice the data rate) and the frame sync clock has a repetition rate of 8 kHz.

Via this interface four octets are transmitted per 125 µs frame **(figure 8)**:

- The first two octets constitute the two 64 kbit/s B channels.
- The third octet is the monitor channel. It is used for the exchange of data using the IOM-1 monitor channel protocol which involves the E bit as a validation bit. In addition, it carries a bit which enables/inhibits the transmission of HDLC frames (IDP0) and it serves to arbitrate the access to the last octet (IDP1).
- The fourth octet is called the Telecom IC (TIC) bus because of the offered busing capability. It is constituted of the 16 kbit/s D channel (2 bits), a four-bit Command/ Indication channel and the T and E bits. The C/I channel serves to control and monitor layer-1 functions (e.g. activation/deactivation of a transmission line..). The T bit is a transparent 8 kbit/s channel which can be accessed from the ICC, and the E bit is used in monitor byte transfer.

Figure 8

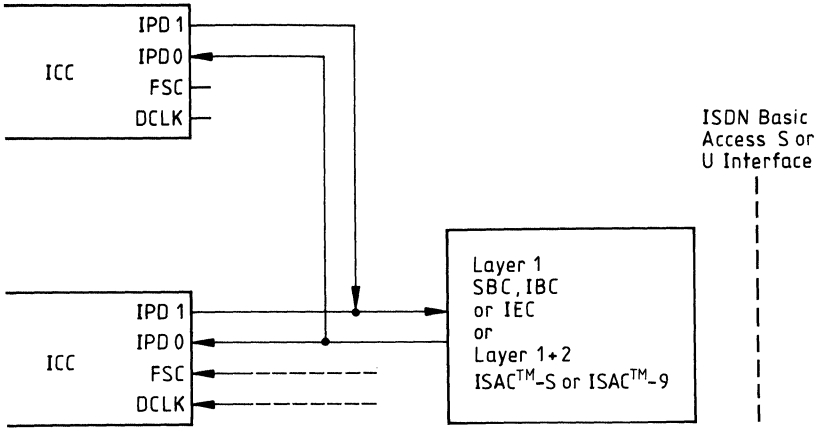
IOM®-1 Frame Structure



TIC Bus and Arbitration via Monitor Channel

The arbitration mechanism implemented in the monitor channel allows the access of more than one (up to eight) ICC to the last octet of IOM (TIC). This capability is useful for the modular implementation of different ISDN services (different service access points) e.g. in ISDN voice/data terminals. The IDP1 pins are connected together in a wired-or configuration, as shown in **figure 8**.

Figure 9
IOM Bus (TIC Bus) Configuration

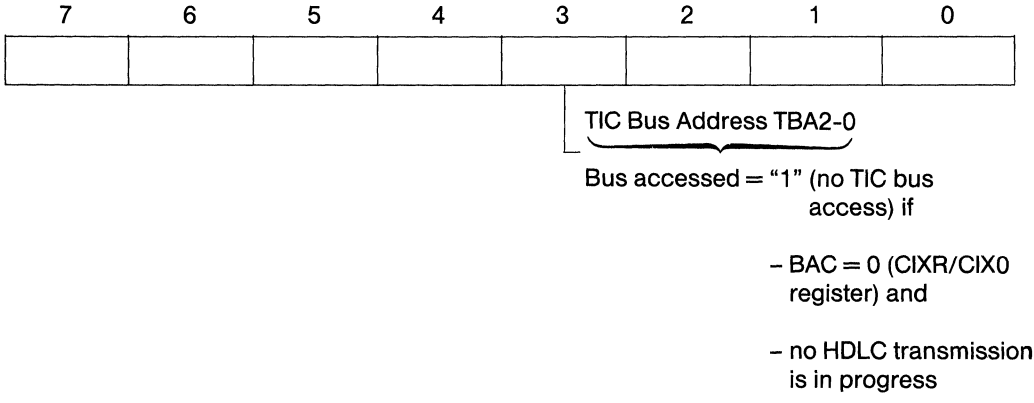


The arbitration mechanism is described in the following.

An access request to the TIC bus may either be generated by software (µP access to the C/I channel) or by the ICC itself (transmission of an HDLC frame). A software access request to the bus is effected by setting the BAC bit (CIXR/CIX0 register) to "1".

In the case of an access request, the ICC checks the bus accessed-bit (bit 3 of IDP1 monitor octet, **see figure 10)** for the status "bus free", which is indicated by a logical "1". If the bus is free, the ICC transmits its individual TIC bus address programmed in STCR register. The TIC bus is occupied by the device which is able to send its address error-free. If more than one device attempt to seize the bus simultaneously, the one with the lowest address value wins.

Figure 10
Monitor Channel Structure on IDP1



When the TIC bus is seized by the ICC, the bus is identified to other devices as occupied via the IDP1 monitor channel bus accessed bit state "0" until the access request is withdrawn. After a successful bus access, the ICC is automatically set into a lower priority class, that is, a new bus access cannot be performed until the status "bus free" is indicated in two successive frames.

If none of the devices connected to the IOM interface request access to the D and C/I channels, the TIC bus address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I channels.

Note Bit BAC (CIXR/CIX0 register) should be reset by the µP when access to the C/I channel is no more requested, to grant other devices access to these channels.

Monitor channel

When the ICC is used in connection with an S interface layer-1 transceiver, an indication must be given to the ICC whether the D channel is available for transmission (TE applications with short passive or extended bus configuration).

This indication is assumed to be given in bit 3 "Stop/Go" (S/G) of the monitor input channel on IDP0 **(figure 11)**. When a HDLC frame is to be transmitted in the D channel, the ICC automatically starts, proceeds with, or stops frame transmission according to the S/G bit value:

Figure 11

Monitor Channel Structure on IDP0

S/G = 1: stop
S/G = 0: go

7	6	5	4	3	2	1	0
1	1	1	1	S/G	1	1	1

IOM-1 Timing

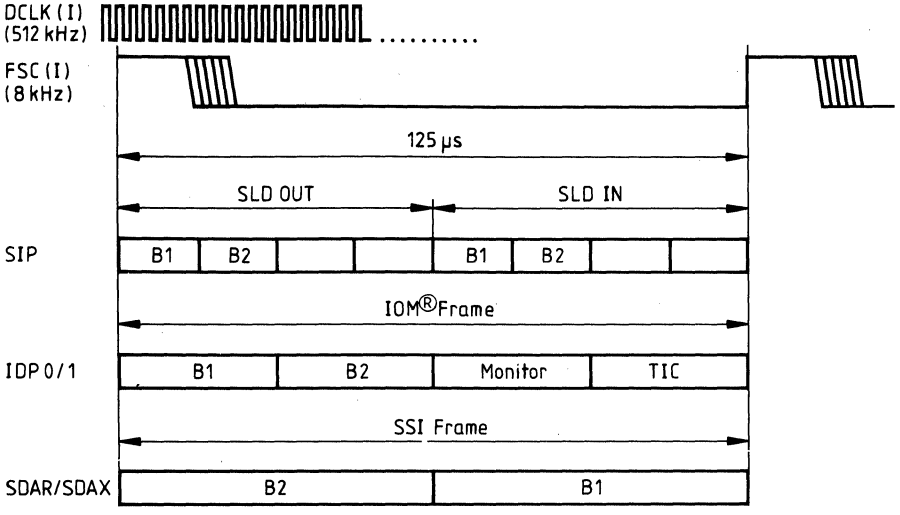
In IOM-1 mode, the ICC may be operated either in timing mode 0 or timing mode 1. The selections is via bit SPM in SPCR register.

Timing mode 0 **(SPM = 0)** is used in terminal applications. Timing mode 1 **(SPM = 1)** is only meaningful in exchange applications when the SLD is used. Programming timing mode 1 minimizes the B channel round-trip delay time on the SLD interface.

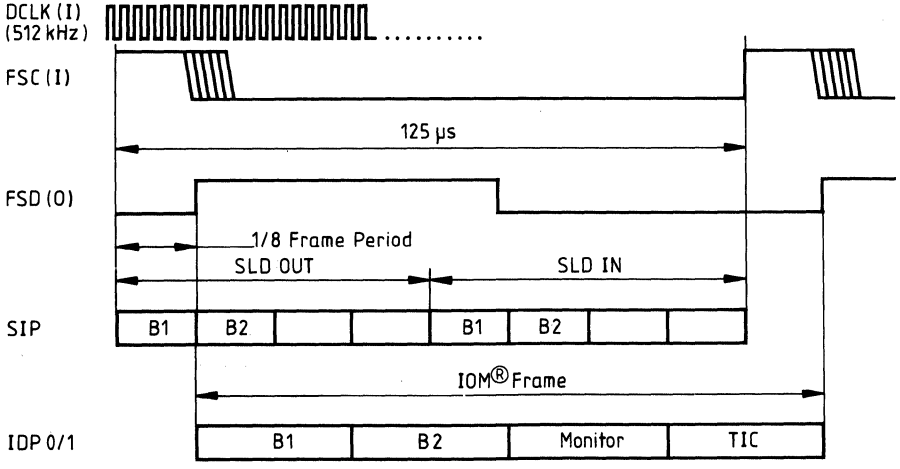
In timing mode 0 the IOM frame begin is marked by a rising edge on the FSC input. It simultaneously marks tthe beginning of the SLD frame **(figure 11)**.

In timing mode 1 the IOM frame begin is marked by a rising edge on FSD output. The FSD output is delayed by the ICC by 1/8 th of a frame with respect to FSC **(figure 12)**.

Figure 12
Interface Timing in IOM-1 Mode



(a) Timing Mode 0



(b) Timing Mode 1

IOM-2

The IOM-2 is a generalization and enhancement of the IOM-1. While the basic frame structure is very similar, IOM-2 offers further capacity for the transfer of maintenance information. In terminal applications, the IOM-2 constitutes a powerful backplane bus offering intercommunication and sophisticated control capabilities for peripheral modules.

The channel structure of the IOM-2 is depicted in **figure 13**:

Figure 13
Channel Structure of IOM-2

B1	B2	Monitor	D	C/I	MR	MX

- The first two octets constitute the two 64 kbit/s B channels.
- The third octet is the monitor channel. It is used for the exchange of data between the ICC and the other attached device(s) using the IOM-2 monitor channel protocol.
- The fourth octet (control channel) contains
  - two bits for the 16 kbit/s D channel
  - a four-bit command/indication channel
  - two bits MR and MX for supporting the monitor channel protocol.

In the case of an IOM-2 interface, the frame structure depends on whether TE- or non-TE is selected, via bit SPM in SPCR register.

Non-TE timing mode (SPM = 1)

In this case, the frame is a multiplex of eight IOM-2 channels **(figure 14)**, each channel has the structure in **figure 13**.

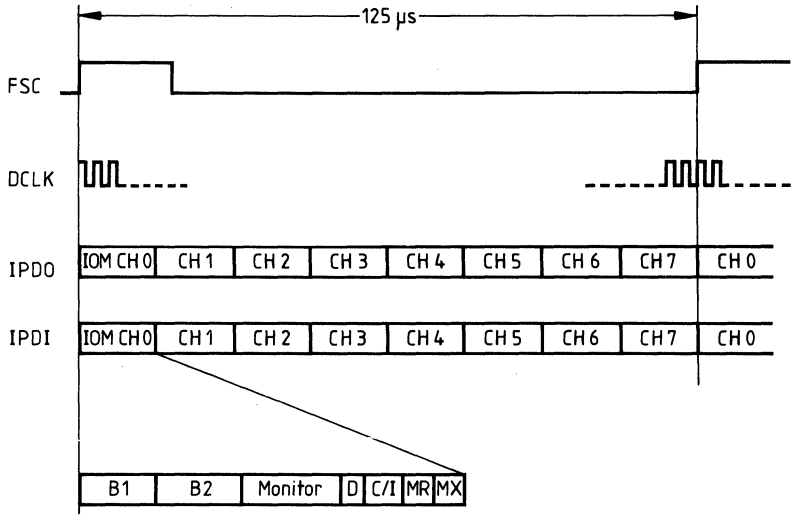
Thus the data rate per subscriber connection (corresponding to one channel) is 256 kbit/s, whereas the bit rate is 2048 kbit/s. The IOM-2 interface signals are:

IDP0,1: 2048 kbit/s

DCLK 4096 kHz-input

FSC: 8 kHz-input

Figure 14
Multiplexed Frame Structure of the IOM-2 Interface in Non-TE Timing Mode



The ICC is assigned to one of the eight channels (0 to 7) via register programming.
This mode is used in ISDN exchange/line card applications.

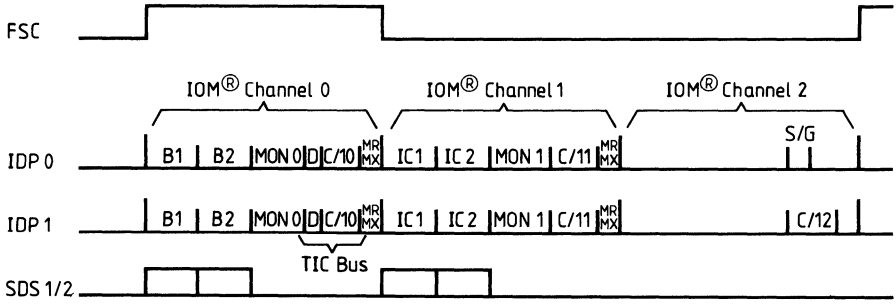
TE Timing Mode (SPM = 0)

The frame is composed of three channels **(figure 14)**:

- Channel 0 contains 144 kbit/s (for 2B + D) plus monitor and command/indication channels for layer-1 devices.
- Channel 1 contains two 64-kbit/s intercommunication channels plus monitor and command/indication channels for other IOM-2 devices.
- Channel 2 is used for enabling/inhibiting the transmission of HDLC frames. This bit is typically generated by an S-bus transceiver (stop/go: bit 5, or 3rd MSB of the last octet on IDP0). On IDP1, bits 2 to 5 of the last octet are used for TIC bus access arbitration.

As in the IOM-1 case **(figure 9)**, up to eight ICCs can access the TIC bus (D and C/I channels). The bus arbitration mechanism is identical to that described previously, except that it involves bits 2 to 5 in channel 2.

Figure 15
Definition of IOM-2 Channels in Terminal Timing Mode



The IOM-2 signals are:

IDP0,1: 768 kbit/s

DCLK: 1536-kHz input

FSC: 8-kHz input.

In addition, to support standard combos/data devices the following signals are generated as outputs:

SDS1/2: 8-kHz programmable data strobe signals for selecting one or both B/IC channel(s).

SSI (Serial Port A)

The SSI (Serial Synchronous Interface) is available in IOM-1 interface mode. Timing mode 0 (SPM = 0) has to be programmed.

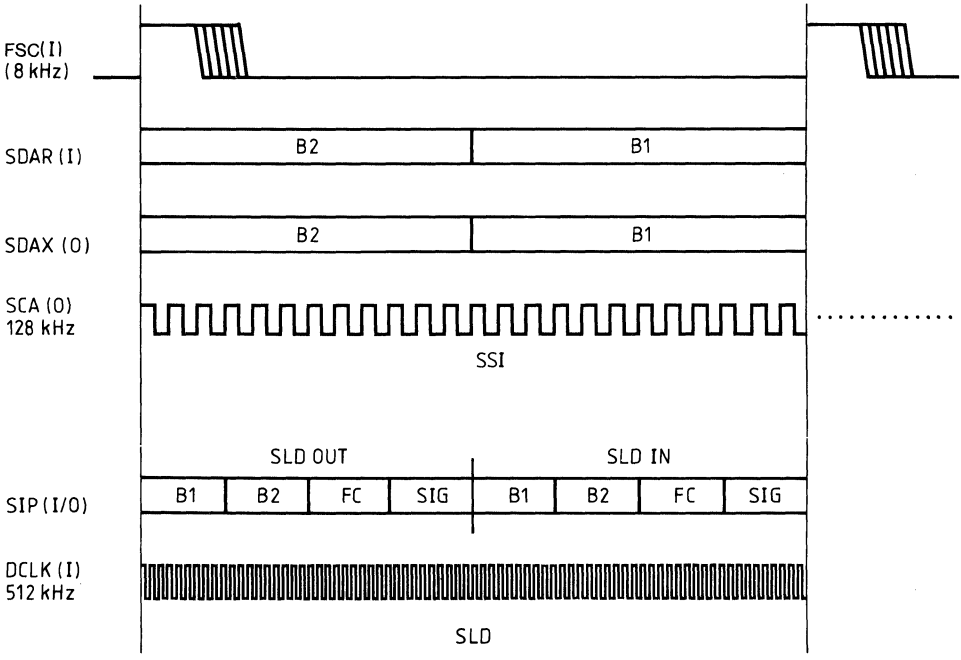
The serial port SSI has a data rate of 128 kbit/s. It offers a full duplex link for B channels in ISDN voice/data terminals. Examples: serial synchronous transceiver devices (USART's, HSCX SAB 82525, ITAC PSB 2110, ...), and CODEC filters.

The port consists of one data line in each direction (SDAX and SDAR) and the 128 kHz clock output (SCA). The beginning of B2 is marked by a rising edge on FSC, **see figure 15.**

The µC system has access to B-channel data via the ICC registers BCR1/2 and BCX1/2.

The µC access must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR).

Figure 16
SSI and SLD Interface Lines



SLD

The SLD is available in IOM-1 interface mode.

The standard SLD interface is a three-wire interface with a 512-kHz clock input (DCL), an 8-kHz frame direction signal input (FSC), and a serial ping-pong data lead (SIP) with an effective full duplex data rate of 256 kbit/s.

The frame is composed of four octets per direction. Octets 1 and 2 contain the two B channels, octet 3 is a feature control byte, and octet 4 is signaling byte **(figure 16)**.

The SLD interface can be used in:

– **Terminal applications** as a full duplex time-multiplexed (ping-pong) connection to B-channel sources/destinations.

  CODEC filters, such as the SICOFI (PEB 2060) or the ARCOFI (PSB 2160) as well as other SLD compatible voice/data modules may be connected directly to the ICC. Terminal specific functions have to be deselected (TSF = 0), so that pin SIP/EAW takes on its proper function as SLD data line. Moreover, in TE applications timing mode 0 has to be programmed.

- **Digital exchange applications** as a full duplex time-multiplexed connection to convey the B channels between the layer-1 devices and a Peripheral Board Controller (e.g. PBC PEB 2050 or PIC PEB 2052), which performs time-slot assignment on the PCM highways, forming a system interface to a switching network.

  Timing mode 1 (SPM = 1) can be programmed in order to minimize the B channel round-trip delay.

The µC system has access to B-channel data, the feature control byte and the signaling byte via the ICC registers:

- C1R,C2R → B1/B2
- CFCR and SFCX → FC
- SSCR and SSCX → SIG

The µP access to C1R,C2R,SFCR, SFCR,SSCR and SSCX must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR) and the BVS-bit (STAR).

Register Description

The parameterization of the ICC and the transfer of data and control information between the µP and ICC is performed through the R- and XFIFO and two register sets. The address map is shown in **table 6**.

The two FIFOs have an identical address range 00-1F_H.

The register set in the address range 20-2A pertains to the HDLC transceiver and LAPD controller. The register set ranging from 30 to 3B pertains to the control of layer-1 functions and of the IOM interface.

For a detailed register description please refer to the ICC Technical Manual.

Table 6
ICC Address Map and Register Summary

Address (hex)	Read		Write	
	Name	**Description**	**Name**	**Description**
00 . . 1F	RFIFO	Receive FIFO	XFIFO	Transmit FIFO
20	ISTA	Interrupt Status Register	MASK	Mask Register
21	STAR	Status Register	CMDR	Command Register
22	MODE	Mode Register		
23	TIMR	Timer Register		
24	EXIR	Extended Interrupt Register	XAD1	Transmit Address 1
25	RBCL	Receive Frame Byte Count Low	XAD2	Transmit Address 2
26	SAPR	Received SAPI	SAP1	Individual SAPI 1
27	RSTA	Receive Status Register	SAP2	Individual SAPI 2
28			TEI1	Individual TEI 1
29	RHCR	Receive HDLC Control	TEI2	Individual TEI 2
2A	RBCH	Receive Frame Byte Count High		
30	SPCR	Serial Port Control Register		
31	CIRR/ CIR0	Command/Indication Receive (0)	CIXR/ CIX0	Command/Indication Transmit (0)
31	MOR/ MOR0	Monitor Receive (0)	MOX/ MOX0	Monitor Transmit (0)
33	SSCR/ CIR1	SIP Signaling Code Receive/ Command/Indication Receive 1	SSCX/ CIX1	SIP Signaling Code Transmit/ Command/Indication Transmit 1
34	SFCR/ MOR1	SIP Feature Control Read/ Monitor Receive 1	SFCW/ MOX1	SIP Feature Control Write/ Monitor Transmit 1
35	C1R	Channel Register 1		
36	C2R	Channel Register 2		
37	B1CR	B1 Channel Register	STCR	Sync Transfer Control Register
38	B2CR	B2 Channel Register	ADF1	Additional Feature Register 1
39	ADF2	Additional Feature Register 2		
3A	MOSR	Monitor Status Register	MOCR	Monitor Control Register

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	-0.4 to $V_{DD}+0.4$	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	-65 to 125	°C

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5$ V, $V_{SS} = 0$ V.

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	
L-input voltage		V_{IL}	-0.4	0.8	V		
H-input voltage		V_{IH}	2.0	$V_{DD}+0.4$	V		
L-output voltage		V_{OL}		0.45	V	$I_{OL} = 7$ mA pin IDP0, IDP1 $I_{OL} = 2$ mA all other pins	
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 $V_{DD}-0.5$		V V	$I_{OH} = -400$ µA $I_{OH} = -100$ µA	
Power supply current	operational	I_{CC}		1.6 3.5 8.0	mA mA mA	DCLK: 512 kHz DCLK: 1536 kHz DCLK: 4096 kHz	$V_{DD} = 5$ V, inputs at 0 V/V_{DD} no output loads
	power down			0.6	mA		
Input leakage current Output leakage current		I_{LI} I_{LO}		10	µA	$0 \text{ V} < V_{IN}, V_{DD}$ to 0 V $0 \text{ V} < V_{OUT} < V_{DD}$ to 0 V	

Capacitances

$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$, $f_C = 1\,MHz$, unmeasured pins returned to GND.

Parameter	Symbol	Limit Values		Unit
		typ.	max.	
Input capacitance	C_{IN}	5	10	pF
Output capacitance $f_C = 1$ MHz	C_{OUT}	10	20	pF
I/O capacitance $f_C = 1$ MHz	C_{IO}	8	15	pF

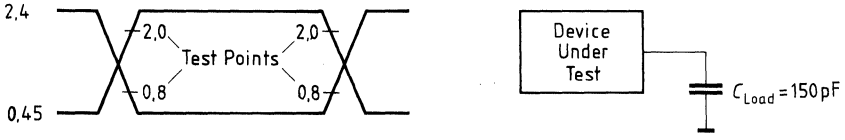
AC Characteristics

$T_A = 0$ to $70\,°C$, $V_{DD} = 5\,V \pm 5\%$

Inputs are driven to 2.4 V for a logical "1" anf to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown below.

Figure 17

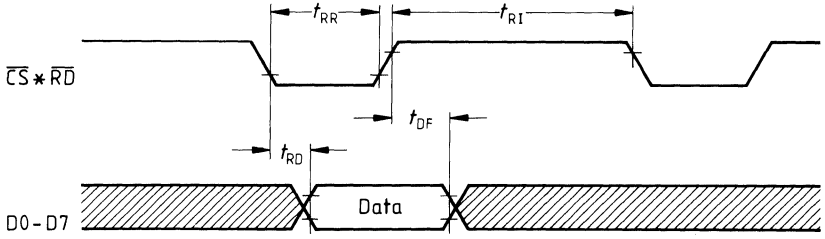
Input/Output Waveform and Load Circuit for AC Tests



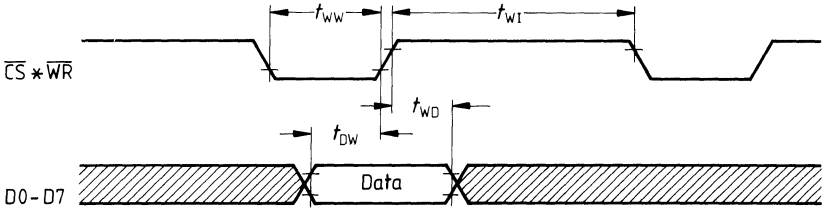
Microprocessor Interface Timing

Siemens/Intel Bus Mode

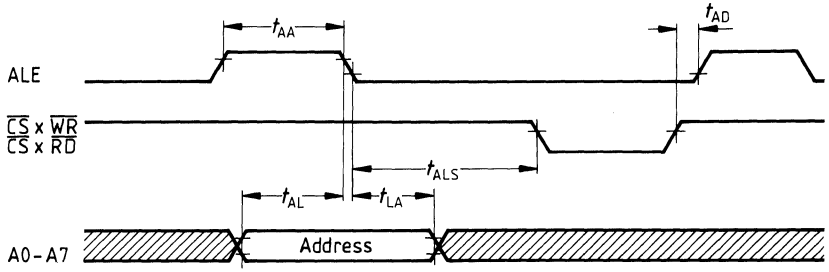
µP Read Cycle



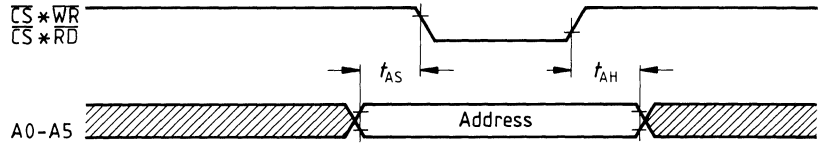
µP Write Cycle



Multiplexed Address Timing

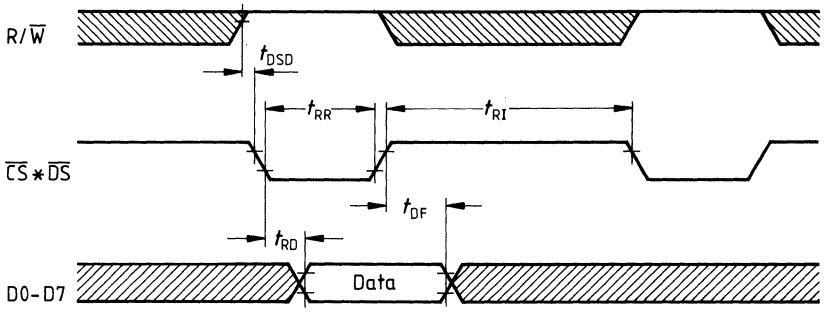


Non-Multiplexed Address Timing

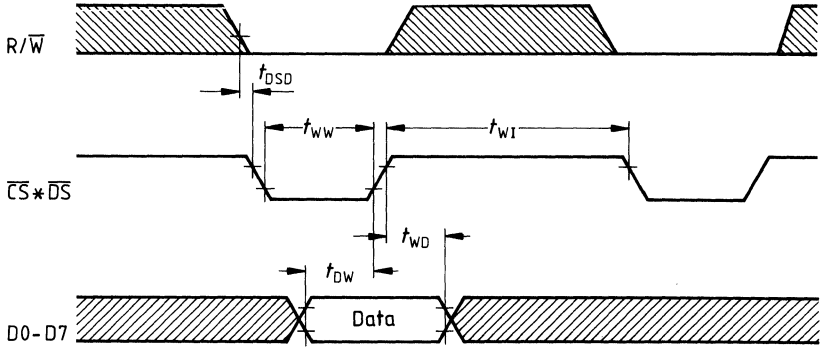


Motorola Bus Mode

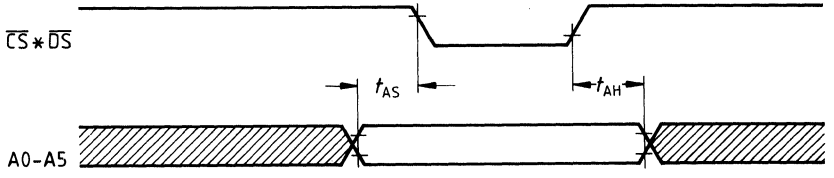
µP Read Cycle



µP Write Cycle



Address Timing



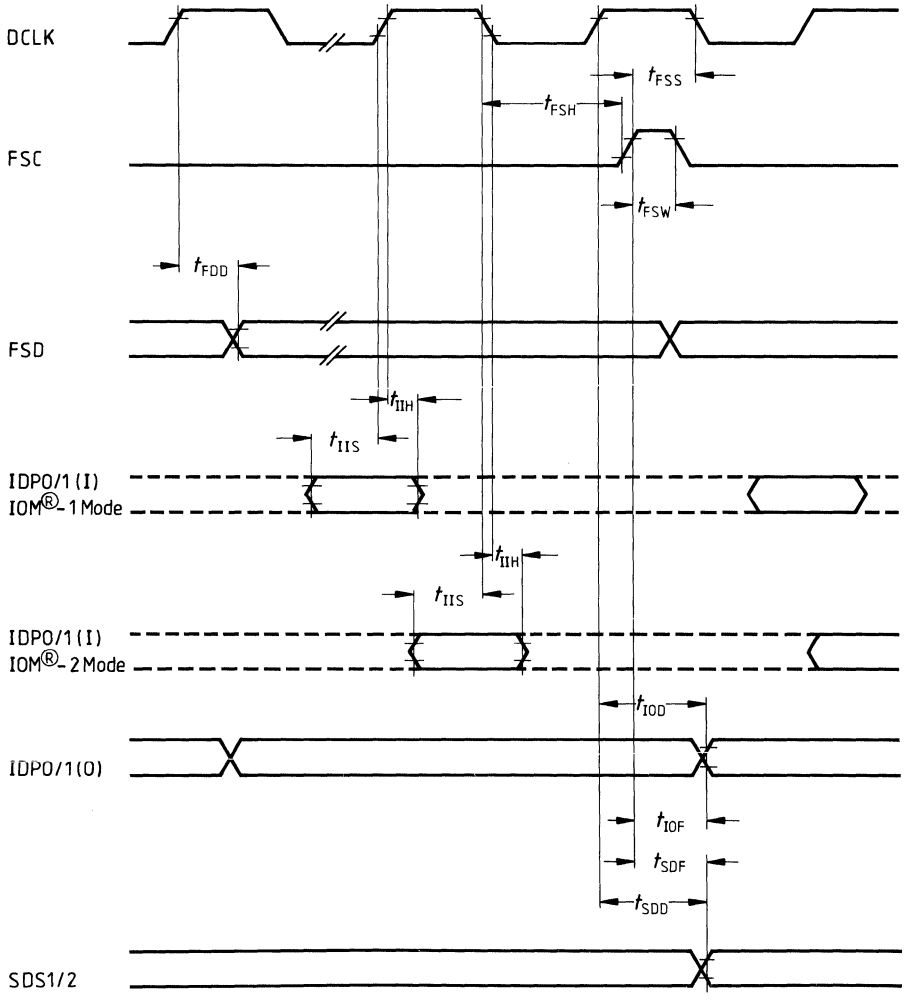
Parameters and Values of the Bus Modes

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	20		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	20		ns
ALE pulse delay	t_{AD}	15		ns
DS delay after $\overline{R/W}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$* $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{WR}$* $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

Serial Interface Timing

IOM Mode

IOM Timing



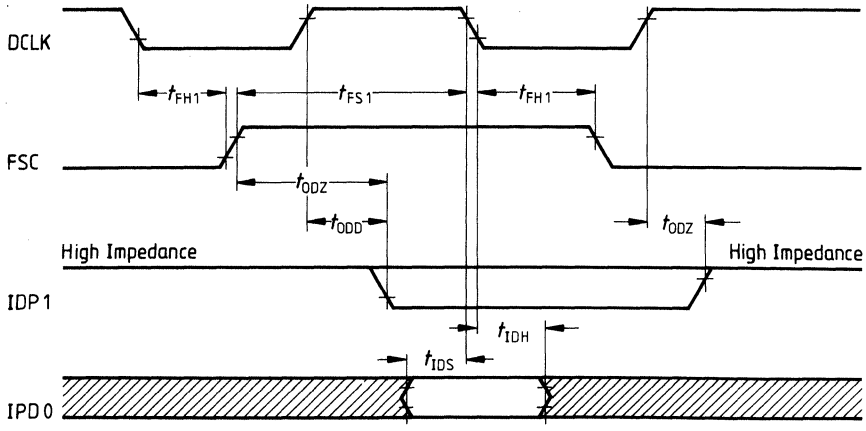
Parameters and Values of IOM Mode

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
IOM output data delay	t_{IOD}	20 20	140 100	ns ns	IOM-1 IOM-2
IOM input data setup	t_{IIS}	40 20		ns ns	IOM-1 IOM-2
IOM input data hold	t_{IIH}	20		ns	
IOM output from FSC	t_{IOF}		80	ns	See note
Strobe signal delay	t_{SDD}		120	ns	
Strobe delay from FSC	t_{SDF}		120	ns	See note
Frame sync setup	t_{FSS}	50		ns	
Frame sync hold	t_{FSH}	30		ns	
Frane sync width	t_{FSW}	40		ns	
FSD delay	t_{FDD}	20	140	ns	

Note: This delay is applicable in two cases only:
1) When FSC appears for the first time, e.g. at system power-up
2) When FSC appears before the excepted start of a frame

HDLC Mode

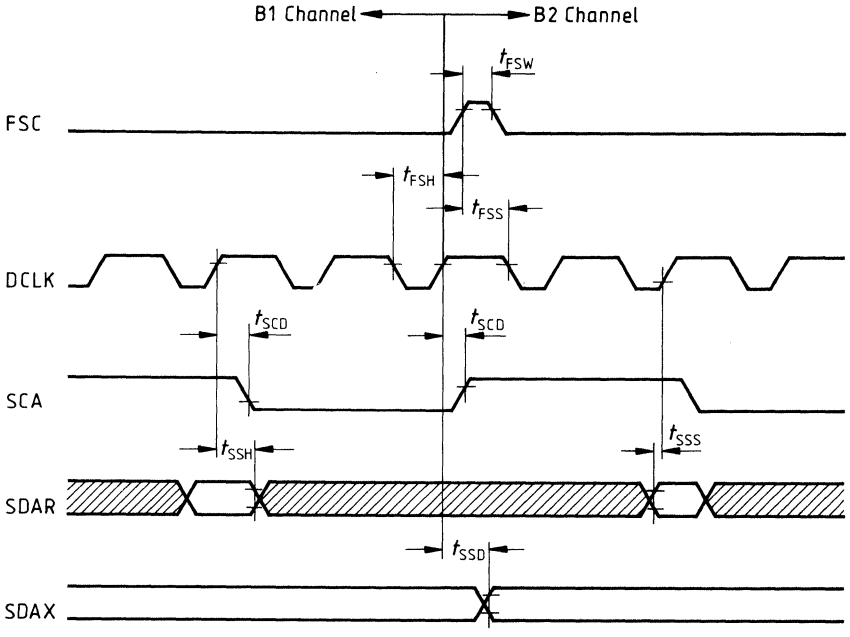
FSC (Strobe) Characteristics



Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC set-up time	t_{FS1}	100		ns
FSC hold time	t_{FH1}	30		ns
Output data from high impedance to active	t_{OZD}		80	ns
Output data from active to high impedance	t_{ODZ}		40	ns
Output data delay from DCL	t_{ODD}	20	100	ns
Input data setup	t_{IDS}	10		ns
Input data hold	t_{IDH}	30		ns

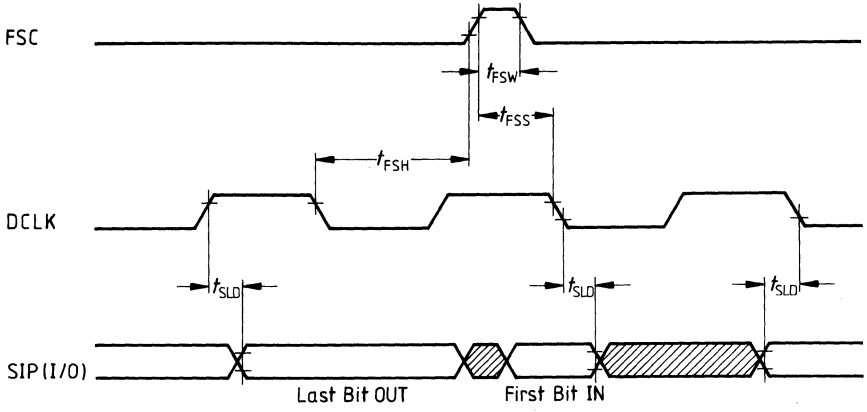
Serial Port A (SSI) Timing

SSI Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCA clock delay	t_{SCD}	20	140	ns
SSI data delay	t_{SSD}	20	140	ns
SSI data setup	t_{SSS}	40		ns
SSi data holf	t_{SSH}	20		ns
Frame sync hold	t_{FSH}	30		ns
Frame sync width	t_{FSW}	40		ns

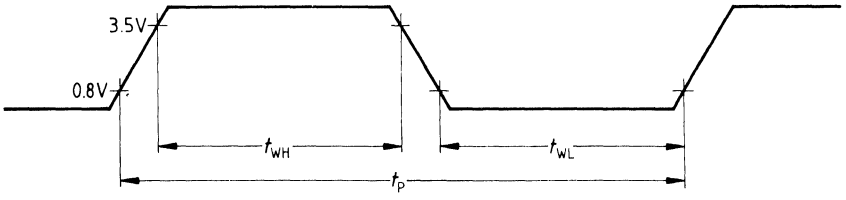
SLD Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
SLD data delay	t_{SLD}	20	140	ns
SLD data setup	t_{SLS}	30		ns
SLD data hold	t_{SLH}	30		ns
Frame sync setup	t_{FSS}	50		ns
Frame sync hold	t_{FSH}	30		ns
Frame sync width	t_{FSW}	40		ns

Clock Time

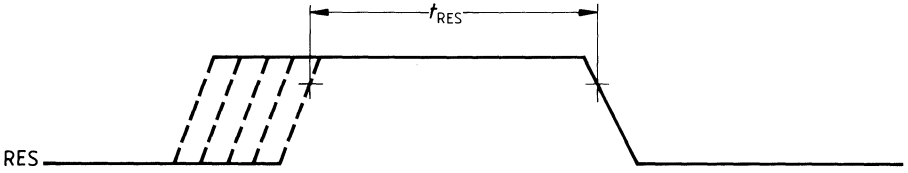
Definition of Clock Period and Width



Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Clock period	t_P	1000		ns	IOM-1
Clock width high	t_{WH}	200		ns	IOM-1
Clock width low	t_{WL}	200		ns	IOM-1
Clock period	t_P	240		ns	IOM-2
Coock width high	t_{WH}	100		ns	IOM-2
Clock width low	t_{WL}	100		ns	IOM-2

Reset

Reset Signal Characteristics



Parameter	Symbol	Limit Values	Test Conditions
		min.	
Length of active high state	t_{RES}	2*DCL clock cycles	During power up