SIEMENS

S/T Bus Interface Circuit Extended (SBCX) PEB 2081

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2081-N	Q67100-H6093	PL-CC-28 (SMD)
PEB 2081-P	Q67100-H6091	P-DIP-28
PEB 2081-P	planned	P-DIP-22

The S/T Bus Interface Circuit Extended (SBCX) PEB 2081 implements the four-wire S/T interface used to link voice/data ISDN terminals, network termination (Central Office and PBX applications), and PBX trunk lines to Central Office. Through selection of operating modes, the device may be employed in all types of applications involving an S/T interface. Two or more PEB 2081 SBCX can be used to build a point-to-point, passive bus, extended passive bus or star configuration.

The PEB 2081 SBCX provides the electrical and functional link between the analog S/T interface according to CCITT recommendation I.430 and T1D1 Basic User Network Interface Specification, respectively and the ISDN Oriented Modular (IOM®) interface Rev. 2.

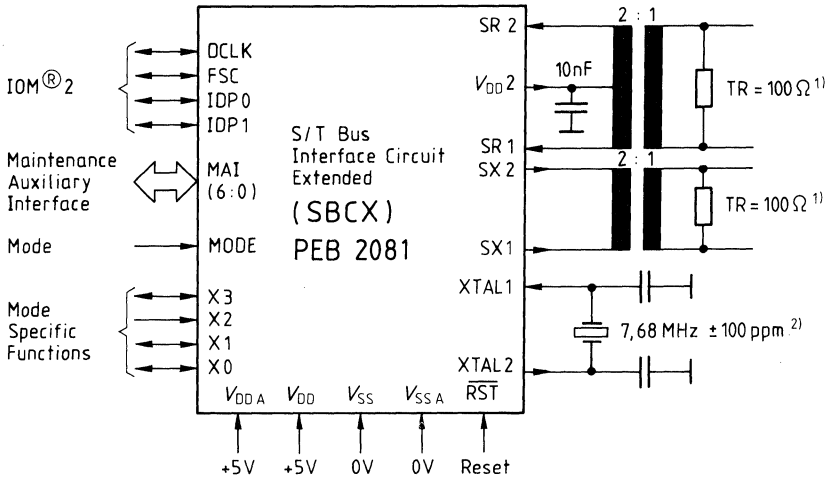
The PEB 2081 SBCX exceeds both the electrical and functional requirements of the S/T interface in order to provide high flexibility to the user with respect of S/T interface wiring configuration and implementation of layer-1 maintenance functions. By provision of some additional features at the IOM-2 interface the user is able to combine the SBCX with other IOM-2 devices in various configurations.

The PEB 2081 SBCX is a 28-pin CMOS device offered in both DIP and PL-CC packages It operates from a single 5 V supply and features a power-down state with very low power consumption.

Features

- Full duplex 2B + D S/T interface transceiver according to CCITT I.430
- Adaptive equalizer
- Receive timing recovery
- Built-in wake-up unit for activation from power-down state
- Conversion of the frame structure between the S/T interface and IOM-2 interface
- Activation and deactivation procedures according to CCITT I.430
- D-channel access control, also in trunk application
- Access to S and Q bits of S/T interface
- Automatic handling of S and Q bit messages
- Software controlled maintenance interface (i/o ports)
- Frame alignment with absorption of phase wander in NT2 network side applications
- Switching of test loops
- Several operating modes
- Advanced CMOS technology
- Low power consumption: standby less than 6 mW
  active max. 80 mW

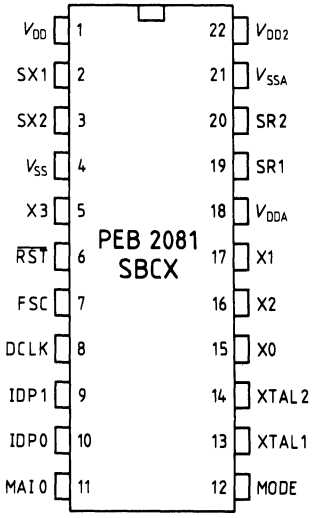
Logic Symbol



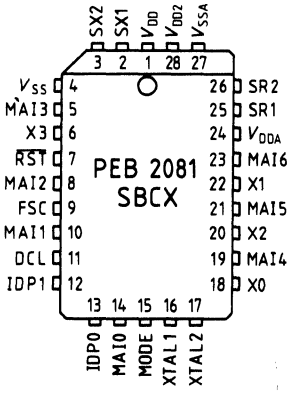
1) Terminating resistors only at the far end
2) For details of crystal **see figures 22 and 25**
3) 10 nF required only for A1 silicon.
Further versions will have a symmetrical receiver.

Pin Configurations
(top view)

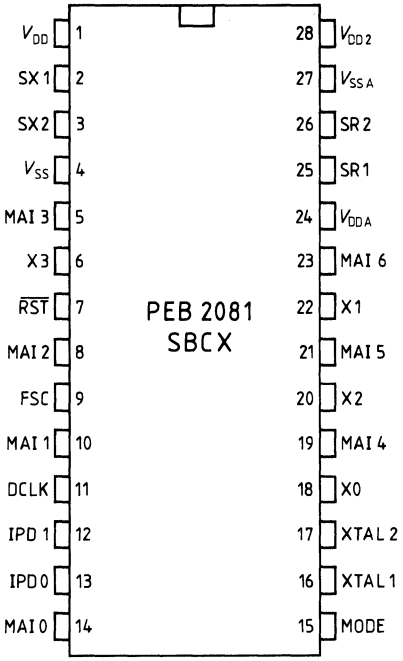
P-Dip-22



PL-CC-28



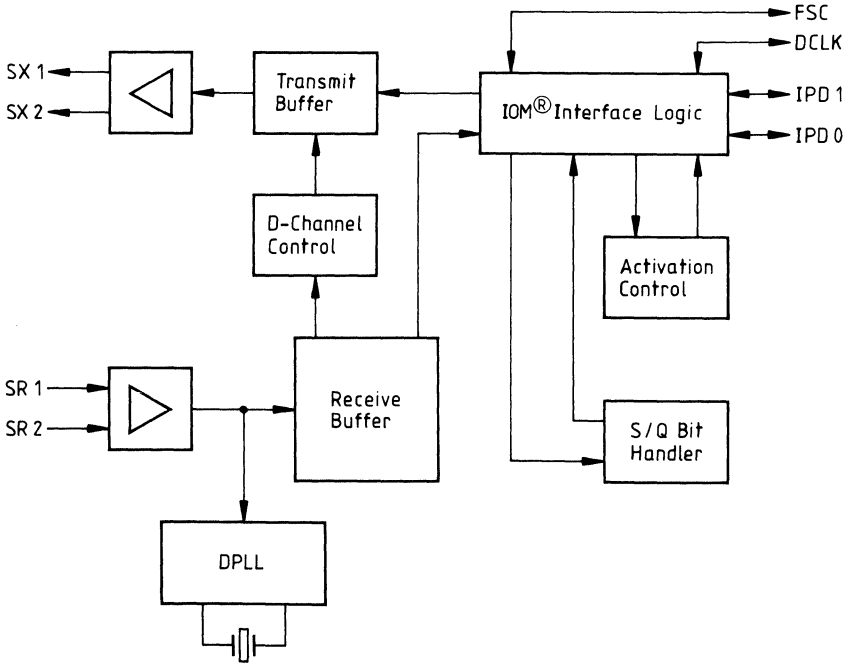
P-DIP-28



Pin Definitions and Functions

Pin No. P-DIP-28 PL-CC-28	Pin No. P-DIP-22	Symbol	Input (I) Output (O)	Function
2	2	SX1	O	Positive transmitter output
3	3	SX2	O	Negative transmitter output
13	10	IDP0	I/O	IOM Data Port 0
12	9	IDP1	I/O	IOM Data Port 1
11	8	DCLK	I/O	Data clock, IOM interface
9	7	FSC	I/O	Frame Sync, IOM interface
15	12	MODE	I	Setting of operating mode
6 20 22 18	5 16 17 15	X3 X2 X1 X0	I/O I/O I/O I/O	Functions dependant on the selected operation mode, **see chapter 2.**
23, 21, 19		MAI (6:4)	O	Maintenance output pins controlled by monitor channel
5, 8, 10, 14	11	MAI (3:0)	I	Maintenance input pins
16	13	XTAL1	I	Connection for external crystal, or input for external clock generator
17	14	XTAL2	O	Connection for external crystal, n.c. when external clock generator is used
25	19	SR1	I	Receiver, signal input
26	20	SR2	I	Receiver, signal input
28	22	V_{DD2}	O	2.5 V reference voltage output; 10 nF to V_{SS}
27	21	V_{SSA}	I	Analog ground
24	18	V_{DDA}	I	Analog power supply +5 V ± 5%
1	1	V_{DD}	I	Digital power supply +5 V ± 5%
4	4	V_{SS}	I	Digital ground
7	6	$\overline{RST}$	I	Reset, active low

Figure 1
Block Diagram



System Integration

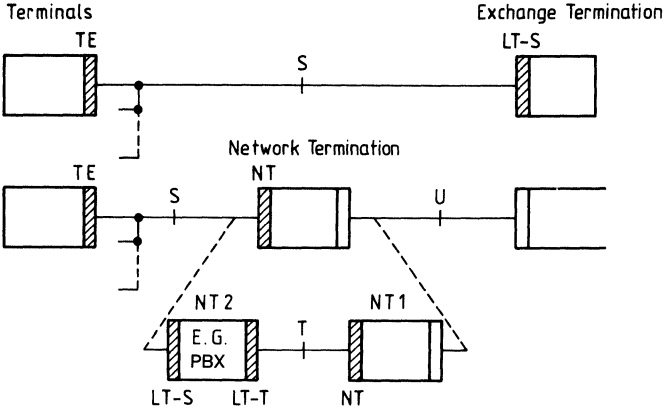
The PEB 2081 SBCX implements the four-wire S and T interfaces used in the ISDN basic access. By programming the corresponding operating mode it may be used at both ends of these interfaces.

The operating modes are:

ISDN terminals (TE)
ISDN network termination (NT)
ISDN subscriber line termination (LT-S)
ISDN trunk line termination (LT-T)
(PBX connection to Central Office).

The basic use of these modes is shown in **figure 2** where the usual nomenclature as defined by the CCITT for the basic access functional blocks and reference points, has been used.

Figure 2
Operating Modes



Terminals and Network Terminations

By adding IOM-2 compatible devices to the PEB 2081 SBCX different configurations are possible ranging from the standard TE and NT implementations shown in **figure 3** and **4** to more complex applications.

Figure 3
ISDN Voice/Data Terminal using the IOM-2 Architecture

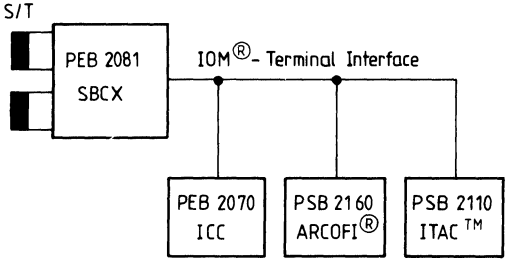
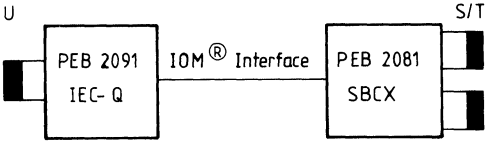
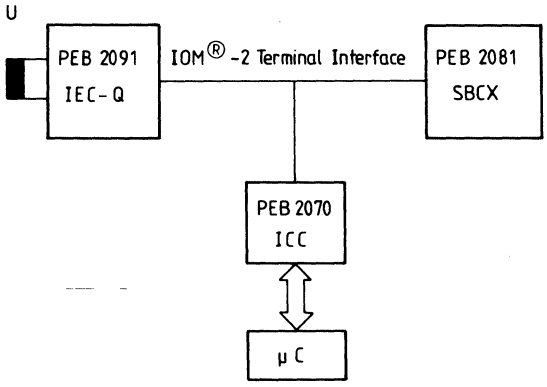


Figure 4
Network Termination with only two Devices



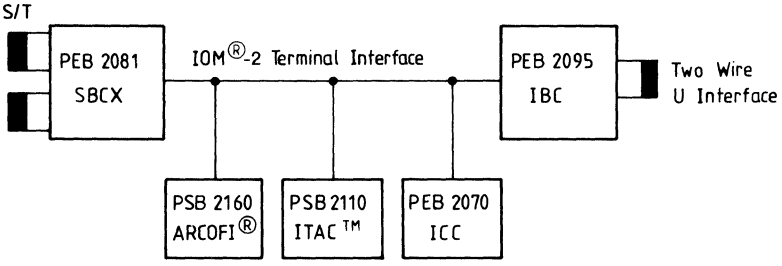
A more complex application is a microcontrolled NT using the PEB 2070 ICC to provide software controlled layer-1 maintenance functions **(figure 5)**. The U and S/T interface maintenance data is conveyed via the IOM interface's monitor channel to the PEB 2070 ICC.

Figure 5
The µC Controls all Layer-1 Maintenance Functions of the NT



More terminal functions can be added to the NT resulting in a U interface terminal with an S/T interface terminal (intelligent NT) (**figure 6**). The functionality of such a configuration includes D-channel collision resolution in upstream direction and B channel switching functions for internal communications.

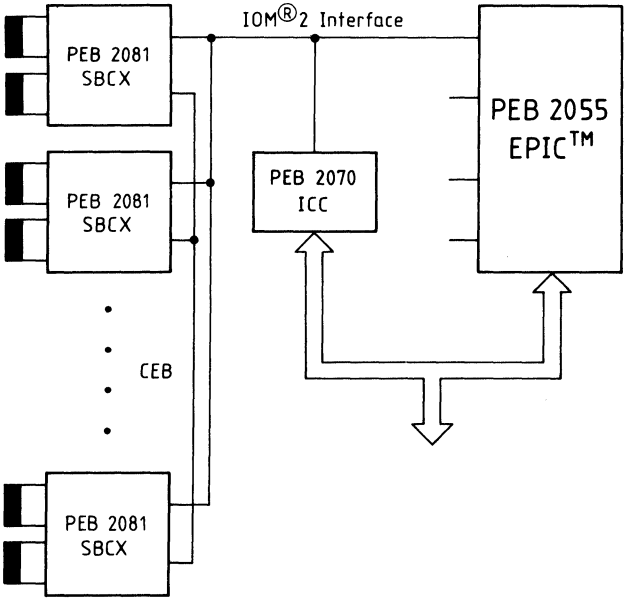
Figure 6
An Intelligent NT Provides Both Terminal (voice/data) and Network Terminating Functions (S/T interface)



Line Terminations

The standard implementation of an S/T interface line card includes one D-channel controller. per line. Due to the S/T interface's ECHO bit function this can be reduced to one D-channel controller per up to eight lines. The PEB 2081 SBCX supports this architecture by handling the ECHO bit externally as a common ECHO Bit (CEB) to all S/T interfaces (**figure 7**)

Figure 7
One LAP-D Controller is Sufficient for up to Eight S/T Interfaces.



S/T Interface Configurations

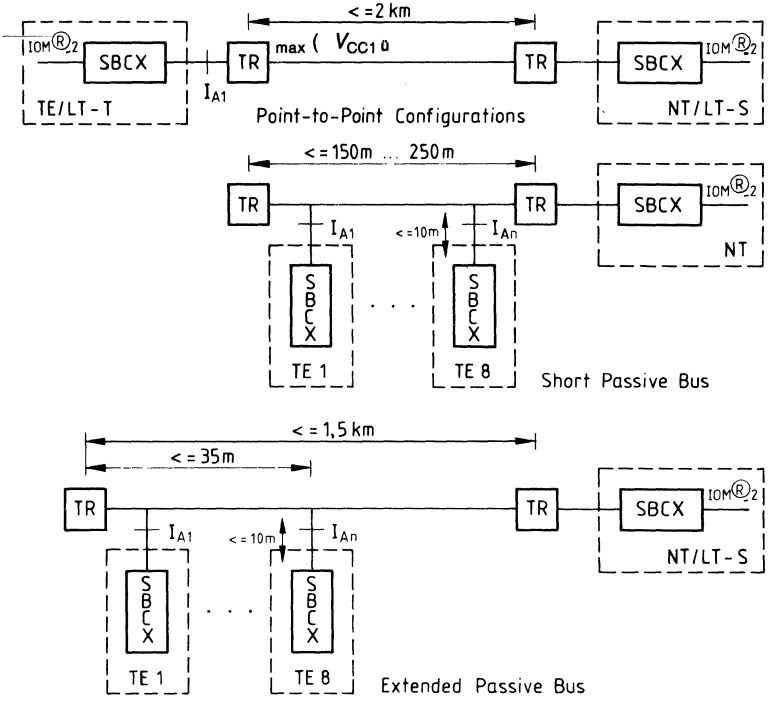
The adaptive equalizer integrated in the receiver of the PEB 2081 SBCX exceeds the electrical requirements of the S/T interface. An overview of the different wiring configurations is given in **figure 8.**

Since maximum attenuation of the line is not the limiting factor, the maximum length of a point-to-point configuration depends on the round trip delay. For special applications it is possible to exceed this limitation by switching the upstream D channel to a transparent mode. Obviously, the extended passive bus configuration benefits from the enhanced receiver characteristic resulting by increasing the loop length.

Figure 8

S/T Interfacing Wiring Configurations

(N.B.: "TR" stands for terminating resistor of value 100 Ω).



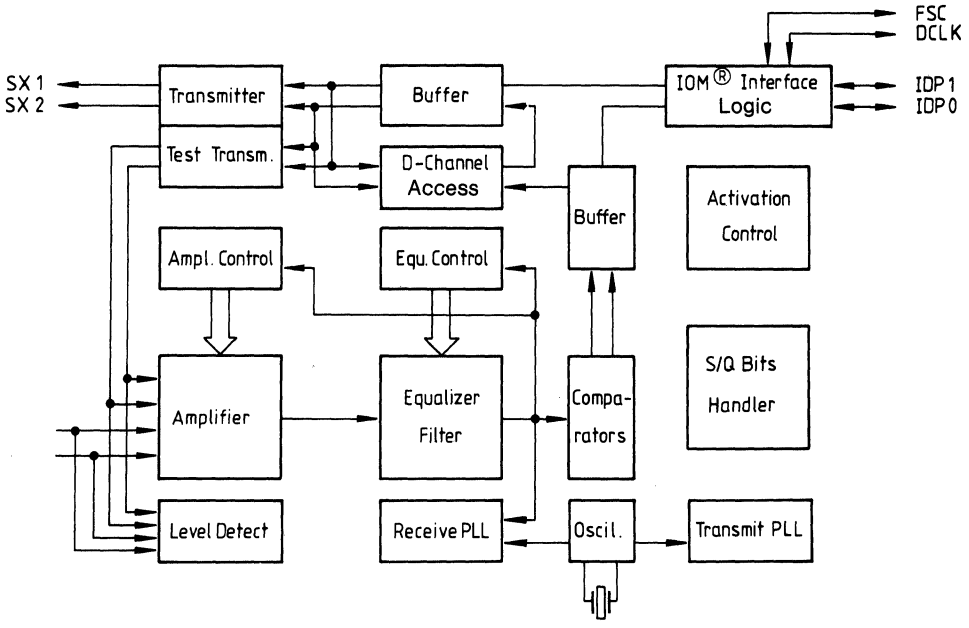
Functional Description

The PEB 2081 SBCX performs the layer-1 functions for the S/T interface of the ISDN basic access.

SBCX Device Architecture and General Functions

The SBCX performs the layer-1 functions of the S/T interface according to CCITT recommendation I.430 and T 1D1 Basic User Network Interface Specification, respectively. It can be used at all ends of the S/T interface. **Figure 9** depicts the device architecture.

Figure 9
SBCX Device Architecture



The Common Functions for all Operating Modes

- Line transceiver functions for the S/T interface according to the electrical specifications of CCITT I.430;
- Conversion of the frame structure between the IOM interface and S/T interface;
- Conversion from/to binary to/from pseudo-ternary code.
- Access to S and Q bits
- Handling of S and Q channel messages
- Level detect.

Mode Specific Functions

- Receive timing recovery for point-to-point, passive bus and extended passive bus configuration.
- S/T timing generation using IOM timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation by handling of the common echo bit.
- Activation/deactivation procedures, triggered by primitives received over the IOM interface or by INFO's received from the line;
- Frame alignment according to CCITT Q.503;
- Execution of test loops.

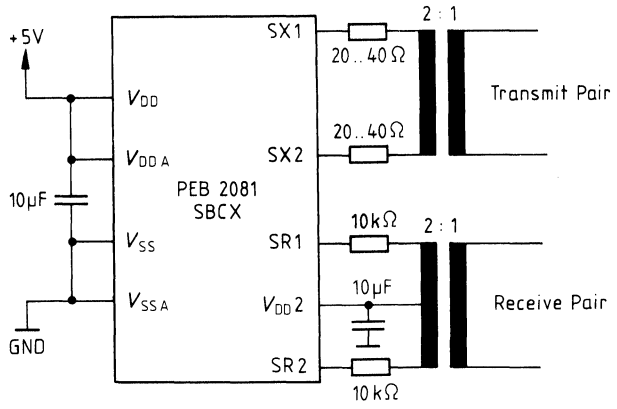
Analog Functions

For both receive and transmit direction, a 2:1 transformer is used to connect the PEB 2081 SBCX to the 4 wire S/T interface. The pseudo-ternary pulse shaping which meets the I.430 pulse templates, is achieved with the integrated transmitter.

The integrated adaptive equalizer is designed to cope with all wiring configuration of the S/T interface, point-to-point, passive bus, and extended passive bus. The maximum allowable line attenuation is increased to more than 20 dB, with the corresponding distortion equalized, and out-of-band noise suppressed.

The level detect block monitors the receive line and therefore initiates switching into power down or power up state. **Figure 10** depicts the analog connections of the PEB 2081 SBCX.

Figure 10
Connection of the Line Transformers and Power Supply to the SBCX



Digital Functions

DPLL circuitry working with a frequency of 7.68 MHz ± 100 ppm in S/T interface master modes generates the 192-kHz-line clock from the reference clock delivered by the network (FSC: 8 kHz) and in S/T interface slave modes extracts the 192-kHz line clock from the receive data stream.

The 7.68 MHz clock may be generated with the use of an external crystal between pins XTAL1 and XTAL2, or by an external oscillator, in which case XTAL2 is not connected.

The D-channel access procedure according to CCITT I.430, including priority management, is fully implemented in the SBCX. When used as an S/T interface master, the device generates the E bits necessary for D-channel collision detection. The received D-bits are provided at pin CEB (common echo bit) for a wired-AND connected NT star configuration.

The buffer memory serves to adapt the different bit rates of the S/T interface and the IOM interface. In addition, in trunk line applications it absorbs the possible deviation between two system clocks, according to CCITT Q.503 (slip detection).

In all applications, the PEB 2081 SBCX gives access to the S and Q bits via the monitor channel. According to its specific S/Q mode, it handles the S and Q channel messages autonomously, i.e. without the aid of a µC (e.g. in NT).

Table 1
Operating Modes and Functions of Mode Specific Pins of the SBCX.

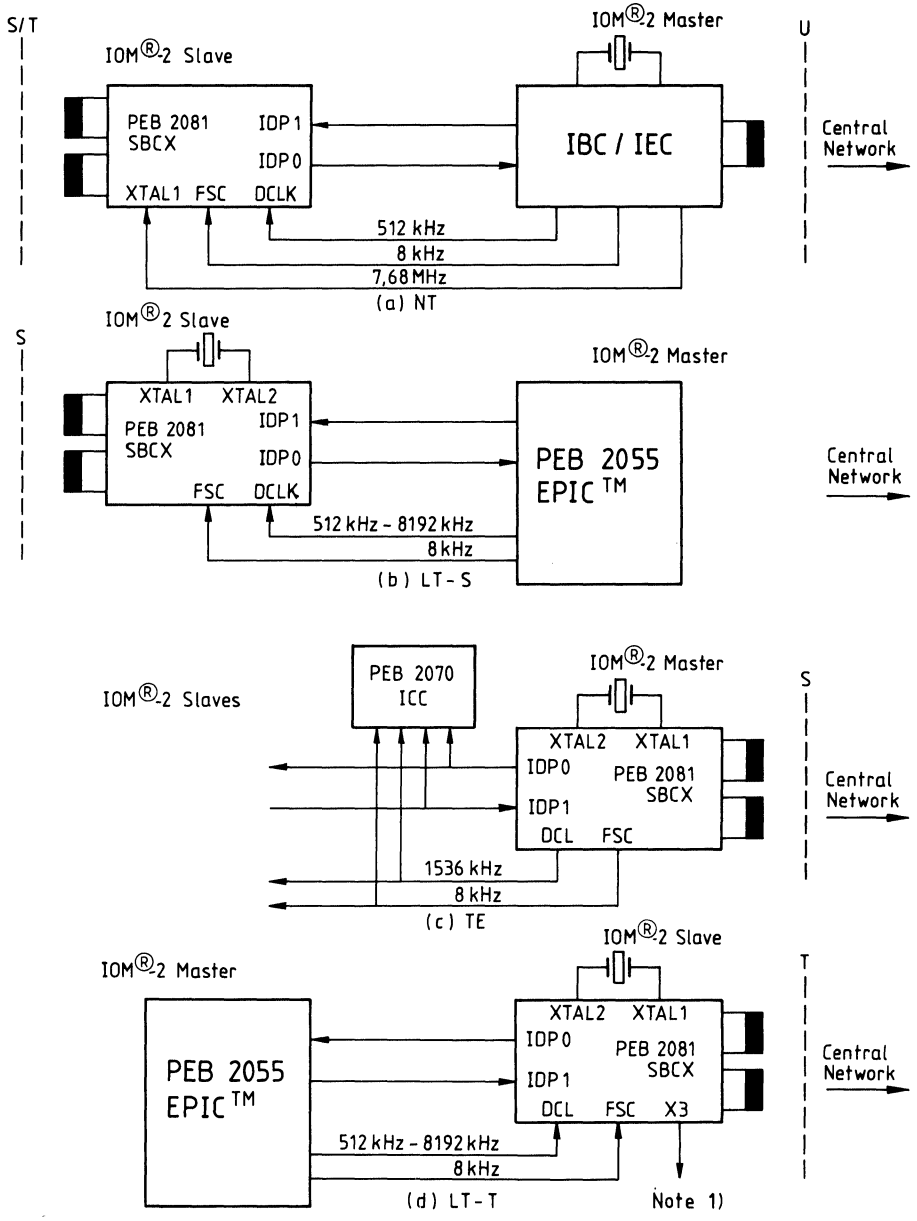
	Application			
	TE	**LT-T**	**NT**	**LT-S**
MODE	i: V_{SS}	i: V_{DD}	i: V_{SS}	i: V_{DD}
DCLK	o: 1536 kHz[1)]	i: 512 kHz to 8192 kHz	i: 512 kHz to 8192 kHz	i: 512 kHz to 8192 kHz
FSC	o: 8 kHz[1)]	i: 8 kHz	i: 8 kHz	i: 8 kHz
X3	o: 768 kHz[1)]	o: 1536 kHz[1)]	i/o: CEB	i/o: CEB
X2	i: V_{SS}	i: ICN2	i: V_{DD}	i: ICN2
X1	i: V_{SS}	i: ICN1	i: V_{SS}	i: ICN1
X0	o: PCK	i: ICN0	i: BUS	i: ICN0

[1)] synchronized to S/T interface
i: input o: output

PCLK Power Converter Clock
BUS Bus configuration specified
CEB Common Echo Bit in NT1 star

Note: Differentiation between LT-T mode and LT-S mode is done by software programming of data bit 0 of the configuration register.

Figure 11
Clocking of the SBCX in Different Operation Modes



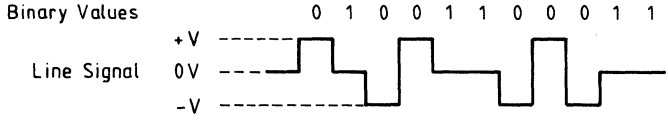
Note 1: Reference clock (1536 kHz), may be used to drive NT2 clock generator.

Interfaces

S/T Interface

According to CCITT recommendation I.430, pseudo-ternary encoding with 100% pulse width is used on the S/T interface. A logical 1 corresponds to a high impedance level (no current), whereas logical 0's are encoded as alternating positive and negative pulses. An example is shown in **figure 12.**

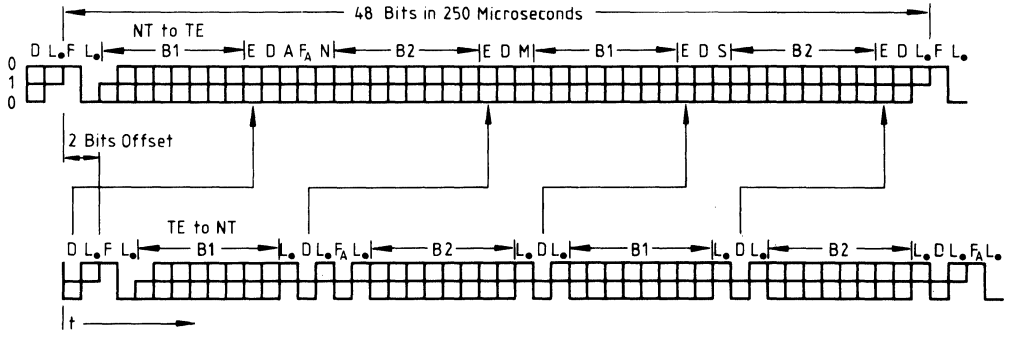
Figure 12
S/T Interface Line Code



One S/T frame consists of 48 bits, at a nominal bit rate of 192 kbit/s. Thus each frame carries two octets of B1, two octets of B2, and four D-bits, according to the B1 + B2 + D structure defined for the ISDN basic access (total useful data rate: 144 kbit/s). Frame begin is marked using a code violation (no mark inversion). The frame structures (from network to subscriber, and subscriber to network) are shown in **figure 13.**

A multi-frame is realized by use of F_A, N, and M bits in the NT to TE direction. **Table 2** shows the S and Q bit positions within the multiframe.

Figure 13
Frame Structure at Reference Points S and T (CCITT I.430)



F = Framing Bit
L = DC Balancing Bit
D = D-Channel Bit
E = D-Echo-Channel Bit
F = Auxiliary Framing Bit or Q-Bit
N = Bit Set to a Binary Value $N = \overline{F_A}$

B1 = Bit within B-Channel 1
B2 = Bit within B-Channel 2
A = Bit Used for Activation
S = S-Channel Bit
M = Multiframing Bit

Note: Dots Demarcate those Parts of the Frame that are Independently DC-Balanced.

Table 2
S and Q Bit Position Identification and Multiframe Structure

Frame Number	NT-to-TE F_A Bit Position	NT-to-TE M Bit	NT-to-TE S Bit	TE-to-NT F_A Bit Position
1	ONE	ONE	SC11	Q1
2	ZERO	ZERO	SC21	ZERO
3	ZERO	ZERO	SC31	ZERO
4	ZERO	ZERO	SC41	ZERO
5	ZERO	ZERO	SC51	ZERO
6	ONE	ZERO	SC12	Q2
7	ZERO	ZERO	SC22	ZERO
8	ZERO	ZERO	SC32	ZERO
9	ZERO	ZERO	SC42	ZERO
10	ZERO	ZERO	SC52	ZERO
11	ONE	ZERO	SC13	Q3
12	ZERO	ZERO	SC23	ZERO
13	ZERO	ZERO	SC33	ZERO
14	ZERO	ZERO	SC43	ZERO
15	ZERO	ZERO	SC53	ZERO
16	ONE	ZERO	SC14	Q4
17	ZERO	ZERO	SC24	ZERO
18	ZERO	ZERO	SC34	ZERO
19	ZERO	ZERO	SC44	ZERO
20	ZERO	ZERO	SC54	ZERO
1	ONE	ONE	SC11	Q1
2	ZERO	ZERO	SC12	ZERO
etc.				

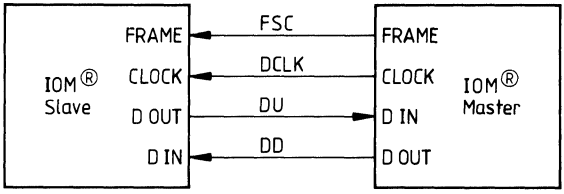
Digital Interface

The PEB 2081 SBCX is provided with a digital (IOM-2) interface, for communication with other ISDN devices to realize OSI layer-1 functions (such as a U transceiver) or upper layer functions (such as ICC, ARCOFI, ITAC and EPIC).

The IOM interface is a four-wire serial interface with: a bit clock, a frame clock, and two data lines per direction **(figure 14)**.

The ISDN user data rate of 144 kbit/s (B1 + B2 + D) is transmitted transparently in both directions over the interface. In addition, it is necessary to interchange control information for activation/deactivation of OSI layer-1 and maintenance functions. This information is transferred using time division multiplexing of the 125 µs S/T interface frame.

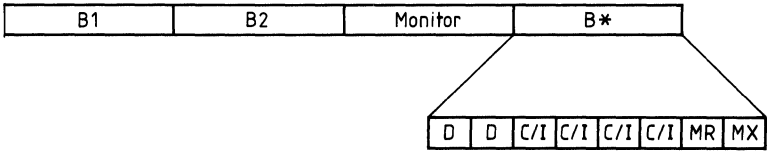
Figure 14
IOM Interface Signals



FSC: Frame synchronization
DCLK: Data clock
DU: Data upstream
DD: Data downstream

The basic frame consists of a total of 32 bits, or four octets: B1 + B2 + D (18 bits) plus 14 overhead bits for maintenance of monitor and control information. The data in both directions is synchronous and in phase **(figure 15)**.

Figure 15
IOM Frame Structure



1st octet B1: B channel (64 kbit/s)
2nd octet B2: B channel (64 kbit/s)
3rd octet: Monitor channel (64 kbit/s), most significant bit first
4th octet B*: 2 bit D channel (16 kbit/s)
4 bit C/I channel
MR, MX bit: used for monitor channel control.

The C/I channel is used for communication between the PEB 2081 SBCX and a processor via a layer-2 device, to control and monitor layer-1 functions. The codes originating from layer-2 devices are called "commands", those from the PEB 2081 SBCX are called "indications". For a list of the C/I codes and their use, refer to the SBCX Tech. Manual.

The monitor channel is used to convey S and Q maintenance bit information and message oriented local functions such as software programming or access to internal registers (e.g. MAI-status).

The PEB 2081 SBCX has implemented the monitor channel protocol according to the IOM-2 specification. It also performs a last look function on the monitor byte and, in transmit direction, a monitor channel access procedure for bus configurations.

For the transfer of S and Q channel information, the PEB 2081 SBCX will autonomously start the monitor channel procedure. Device internal registers are only transferred as a result of a "read" command.

Nominal bit rate of data (IDP1 and IDP0):

256 kbit/sec ...4096 kbit/sec

Nominal frequency of DCLK:

512 kHz ...8192 kHz

Nominal frequency of FSC: 8 kHz

For the exact electrical definition **see page 419** and the IOM-2 interface specification.

Figure 16
Timing of Data and Clocks of the IOM Interface in the 512-kHz-Mode

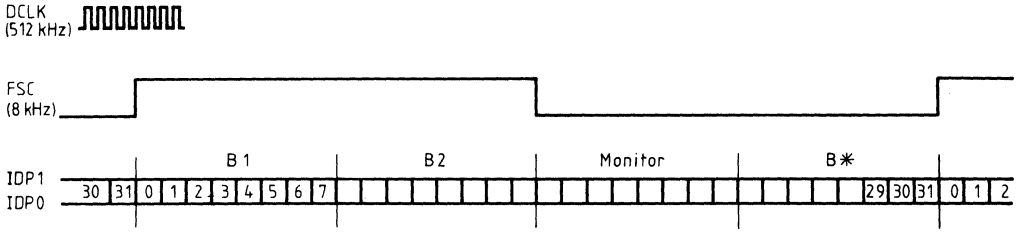


Figure 17
Timing of Data and Clocks of the IOM Interface in the 4096-kHz-Mode

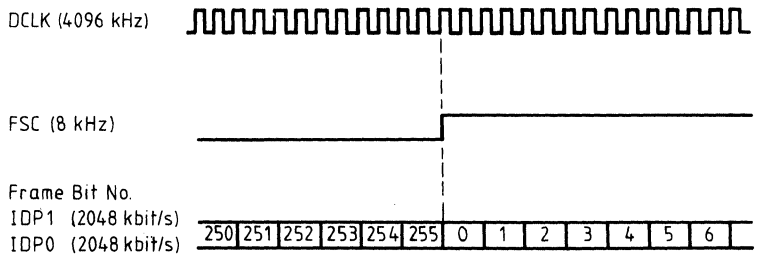
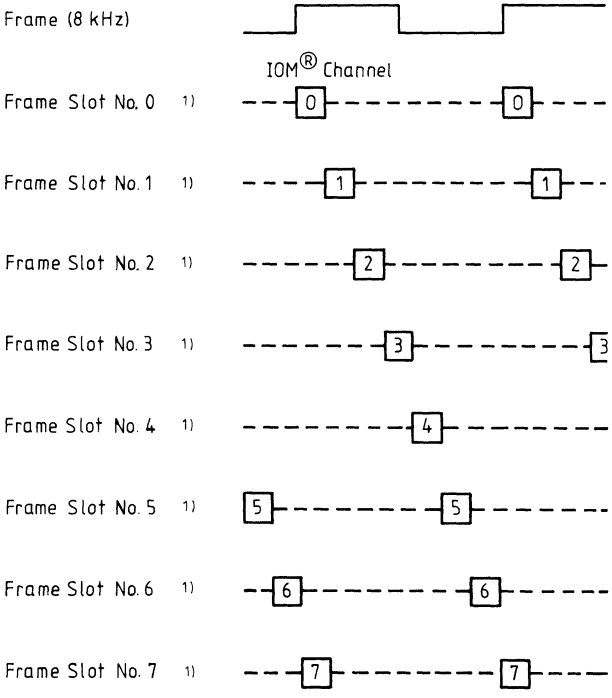


Table 3
Allocation of IOM Channels

IOM Channel No.	ICN2	ICN1	ICN0	Bit No.
0	0	0	0	0... 31
1	0	0	1	32... 63
2	0	1	0	64... 95
3	0	1	1	96...127
4	1	0	0	128...159
5	1	0	1	160...191
6	1	1	0	192...223
7	1	1	1	224...255

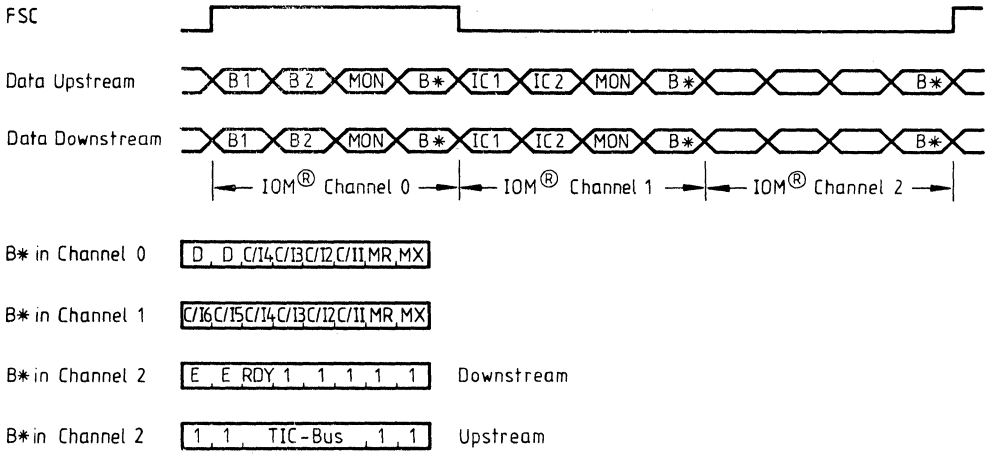
Figure 18
Position of IOM Channels as a Function of Time-Slot Allocation in 4096-kHz-Mode



1) IDP1 (2048 kbit/s)
IDP0 (2048 kbit/s)

In TE mode, the data clock DCLK has a frequency of 1.536 MHz. As a consequence, the IOM interface provides three channels. The PEB 2081 SBCX only uses IOM channel 0, and for D-channel access control, the C/I field of IOM channel 2. The remaining two IOM channels are for the use of other devices within the TE **(figure 19)**.

Figure 19
Definition of the IOM-2 Terminal Interface



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V
Power dissipation	P_D	1	W

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$

All pins except SX1,2; SR1,2; XTAL1,2; V_{DD2}

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V	
L-output voltage (IDP1,0 only)	V_{OL} V_{OL1}		0.45 0.45	V V	$I_{OL} = 2$ mA $I_{OL} = 7$ mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.5 V_{DD} −5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$
Power supply current: operational	I_{CC}		12	mA	$V_{DD} = 5$ V inputs at V_{SS}/V_{DD}
Power supply current: power down			0.8	mA	no output loads
Input leakage current	I_{LI}		10	mA	$0\ V \le V_{IN} \le V_{DD}$
Output leakage current	I_{IO}				$0\ V \le V_{OUT} \le V_{DD}$

DC Characteristics

Pin SX1; SX2

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Absolute value of output pulse amplitude (V_{SX2}–V_{SX1})	V_X V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω[1)] R_L = 400 Ω[1)]
Transmitter output current	I_X	7.5	13.4	mA	R_L = 5.6 Ω[1)]
Transmitter output impedance	Z_X	10 80		kΩ kΩ	inactive or during binary one (V_{DD} = 0...5 V) during binary zero[2)] R_L = 50 Ω

Pin VDD 2

Receiver output voltage	V_R	2.4	2.6	V	$I_O \leq 5$ µA

Pin 5 R; SR 2

Receiver input impedance	Z_R	10 100		kΩ Ω	V_{DD} = 5 V V_{DD} = 0 V

Pin XTAL1

H-input voltage L-input voltage	V_{HI} V_{IL}	3.5 −0.4	V_{DD} +0.4 1.5	V V	

Pin XTAL2

H-output voltage	V_{OH}	4.5		V	I_{OH} = 5 mA, $C_L \leq$ 50 pF
L-output voltage	V_{OL}		0.4	V	I_{OH} = 5 mA, $C_L \leq$ 50 pF

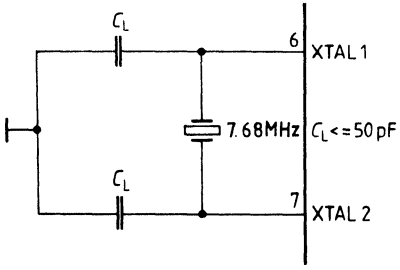
Notes: 1) Due to the transformers, the load resistance as seen by the circuit is four times R_L.
2) 80...100 Ω external resistance required

Capacitances

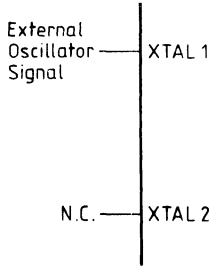
$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$
All pins except SX1,2

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Pin capacitance			7	pF
SX1,2				
Output capacitance against V_{SS}	C_O		10	pF
XTAL1,2				
Load capacitance	C_D		50	pF

Recommended Oscillator Circuits



Crystal Oscillator Mode



Driving from External Source

Clock Signals of the SBCX. Duty Ratios are Indicated High: Low

	Operating Mode			
	TE	**LT-T**	**NT**	**LT-S**
DCLK	o: 1.536 MHz 3:2	i: 512 kHz to 6172 kHz	i: 512 kHz to 6172 kHz	i: 512 kHz to 6172 kHz
FSC	o: 8 kHz 1:2	i: 8 kHz	i: 8 kHz	i: 8 kHz
X3	o: 768 kHz 1:1	o: 1536 MHz 3:2		
X0	o: 32 kHz/16 kHz 1:1			

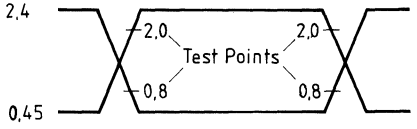
Input and Output Pin Configurations

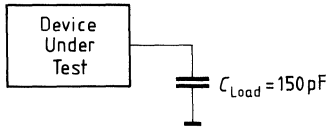
IDP (1:0) are open drain outputs.
CEB is an open drain output/input.
All other output pins are push/pull outputs.

AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".





Jitter

In TE mode, the timing extraction jitter of the PEB 2081 SBCX conforms to CCITT Recommendation I.430 (−7% to +7% of the S/T-interface bit period).

In the NT and LT-S applications, the clock input FSC is used as reference clock to provide the 192-kHz-clock for the S/T interface. In the case of a plesiochronous 7.68-MHz-clock generated by an oscillator, the clock FSC should have a jitter of less than 100 ns peak-to-peak. (In the case of a zero input jitter on FSC, the PEB 2081 SBCX generates 130 ns "self-jitter" on the S/T interface.)

In the case of a synchronous 7.68-MHz-clock (input XTAL1), the PEB 2081 SBCX transfers the input jitter of XTAL1 and FSC to the S/T interface. The maximum jitter of the NT/LT-S output is limited to 260 ns peak-to-peak (CCITT I.430).

Clock Timing

The clocks in the different operating modes are summarized in **table 4**, with duty ratios. The 1.536-MHz-clock is phase-locked to the receive S signal, and is derived using the internal DPLL and the 7.68 MHz ± 100 ppm crystal (TE and LT-T).

As a consequence of this DPLL tracking, the high state of CP may be either reduced or extended by one 7.68-MHz-period (duty ratio 2:2 or 4:2 instead of 3:2). Since X3 and FSC are derived from DCLK (TE mode), the high state or the low state may likewise be reduced or extended by the same amount.

Figure 20
Definition of Clock Period and Width

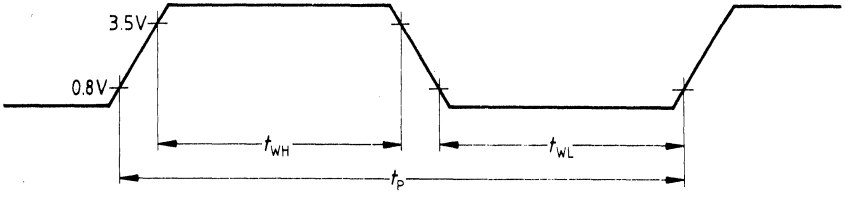


Table 4 to 8 give the timing characteristics of the clocks

Table 4
XTAL1,2

Parameter	Symbol	Limit Values		Unit
		min.	max.	
High phase of crystal/clock	t_{WH}	20		ns
Low phase of crystal/clock	t_{WL}	20		ns
Clock period	t_P	130.08	130.34	ns

Table 5
DCLK

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 1.536 MHz	$t_{P\,O}$	520	651	782	ns	OSC ± 100 ppm
(TE) 1.536 MHz	$t_{WH\,O}$	240	391	541	ns	OSC ± 100 ppm
(TE) 1.536 MHz	$t_{WL\,O}$	240	260	281	ns	OSC ± 100 ppm
(NT, LT-S, LT-T)	$t_{WH\,I}$	90			ns	
(NT, LT-S, LT-T)	$t_{WL\,I}$	90			ns	

Table 6

X3

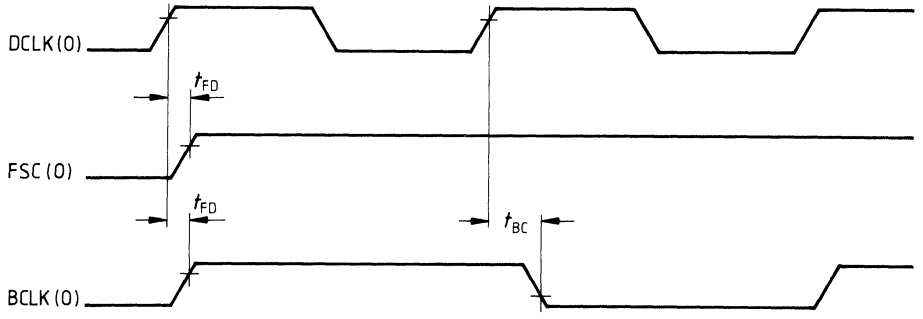
(LT-T) 1536 kHz	$t_{P\,O}$	520	651	782	ns	OSC ± 100 ppm
(LT-T) 1536 kHz	$t_{WH\,O}$	240	391	541	ns	OSC ± 100 ppm
(LT-T) 1536 kHz	$t_{WL\,O}$	240	260	281	ns	OSC ± 100 ppm
(TE) 768 kHz	$t_{P\,O}$	1150	1302	1450	ns	OSC ± 100 ppm
(TE) 768 kHz	$t_{WH\,O}$	520	651	782	ns	OSC ± 100 ppm
(TE) 768 kHz	$t_{WL\,O}$	520	651	782	ns	OSC ± 100 ppm

Table 7

X0

(TE) 32 kHz	$t_{P\,O}$	31.1	31.25	31.4	µs	OSC ± 100 ppm
(TE) 32 kHz	$t_{WH\,O}$	15.4	15.6	15.8	µs	OSC ± 100 ppm
(TE) 32 kHz	$t_{WL\,O}$	15.4	15.6	15.8	µs	OSC ± 100 ppm

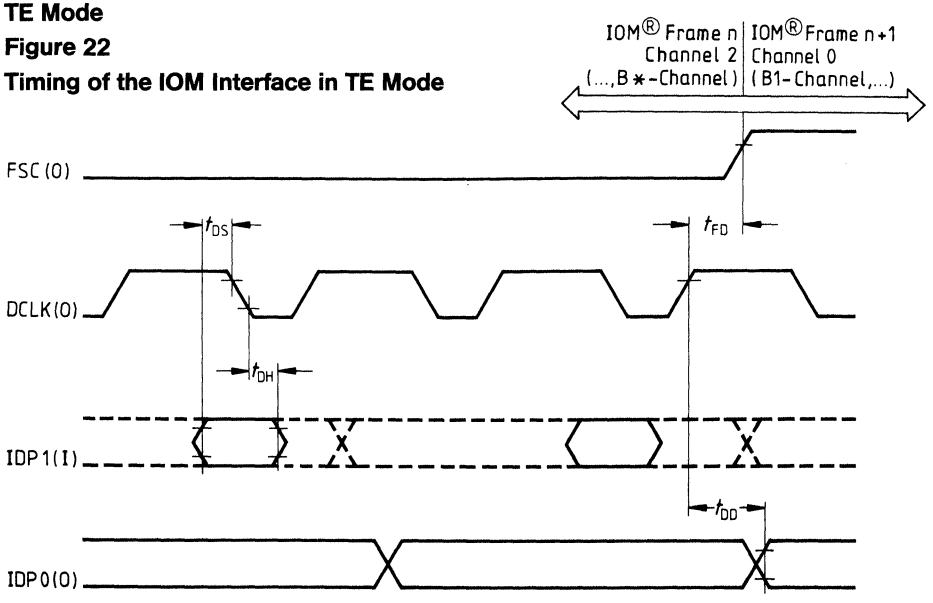
Figure 21
DCLK, BCLK and FSC Relationship in TE Mode



Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Delay DCLK – BCLK	t_{BD}	−200		50	ns	$C_L = 150$ pF
Delay DCLK – FSC	t_{FD}	−200		50	ns	$C_L = 150$ pF

IOM Interface

TE Mode
Figure 22
Timing of the IOM Interface in TE Mode



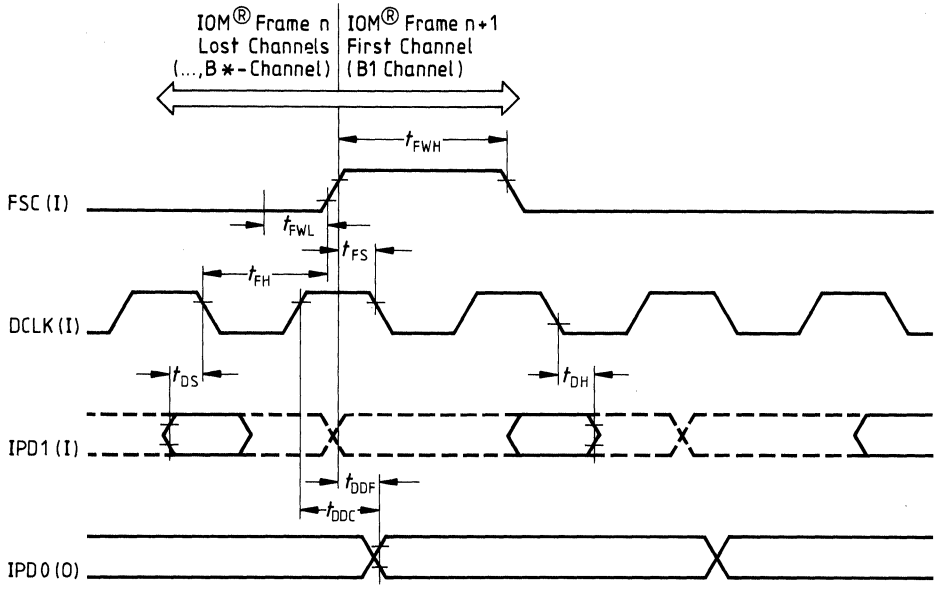
IOM Interface in TE Mode

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Frame sync delay	t_{FD}	−200		−50	ns	C_L = 150 pF
Data delay	t_{DD}			100	ns	C_L = 150 pF
Data setup	t_{DS}	20			ns	
Data hold	t_{DH}	50			ns	

TE Mode

NT, LT-S, and LT-T Modes

Figure 23
Timing of the IOM Interface in NT Mode



IOM Interface in NT Mode

Parameter	Symbol	Limit values			Unit
		min.	typ.	max.	
Frame sync hold	t_{FH}	30			ns
Frame sync setup	t_{FS}	70			ns
Frame sync high	t_{FWH}	130			ns
Frame sync	t_{FWL}	t_{DCL}			
Data delay to clock	t_{DDC}			100	ns
Data delay to frame	t_{DDF}			150	ns
Data setup	t_{DS}	20			ns
Data hold	t_{DH}	50			ns

Timing of Special Function Pins

$\overline{\text{RST}}$ Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Length of active (low) state	t_{WL}	1		µs

CEB Characteristics

The form of the CEB input/output (pin X3, NT and LT-S mode) is given by **figure 27** for the case of two S/T interfaces having a minimum loop delay and a maximum loop delay, respectively.

Figure 24
Star Configuration in NT and LT-S Mode

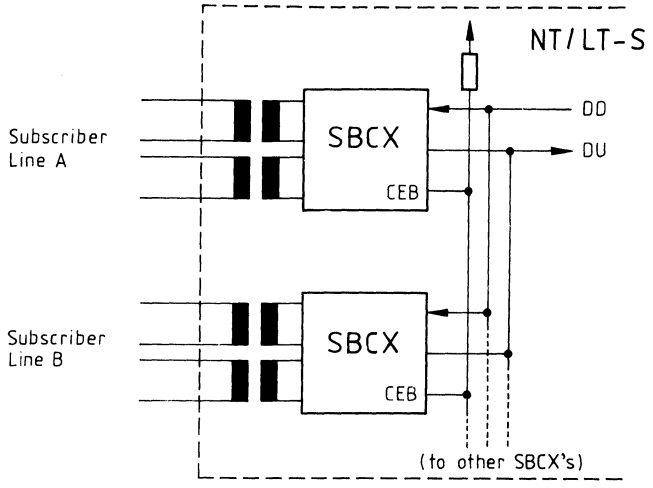


Figure 25
Timing of CEB Output

The AC Characteristics of CEB Output and Input are shown in Figures 5.8-9 and Table 11.

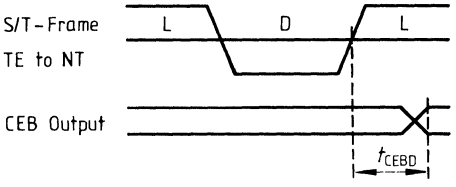


Figure 26
Timing of CEB Input

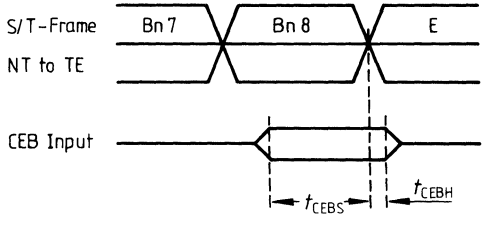
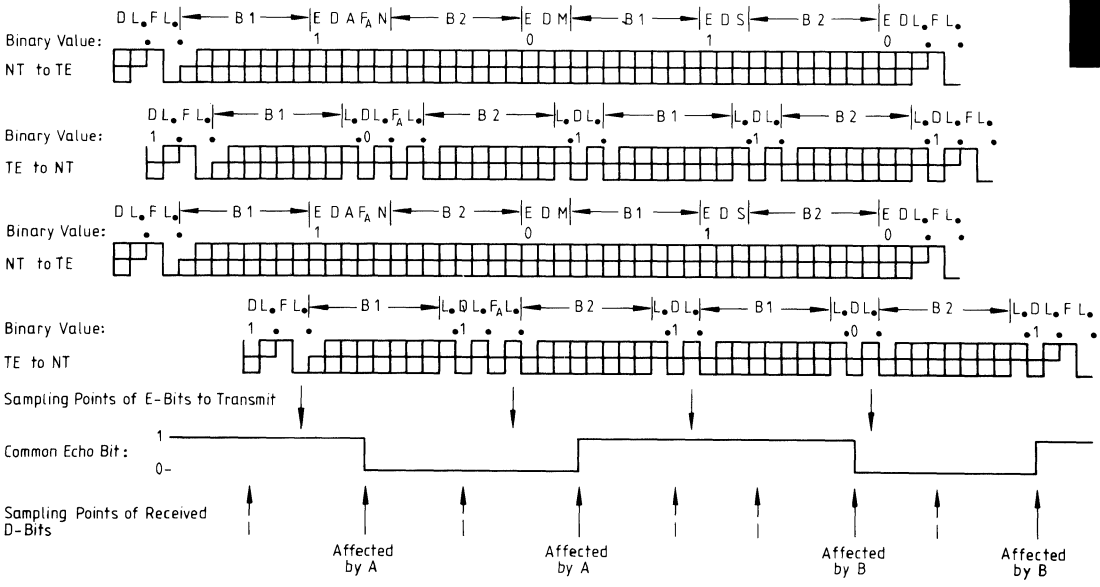


Table 8

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CEB delay	t_{CEBD}	3		5	µs	$C_L = 100$ pF
CEB setup	t_{CEBS}	5			µs	
CEB hold	t_{CEBH}	0			µs	

Figure 27
Timing of CEB



Condition: All Transmit Frames NT ⟶ TE are in Phase.

S/T Interface Transformer

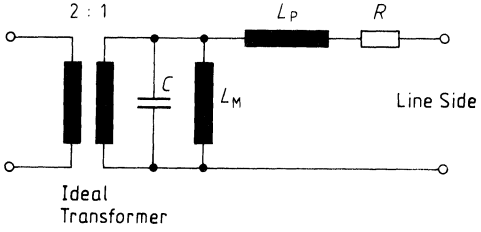
The PEB 2081 SBCX is connected to the 4 wire S/T interface by use of two transformers. Both sides of the transformers must be center tapped.

Transformer Model

The model parameters of the transformer are defined below (all measurements at 10 kHz):

primary to secondary transformer ratio:	1:2 ± 1%
primary total DC resistance:	$R \leq 10\ \Omega$
primary inductance:	$L_M > 20$ mH
primary inductance with secondary short-circuited:	$L_P < 20\ \mu H$
primary capacitance with secondary open:	$C < 40$ pF

Figure 28
Transformer Model



Transmitter Characteristics

The DC characteristics of the transmitter are given in **page 419 and 420.** Rising and falling edges of pulses on 50 Ω load are typically 300 ns.