General Description

The Primary Rate Access Clock Generator and Transceiver PRACT (PEB 22320) is a monolithic CMOS device which implements the analog receive and transmit line interface functions to primary rate PCM carriers. It may be programmed or hard-wired to operate in 1.544-Mbit/s (T1) or 2.048-Mbit/s (CEPT) carrier system.

The PRACT recovers clock and data using an adaptively controlled receiver threshold. It is transparent to ternary codes and shapes the output pulse following the AT&T Technical Advisory #34 or CCITT G.703. The jitter tolerance of the device meets the CCITT (I.431) recommendation and many other specifications by AT&T/Bellcore. An on-chip selectable jitter attenuation is available which meets the I.431 recommendation for CEPT – and the PUB 62411 for T1 application. Diagnostic facilities are included.

Specially designed line interface circuits simplify the tedious task of protecting the device against overvoltage damage while still meeting the return loss requirements.

The PRACT is suitable for use in a wide range of voice and data applications such as for connections of digital switches and PBXs to host computers for implementations of primary ISDN subscriber loops as well as for terminal applications. The maximum range is determined by the maximum allowable attenuations.

In the T1 case the PRACT's power consumption is mainly determined by the line length and type of the cable.

Type	Package
PEB 22320-N	P-LCC-44-1 (SMD)

Features

- ISDN-line interface for 1544 and 2048 kbit/s (T1 and CEPT)
- Data and clock recovery
- Transparent to ternary codes
- Low transmitter output impedance for a high return loss with reasonable protection resistors (CCITT G.703 requirements for the line input return loss fulfilled)
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 applications
- Jitter specifications of CCITT I.431 and many AT&T/Bellcore publications met
- Wander and jitter attenuation
- Jitter tolerance of receiver: 0.5 UI s
- Implements local and remote loops for diagnostic purposes
- Monolithic line driver for a minimum of external components
- Low power, reliable CMOS technology
- Loss of signal indication for receiver
- Clock generator for system clocks

Block Diagram