SIEMENS

Memory Time Switch Small (MTSS)

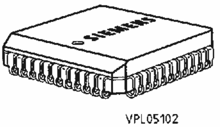
PEB 2046
PEF 2046

Preliminary Data

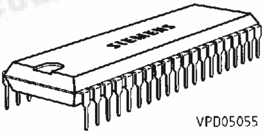
CMOS IC

1 Features

- Time/space switch for 2048-kbit/s PCM systems
- Switching of up to 256 incoming PCM channels to up to 256 outgoing PCM channels
- 8-input and 8-output PCM lines
- Configurable for a 4096- and 8192-kHz device clock
- Tristate function for further expansion and tandem operation
- 8-bit µP interface
- Single + 5 V power supply
- Advanced low power CMOS technology



P-LCC-44

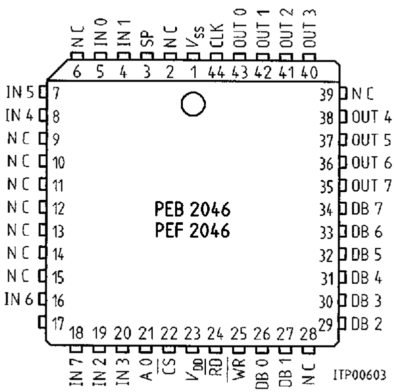


P-DIP-40

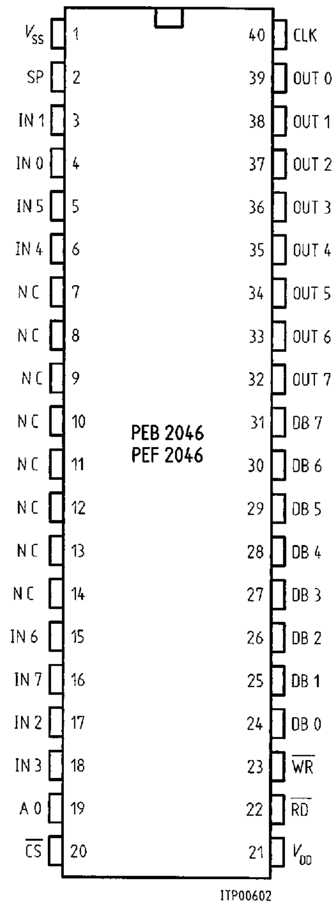
Type	Ordering Code	Package
PEB 2046-N	Q67100-H6104	P-LCC-44 (SMD)
PEB 2046-P	Q67100-H6105	P-DIP-40
PEF 2046-N	Q67100-H6107	P-LCC-44 (SMD)
PEF 2046-P	Q67100-H6108	P-DIP-40

Pin Configurations
(top view)

P-LCC-44



P-DIP-40



1.1 Pin Definitions and Functions

Pin No. P-LCC	Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
1	1	V_{SS}	I	**Ground** (OV)
3	2	SP	I	**Synchronization Pulse:** The PEx 2046 is synchronized relative to the PCM system via this line.
4 5 7 8 17 18 19 20	3 4 5 6 15 16 17 18	IN1 IN0 IN5 IN4 IN6 IN7 IN2 IN3	I I I I I I I I	**PCM-Input Ports:** Serial data is received at these lines at standard TTL levels.
21	19	A0	I	**Address 0:** When high, the indirect register access mechanism is enabled. If A0 is logical 0 the mode and status registers can be written to and read respectively.
22	20	$\overline{\text{CS}}$	I	**Chip Select:** A low level selects the PEx 2046 for a register access operation.
23	21	V_{DD}	I	**Supply Voltage:** 5 V ± 5 %.
24	22	$\overline{\text{RD}}$	I	**Read:** This signal indicates a read operation and is internally sampled only if $\overline{\text{CS}}$ is active. The MTSS puts data from the selected internal register on the data bus with the falling edge of $\overline{\text{RD}}$. $\overline{\text{RD}}$ is active low.
25	23	$\overline{\text{WR}}$	I	**Write:** This signal initiates a write operation. The $\overline{\text{WR}}$ input is internally sampled only if $\overline{\text{CS}}$ is active. In this case the MTSS loads an internal register with data from the data bus at the rising edge of $\overline{\text{WR}}$. $\overline{\text{WR}}$ is active low.
26 27 29 30 31 32 33 34	24 25 26 27 28 29 30 31	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	I/O I/O I/O I/O I/O I/O I/O I/O	**Data Bus:** The data bus is used for communication between the MTSS and a processor.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
35	32	OUT7	O	**PCM-Output Port:** Serial data is sent by these lines at standard CMOS or TTL levels. These pins can be tristated.
36	33	OUT6	O	
37	34	OUT5	O	
38	35	OUT4	O	
40	36	OUT3	O	
41	37	OUT2	O	
42	38	OUT1	O	
43	39	OUT0	O	
44	40	CLK	I	**Clock:** 4096- or 8192-kHz device clock.

1.2 Functional Symbol

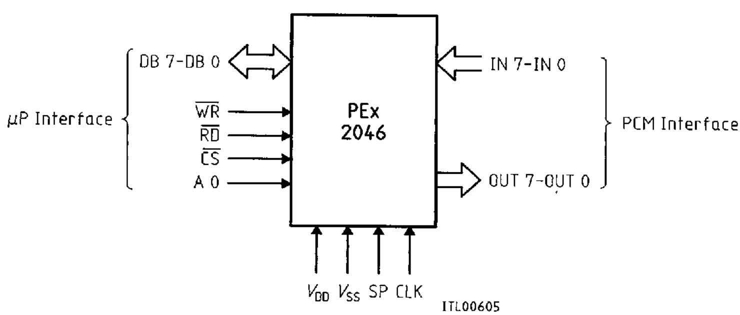


Figure 1
Functional Symbol for the Standard Configuration

1.3 Device Overview

The Siemens Memory Time Switch PEx 2046 is a monolithic CMOS circuit connecting any of 256 incoming PCM channels to any of 256 outgoing PCM channels. The on-chip connection memory is accessed via the 8-bit µP interface.

The PEx 2046 is fabricated using the advanced CMOS technology from Siemens and is mounted in a P-DIP-40 or a P-LCC-44 package. Inputs and outputs are TTL-compatible.

2 Functional Description

The PEx 2046 is a memory time switch device. It can connect any of 256 PCM input channels to any of 256 output channels.

The input information of a complete frame is stored in the on-chip 4-Kbit speech memory SM (**see figure 2**). The incoming 256 channels of 8 bits each are written in sequence into fixed positions in the SM. This is controlled by the input counter in the timing control block with a 8-kHz repetition rate.

For outputting, the connection memory (CM) is read in sequence. Each location in CM points to a location in the speech memory. The byte in this speech memory location is read into the current output time-slot. The read access of the CM is controlled by the output counter which also resides in the timing control block.

Hence the CM needs to be programmed beforehand for the desired connection. The CM address corresponds to one particular output time-slot and line number. The contents of this CM-address points to a particular input time-slot and line number (now resident in the SM).

In the following chapters the functions of the PEx 2046 will be covered in more detail.

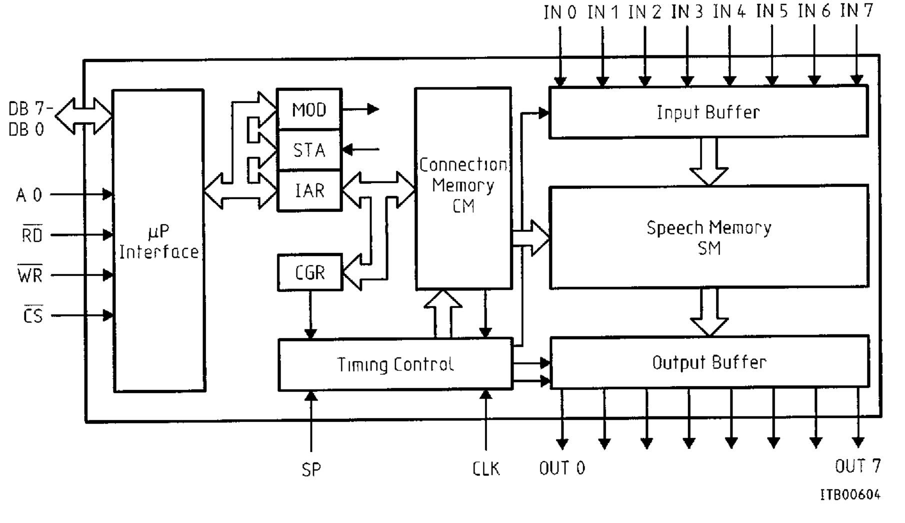


Figure 2
Block Diagram of the PEx 2046

2.1 Basic Functional Principles

Preparation of the Input Data

The PEx 2046 works in 2048-kbit/s PCM systems. The frame frequency is 8000 Hz. Therefore a frame consists of 32 time-slots of 1 byte each. In order to fill the speech memory, which has a fixed capacity of 256 channels, 8 input lines are necessary.

The PEx 2046 runs with either a 4096- or a 8192-kHz device clock as selected with CFG:CPS.

The preparation of the input data is made in the input buffer. It converts the serial data of a time-slot to parallel form.

In standard configuration time-slot 0 begins with the rising edge of the SP pulse as shown in **figure 3.**

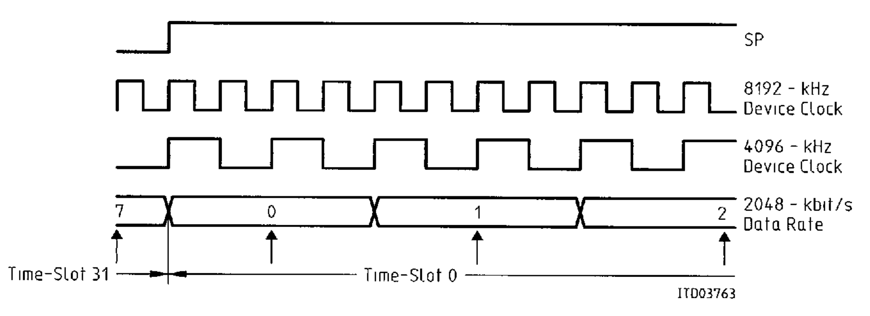


Figure 3
Latching Instant for Input Data

As can be seen there the beginning of a input time-slot is defined such, that the input lines have settled to a stable value, when the datum is actually sampled.

2048-kbit/s data is sampled after 3/4 of the according bit period, i.e. with the rising edge of the 4^{th} 8192-kHz clock cycle or the falling edge of the 2^{nd} 4096-kHz clock cycle of the considered bit period.

Speech Memory

The prepared input data is written into the speech memory SM. It has a capacity of 256 bytes to store one frame of all active input lines. The destination SM addresses are supplied by the input counter, which resides in the timing control block. They ensure that a certain input channel is always written to the same physical speech memory location. The input counter is synchronized with the rising edge of the SP signal.

The 9-bit addresses to read the speech memory are supplied by the connection memory. These are programmable and need not follow any recognizable sequence.

Write and read accesses of the SM occur alternately.

Connection Memory

The connection memory (CM) is a RAM organized as 256 × 10 bits. It contains the 9-bit speech memory address and a validity bit for the 256 possible output channels. While the speech memory address points to a location in the SM, the validity bit is processed in the timing control block: If the TE bit in the mode register (**see chapter 4.1**) is set to logical 0, the validity bit is directly forwarded to the output buffer as the tristate control signal. Otherwise (if TE = high), an all-zero speech memory address causes the output for the associated channel to be tristate. In this case the all-zero speech memory address (time-slot 0 on output line 0) cannot be used for switching purposes.

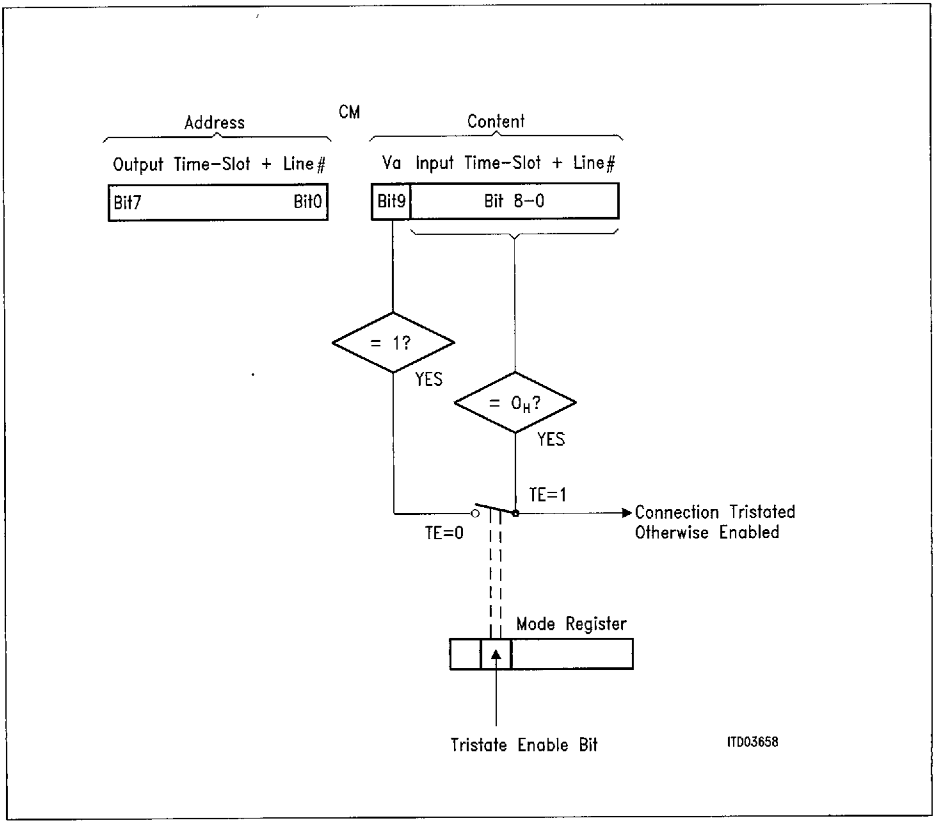


Figure 4
The Influence of the Connection Memory on the Output Validity

The CM is written via the µP interface using the indirect register access scheme (**see section Indirect Register Access**). It is read using addresses supplied by the output counter which resides in the timing control block. The output counter generates addresses that form an enumerative sequence. Thus the connection memory is read cyclically and establishes the correct time-slot sequence of the outputs.

The output counter is synchronized with the falling and rising edge of the SP signal in standard and primary access configurations, respectively.

The connection memory addresses and data encode the number of the output and input channels, respectively. For a detailed description of the code please refer to **section Indirect Register Access and Connection Memory Access.**

Output Buffer

The output buffer rearranges the data read from the speech memory. It basically converts the parallel data to serial data. Depending on the tristate control signal from the timing control block the output buffer outputs the data or switches the line to high impedance.

Figure 5 shows, when the single bits are output. They are clocked off at the rising clock edge at the beginning of the considered bit period. Time-slot 0 starts two t_{CP8} before the falling edge of the SP pulse.

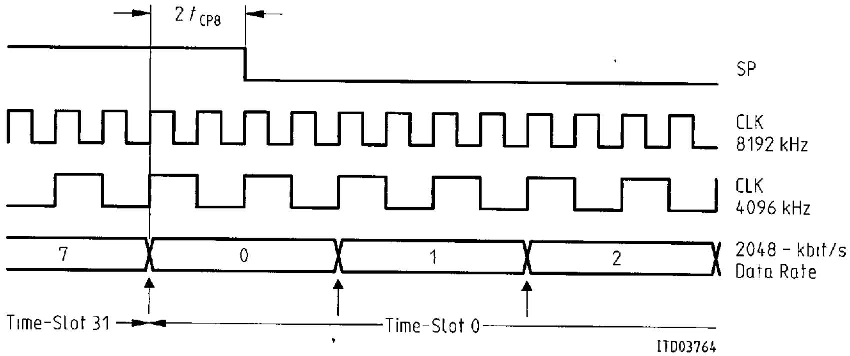


Figure 5
Clocking Off Instant Output Data

2.2 Microprocessor Interface and Registers

The PEx 2046 is programmed via the µP interface. It consists of the data bus DB7 … DB0, the address bit A0, the Write ($\overline{WR}$), the Read ($\overline{RD}$) and Chip Select ($\overline{CS}$) signal, as shown in **figure 6.**

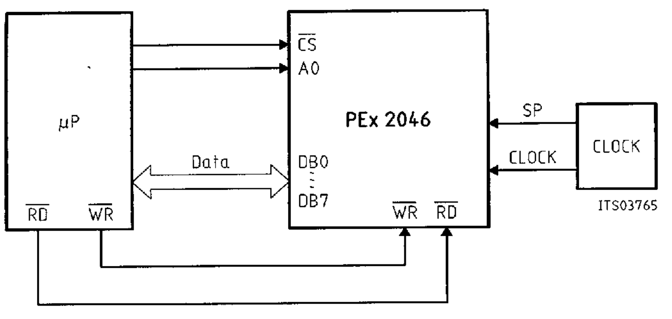


Figure 6
The PEx 2046 Controlled by a Microprocessor

To perform any register access, CS has to be zero. This pin is provided, so that a single chip can be activated in an environment where one microprocessor controls many slave processors (**see figure 11**).

The PEx 2046 incorporates 3 user programmable registers,

- the mode register (MOD)
- the status register (STA)
- the configuration register (CFR) and

as well as

- the connection memory (CM).

The mode register is a write only register; the status register is a read only register. CFR and CM can be read and written. The single address bit A0 does not offer enough address space to encode all access possibilities. Therefore the indirect access scheme is used to access the CFR and CM. It uses the indirect access register (IAR), which is provided on chip.

Using the 3 signals A0, $\overline{WR}$ and $\overline{RD}$ the IAR, MOD and STA registers can be identified according to **table 1**.

Table 1
Addressing of the Direct Registers

A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The A0 address distinguishes between the IAR and the directly accessible registers. The $\overline{WR}$ and $\overline{RD}$ strobes combined with an A0 equal to logical 0 identify the mode- and status registers, respectively. The data bus contains the associated information. In the following paragraphs the indirect register access and the register contents will be described.

Indirect Register Access (A0 = 1)

To perform an indirect register access 3 consecutive instructions have to be programmed. One indirect register access has to be completed before the next one can begin. The 3 instructions of the indirect access operate on the indirect access register. It receives, in sequence the control byte, the data byte and the address byte according to **table 2**.

Table 2
IAR Byte Structure

Bit 7							Bit 0	
0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The data byte contains the information which shall be written into the connection memory or the indirect registers, i.e. the CSR or the CFR. The address byte indicates which one of the indirect registers shall be accessed or in which location of the CM the data shall be written. The control byte determines whether the connection memory or one of the indirect registers shall be accessed and whether a write or read operation shall be performed.

Before an indirect access is started, the Z- and B bits of the status register must be 0. With the first instruction the Z bit is set (**see chapter 4.2**). After the third instruction the PEx 2046 accesses the physical register or memory location. This access requires maximally 900 ns. After the access finishes the Z bit is reset. The 3 instructions are separated by intervals where both $\overline{WR}$ and $\overline{RD}$ are in a high state.

Figure 7 illustrates a write operation on the IAR.

It is possible to read or write the direct access registers (i.e. the mode or status register) while an indirect access is in progress. Thus the status register may be read in the time intervals that separate the three sequential indirect access instructions. Also, the current indirect access may be aborted by setting the MOD:RI.

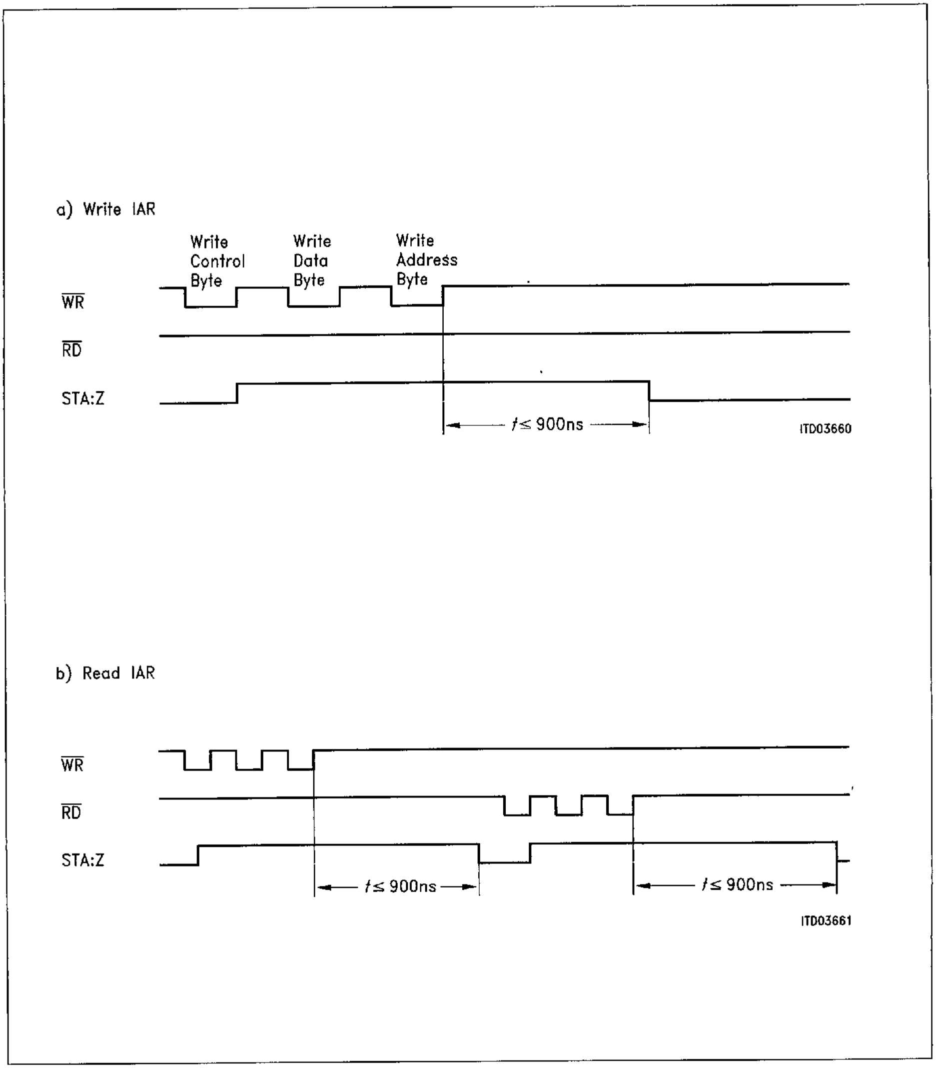


Figure 7
Timing Diagrams for IAR

Bits K1 and K0 of the control byte determine whether a CM or an indirect register access shall be performed. When K1 and K0 are both logical 1, one of the indirect registers is accessed. For all other combinations the connection memory is accessed.

Table 3
Decoding the K1 and K0 Bits

K1	K0	Accessed Register	R/W
0	0	CM	R
0	1	CM	W
1	0	CM	W
1	1	indirect register	R or W

In the case of a CM access the K1 and K0 bits also indicate the type of the access: One bit being logical 0 a read operation.

The same distinction function is performed by bit C0 of the control byte in the case of an indirect register access. According to **table 5** a high on C0 initiates a read, a low write operation. The value of the C1 bit is of no significance in this application. However to avoid future incompatibility problems, it is strongly recommended to set C1 to logical 0.

Table 4
Addressing of the Indirect Registers

K1	K0	C0	Address Byte (hex)	Access
1	1	1	FE	CFR read
1	1	0	FE	CFR write

The address byte holds the CM address for a connection memory access, for indirect register access it indicates which one of the two indirect registers is accessed. A hexadecimal FE_H addresses the configuration register. **Table 4** lists all possible choices of indirect register accesses.

The data to be written to the different registers or the CM reside in the data byte. For CM accesses not 8 but 10 bits are written into the selected location. The two bits in excess come from the C0 and C1 bits of the control byte and are interpreted as the most significant bits of the data word. (D9 and D8). Accordingly the 3 CM-access instructions are interpreted as shown in **table 5.**

Table 5
CM Access IA Byte Structure

Bit 7							Bit 0	
0	0	K1	K0	0	0	D9	D8	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The following example illustrate how an indirect memory access works.

The instruction sequence

00110000

11111111 $A0 = 1, \overline{WR} = 0, \overline{RD} = 1, \overline{CS} = 0$

11111110

writes the hexadecimal value FF_H into the configuration register.

The instruction sequence

00010010

00000000 $A0 = 1, \overline{WR} = 0, \overline{RD} = 1, \overline{CS} = 0$

10101010

writes the hexadecimal value 200_H into the connection memory location AA_H thus tristating the output.

To read the indirect registers or the CM two sequences of 3 instructions each have to be programmed.

In the first sequence the PEx 2046 is instructed which register or CM address to read. The data transferred to the PEx 2046 in this first sequence is of no importance.

With the first write instruction STA:Z is set.

After the first 3 instructions the PEx 2046 needs 900 ns to read the specified location and to write the result to the IAR. It overwrites the data byte and in the case of a CM-read operation additionally bits 1 and 0 of the control byte. The status register bit Z is reset after maximally 900 ns. Then 3 read operations follow. Again, STA:Z is set with the first read instruction. The 3 instructions read 3 bytes from the IAR. **Figure 7** shows this procedure. The data byte and, in the case of a CM-read operation, the C1 and C0 bits in the control byte show the values read from the indirect registers or the CM. The K0, K1 bits and the address byte have not changed their values since the proceeding write instruction sequence.

After the third read operation the PEx 2046 needs another 900 ns to reset the indirect access mechanism and the Z-bit in the status register.

With the following instruction sequence

00000001

11111111 $A0 = 1, \overline{WR} = 0, \overline{RD} = 1, \overline{CS} = 0$

10101010

the byte sequence

11001110

00000000 $A0 = 1, \overline{WR} = 1, \overline{RD} = 0, \overline{CS} = 0$

10101010

can be read.

The CM-location AA_H, which has been written to 200_H in the last example is read again.

Bits 7, 6, 3, 2, of the control byte showing logical 0 in the first byte at the beginning of the read access reappear as logical 1 in the fourth byte. This is due to the internal device architecture. These bits are unused and are recommended to be set to logical 0 to avoid future incompatibility problems.

In CFR-read accesses, bit 1 and bit 0 (C1 and C0) of the read control byte have a value of logical 1.

Register Contents

You will find a detailed description of the different register contents in **section 4**. This paragraph only gives a short overview of the different registers:

The mode register contains bits to determine the output tristating scheme, to control the CM-reset mechanism, to interrupt the indirect access mechanism and to switch the chip to standby.

The status register consists of 3 bits. They tell whether the PEx 2046 is busy resetting its connection memory or performing an indirect access or whether operational conditions have occurred which might lead to a partial or complete loss of data in the connection and speech memory. Bits 4 to 0 of the status register default to logical 0.

The configuration register is used to select the device clock frequency. The most significant 7 bits default to logical 1, if the register is read.

The connection memory content and address contain the connection information. Specifics are explained in the following sections.

2.3 Standard Configuration

In this application 256 channels per frame are written into the speech memory. Each one of them can be connected to any output channel.

According to **table 8** and depending on the selected mode the least significant bits of the connection memory address and data contain the logical pin numbers, the most significant bits the time-slot number of the output and input channels.

The following example explains the programming sequence.

Time-slot 7 of the incoming 2048-kbit/s input line IN2 shall be connected to time-slot 6 of the output line OUT 5 of an 2048-kbit/s system.

Therefore the following byte sequence on the data bus has to be used to program the CM properly:

00010000

01110010

00110101

The frame, for all input channels, starts with the rising edge of the SP signal. The frame for all output channels begins two t_{CP8} (with 8192-kHz device clock) or one t_{CP4} period (4096-kHz device clock) before the falling SP edge. The period of time between the rising and falling edge of the SP pulse should be

$$t_{SPH} = (2 + N \times 4)\, t_{CP8} \qquad (0 \leq N \leq 255)$$
$$= (1 + N \times 2)\, t_{CP4}$$

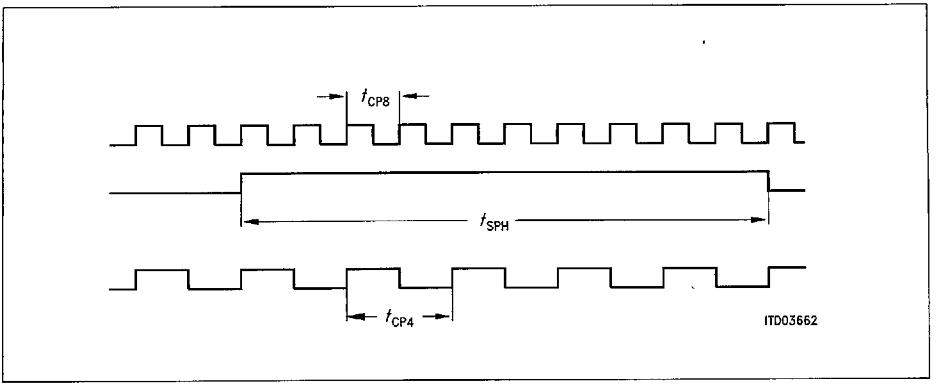


Figure 8
SYP Duration for N = 2

N is an user defined integer. By varying N, t_{SPH} can be varied in 2048-kHz clock period steps. For an example using N = 2 refer to **figure 8**.

The device is synchronized after 3 SP pulses (**see chapter 3.2**).

3 Operational Description

3.1 Power Up

Upon power up the PEx 2046 is set to its initial state. The mode and configuration register bits are all set to logical 1. The status register B bit is undefined, the Z bit contains logical 0, the R bit is undefined.

This state is also reached by pulling the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to logical 0 at the same time (software reset). For the software reset the state of $\overline{\text{CS}}$ is of no significance.

3.2 Initialization Procedure

After power up a few internal signals and clocks need to be initialized. This is done with the initialization sequence. To give all signals and clocks a defined value the MTSS must encounter 3 falling and 2 rising edges of the SP signal. The resulting SP pulses may be of any length allowed in normal operation, the time interval between the two SP pulses may be of any length down to 250 ns.

With all signals being defined, the CM needs to be reset. To do that a logical 0 is written into MOD:RC. STA:B is set. The resulting CM reset is finished after at most 250 µs and is indicated by the status register B-bit being logical 0. Changing the pulse shaping factor N during CM reset may result in a CM-reset time longer than 250 µs.

To prepare the PEx 2046 for programming the CM, the RI bit in the mode register must be reset. Note that one mode register access can serve to reset both RC- and RI bits as well as configuring to chip (i.e. selecting operating mode etc.).

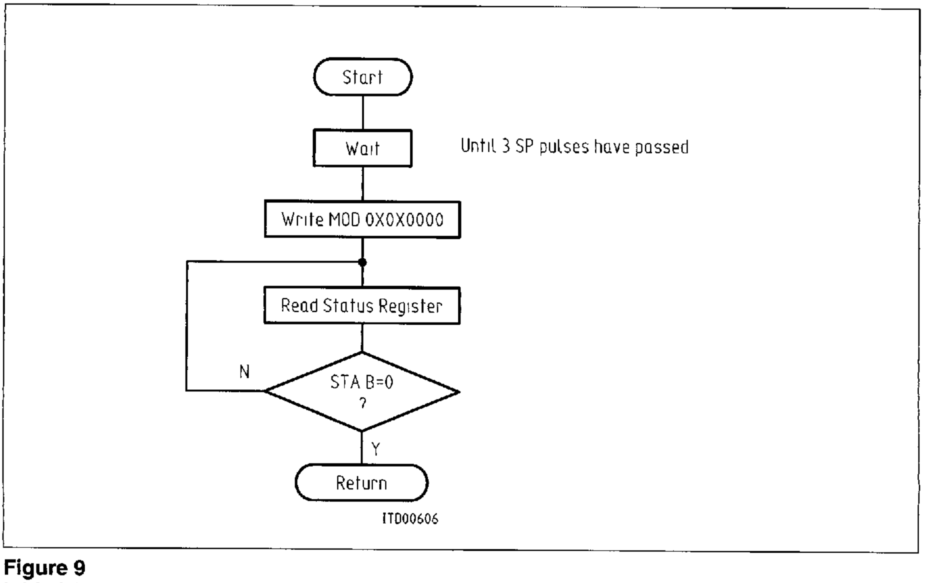


Figure 9
Initializing the PEx 2046 for a 8192-kHz Device Clock

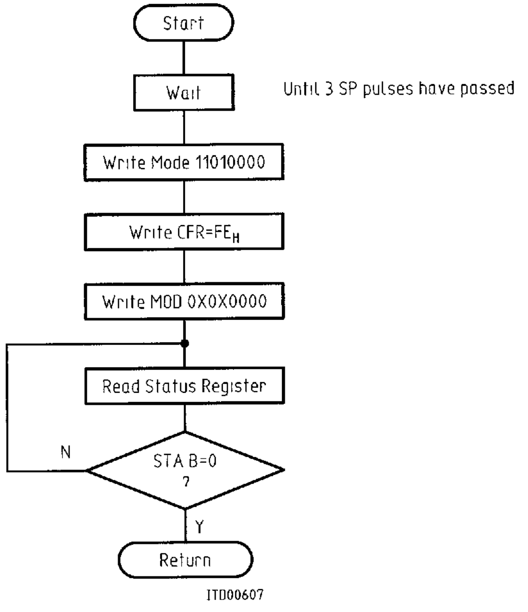


Figure 10
Initializing the PEx 2046 for a 4096-kHz Device Clock

3.3 Operation with a 4096-kHz Device Clock

In order for the MTSS to operate with a 4096-kHz device clock the CPS bit in the CFR register needs to be reset. This has to be done before the CM reset and needs up to 1.8 µs. Please keep in mind, MOD:RI has to be reset prior to performing an indirect register access. For a flow chart of this process refer to **figure 9**.

3.4 Standby Mode

With MOD:SB being logical 1 the PEx 2046 works as a backup device in redundant systems. It can be accessed via the µP interface and works internally like an active device. However, the outputs are high impedance. If the SB bit is reset the outputs are switched to low impedance for the programmed active channels and this MTSS can take over from another device which has been recognized as being faulty. **(See figure 10)**

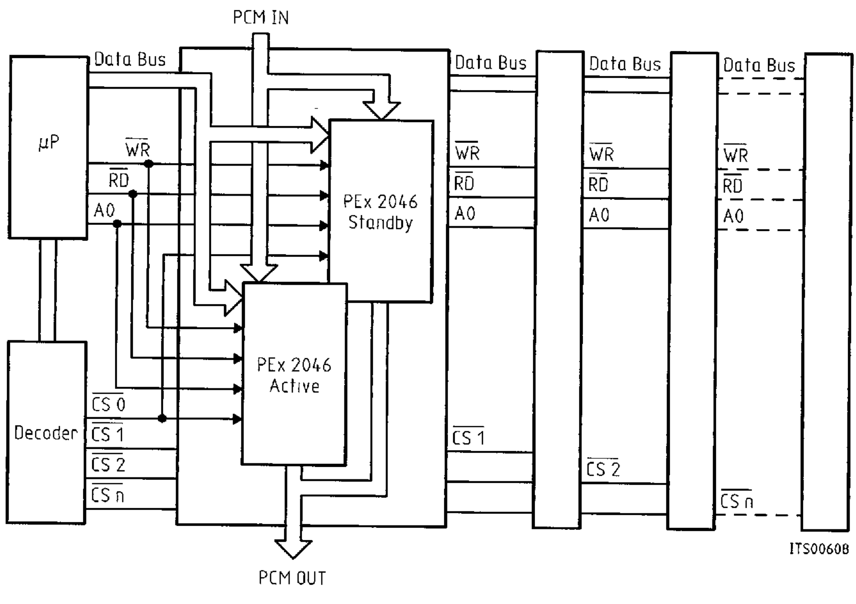


Figure 11
Device Setup in Redundant Systems

4 Detailed Register Description

The following registers may be accessed:

Table 6
Addressing the Direct Registers

Address A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The chapters in this section cover the registers in detail.

4.1 Mode Register (MOD)

Access: Write on address 0

DB 7 … DB 0

RC	TE	RI	SB	0	0	0	0

Value after power up: FF_H

RC **Reset Connection** memory; writing a zero to this bit causes the complete connection memory to be overwritten with 200_H (tristate). During this time STA:B is set. The maximum time for resetting the connection memory is 250 µs.

TE **Tristate Enable**; this bit determines which tristating scheme is activated:

TE = 1: If the speech memory address written into the connection memory is S8 – S0 = 0, the output channel is tristated.

TE = 0: The S9 bit written into the connection memory is interpreted as a validity bit: S9 = 0 enables the programmed connection, S9 = 1 tristates the output.

Note: If TE = 1, time-slot 0 of the logical input line 0 cannot be used for switching.

RI **Reset Indirect** access mechanism; setting this bit resets the indirect access mechanism. RI has to be cleared before writing/reading IAR after reset.

SB **Stand By**; by selecting SB = 1 all outputs are tristated. The connection memory works normally. The PEx 2046 can be activated immediately by resetting SB.

Table 7
Input and Output Pin Arrangement

Input Pin Arrangement			Output Pin Arrangement		
Pin No.		8 × 2 Mbit/s	Pin No.		8 × 2 Mbit/s
P-LCC	P-DIP		P-LCC	P-DIP	
4	3	IN1	35	32	OUT7
5	4	IN0	36	33	OUT6
7	5	IN5	37	34	OUT5
8	6	IN4	38	35	OUT4
17	15	IN6	40	36	OUT3
18	16	IN7	41	37	OUT2
19	17	IN2	42	38	OUT1
20	18	IN3	43	39	OUT0

4.2 Status Register (STA)

Access: Read at address 0

DB 7							DB 0
B	**Z**	**R**	**0**	**0**	**0**	**0**	**0**

B **Busy:** The chip is busy resetting the connection memory (B = 1). B is undefined after power up and logical 0 after the device initialization.

Note: The maximum time for resetting the connection memory is 250 µs.

Z Incomplete instruction; a three byte indirect instruction is not completed (Z = 1). Z is 0 after power up.

Note: Z is reset and the indirect access is cancelled by setting MOD:RI or resetting MOD:RC.

R Initialization **Request**. The connection memory has to be reset due to loss of data (R = 1). The R bit is set after power failure or inappropriate clocking and reset when the connection memory reset is finished. R is undefined after power up and logical 0 after the device initialization.

4.3 Indirect Access Register (IAR)

(Read or Write Operation with Address A0 = 1)

An indirect access is performed by reading/writing three consecutive bytes (first byte = control byte, second byte = data byte, third byte = address byte) to/from IAR. The structure is shown in **table 8**.

Table 8
The 3 Bytes of the Indirect Access

Bit 7							Bit 0	
0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The control byte bits K1, K0, C1 and C0 together with the address byte determine the type of access being performed according to **table 9.**

Table 9
Encoding the Different Types of Indirect Accesses

K1	K0	C1	C0	Address Byte	Type of Access
0	0	D9	D8	CM Address	Read CM
1	0	D9	D8	CM Address	Write CM
0	1	D9	D8	CM Address	Write CM
1	1	0	0	FE_H	Write CFR
1	1	0	1	FE_H	Read CFR

Connection Memory Access

For a connection memory access the control byte bits C1 and C0 contain the data bits D9 and D8, respectively. D9 is the validity bit which together with D8 and the data byte D7 – D0 is written to the CM address IA7 – IA0.

The function of the validity bit is controlled by STA:TE. D8 – D0 and IA7 – IA0 contain the information for the logical line and time-slot numbers of the programmed connection, D8 – D0 for the inputs, IA7 – IA0 for the outputs. **Table 10** shows the programming of these bits.

Standard Configuration

Table 10
Time-Slot and Line Programming

2-Mbit/s input lines	Bit	D3	to	D0	Line number
	Bit	D8	to	D4	Time-slot number
	Bit	D9			Validity bit
2-Mbit/s output lines	Bit	IA2	to	IA0	Line number
	Bit	IA7	to	IA0	Time-slot number

The pulse shape factor N may take any integer value from 0 to 255.

Configuration Register Access (CFR)

Access: Read or write indirect address FE_H

For a read access the bit 0 of the control byte must be set to logical 1 and for a write access to logical 0.

Value after power up or software reset: FF_H

DB 7							DB 0
1	1	1	1	1	1	1	CPS

CPS … **Clock Period Select:** Device clock is set to 8192 kHz (logical 1) or 4096 kHz (logical 0).

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEB 2046	T_A	0 to 70	°C
Storage temperature PEB 2046	T_{stg}	– 65 to 125	°C
Ambient temperature under bias PEF 2046	T_A	– 40 to 85	°C
Storage temperature PEF 2046	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V

DC Characteristics

Ambient temperature under bias range; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V.

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	– 0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} + 0.4	V	
L-output voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA
Operational power supply current	I_{CC}		10	mA	V_{DD} = 5 V, inputs at 0 V or V_{DD}, no output loads
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

T_A = 25 °C, V_{DD} = 5 V ± 5 %, V_{SS} = 0 V.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
I/O capacitance	C_{IO}		20	pF
Output capacitance	C_{OUT}		15	pF

AC Characteristics

Ambient temperature under bias range, V_{DD} = 5 V ± 5 %.

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

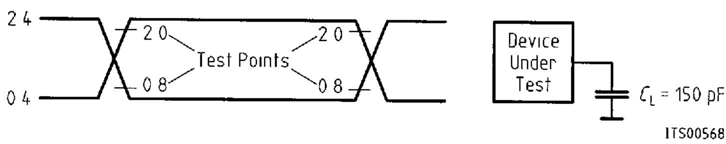


Figure 12
I/O Waveform for AC Tests

µP-Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address stable before $\overline{RD}$	t_{AR}	0		ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ width	t_{RR}	90		ns
$\overline{RD}$ to data valid	t_{RD}		90	ns
Address stable to data valid	t_{AD}		90	ns
Data float after $\overline{RD}$	t_{DF}	5	25	ns
Read cycle time	t_{RCY}	160		ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold time	t_{WA}	0		ns
$\overline{WR}$ width	t_{WW}	60		ns
Data setup time	t_{DW}	5		ns
Data hold time	t_{WD}	15		ns
Write cycle time	t_{WCY}	160		ns

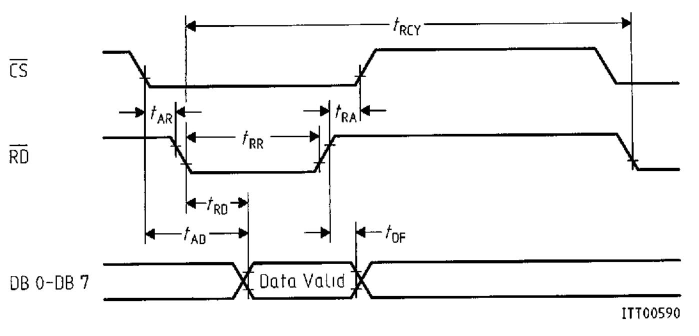


Figure 13
µP-Read Cycle

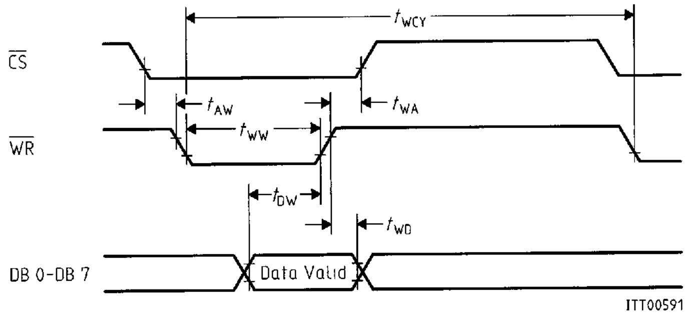


Figure 14
µP-Write Cycle

PCM-Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCM-input setup	t_S	0		ns
PCM-input hold	t_H	30		ns
PEB 2046 output delay	t_D		45	ns
PEF 2046 output delay	t_D		50	ns

Clock and Synchronization Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock period 8 MHz high	$t_{CP8\ H}$	40		ns
Clock period 8 MHz low	$t_{CP8\ L}$	48		ns
Clock period 8 MHz	t_{CP8}	120		ns
Synchronization pulse setup 8 MHz	t_{SS8}	10	$t_{CP8} - 20$	ns
Synchronization pulse delay 8 MHz	t_{SH8}	0	$t_{CP8} - 20$	ns
Clock period 4 MHz high	$t_{CP4\ H}$	90		ns
Clock period 4 MHz low	$t_{CP4\ L}$	90		ns
Clock period 4 MHz	t_{CP4}	240		ns
Synchronization pulse setup 4 MHz	t_{SS4}	10	$t_{CP4} - 30$	ns
Synchronization pulse delay 4 MHz	t_{SH4}	30	$t_{CP4} - 10$	ns

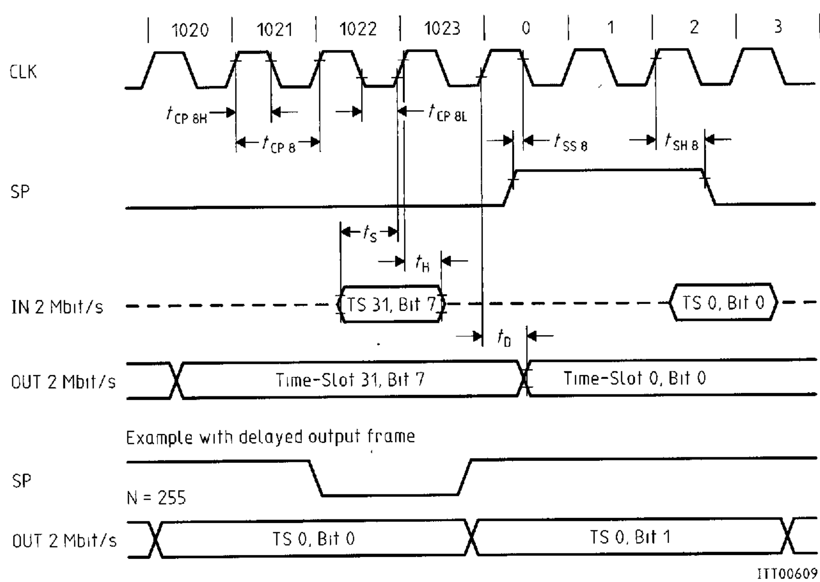


Figure 15
PCM-Line Timing with a 8-MHz Device Clock

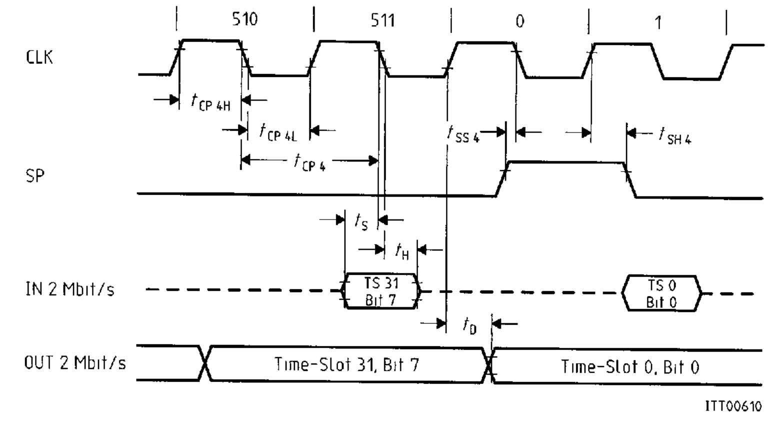
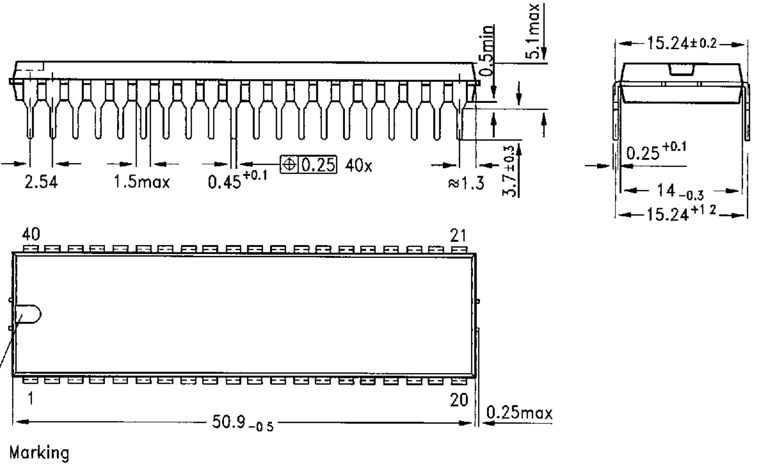


Figure 16
PCM-Line Timing with a 4-MHz Device Clock

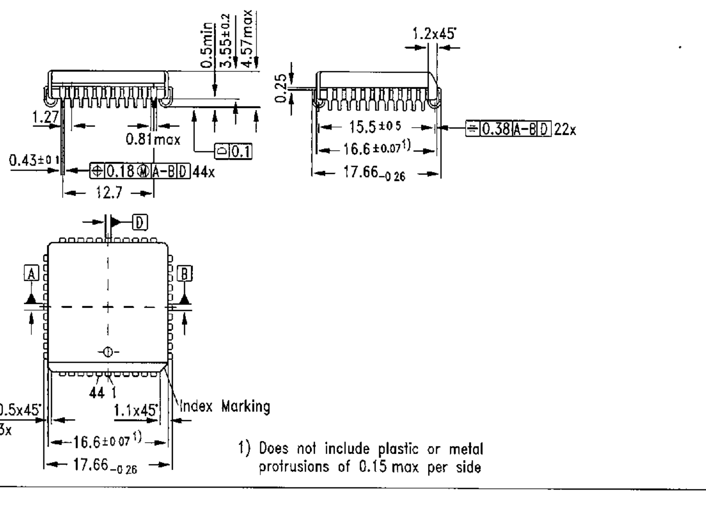
Busy Times

Operation	Max. Values	Unit
Indirect register access	900	ns
Connection memory reset	250	µs

Plastic Package, P-DIP-40
(Plastic Dual In-Line Package)



Plastic Package, P-LCC-44 (SMD)
(Plastic Leaded Chip Carrier)



Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm