Cologne Chip

HFC - S+
B ISDN 2BDS0

ISDN HDLC FIFO controller
with
S/T interface
and
U-chip support

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Revision History

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Features

- One chip ISDN-S-controller with B- and D-channel HDLC support
- Independent Read and Write HDLC-Channels for 2 ISDN B-channels and one ISDN D-channel
- B1- and B2-channel transparent mode independently selectable
- FIFO-size: 4x 7.5 KByte (B-channel) and 2x 512 Byte (D-channel)
- max. 31 HDLC frames (B-channel) and 15 HDLC frames (D-channel) per channel and direction in FIFO
- 56 kbit/s restricted mode for U.S. ISDN lines selectable by software
- full I.430 ITU S/T ISDN support in TE and NT mode for the 3.3V and 5V supply
- B1+B2 HDLC mode
- PCM30 interface configurable to interface MITEL ST™ bus (MVIP™), Siemens IOM2™ or GCI™ for interface to U-chip or external codecs
- direct 8 bit ISA-PC bus interface with buffers for ISA-databus
- One of 6 interrupt channels on ISA-PC bus selectable by software
- ISA-I/O-address selectable by software
- only 2 I/O addresses used on ISA-PC bus
- microprocessor interface compatible to Motorala bus and Siemens/Intel bus
- simple DMA access to PCM30 interface for tone synthetisation
- Timer with interrupt and watchdog capability in processor mode
- 3.3V and 5V supply voltage
- rectangular QFP 100 case

1 General description

The HFC-S+ is an ISDN S/T HDLC basic rate controller for so called „passive“ ISDN PC cards with integrated S/T interface and PCM30 highway interface. It only needs an external SRAM to form a high performance ISDN PC card. Most problems with passive ISDN PC cards as small FIFOs and massive interrupt load for the host CPU are overcome by the HFC-S+. So we call ISDN cards with the HFC-S+ „semi-active“.

Additionally the HFC-S+ can be used as a microprocessor peripheral in non-PC applications.

The ultra-deep FIFOs of the HFC-S+ are realized with an external SRAM. Also an industrial standard serial interface for telecom peripheral ICs is implemented. Codecs are normally connected to this interface.

1.1 Applications

- ISDN PC card
- ISDN terminal adapter
- ISDN PABX
- ISDN modems

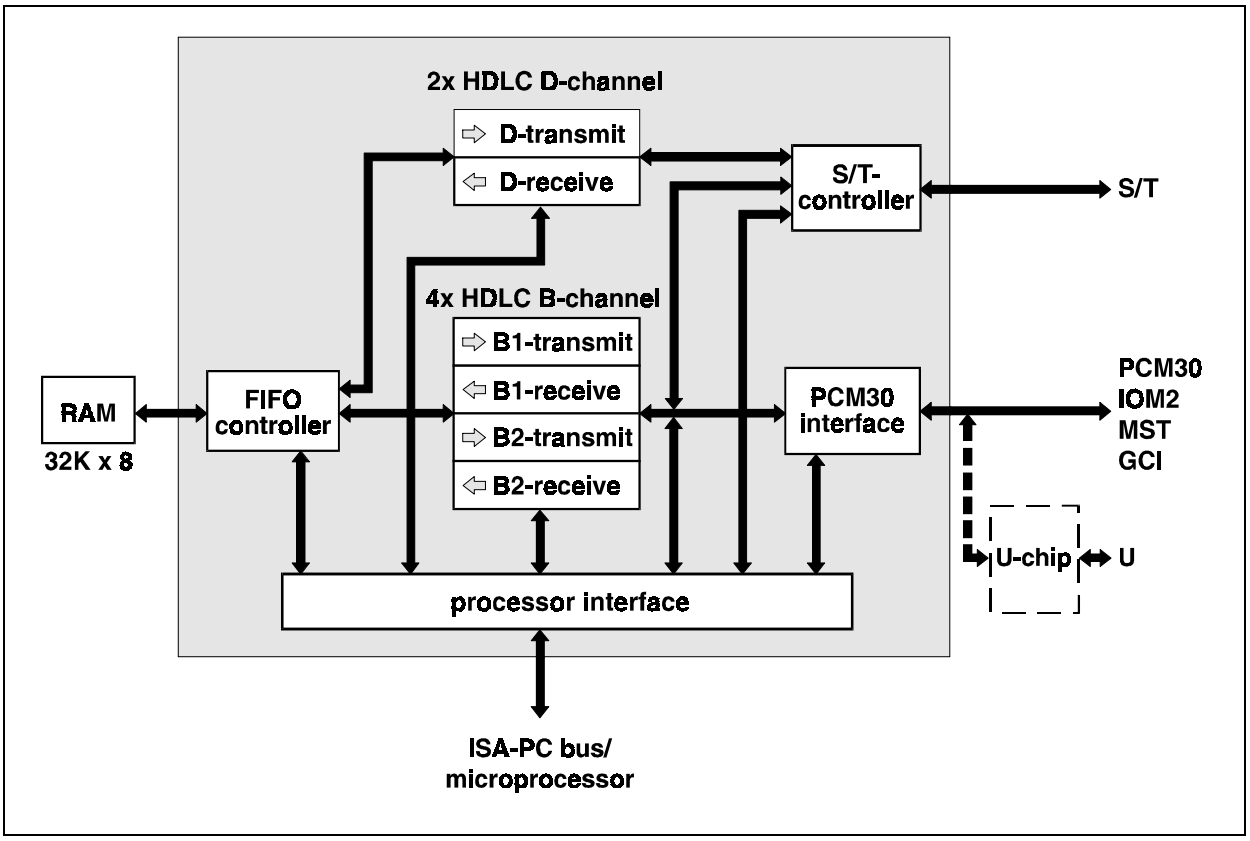


Figure 1: HFC-S+ block diagram

1.2 Mode description

The HFC-S+ has 4 different bus modes, which can be selected by the lines ALE and IIOSEL0-IIOSEL3. Depending on the selected mode the function of several pins is different (see: Pin description).

ALE	IIOSEL0..3	Selected mode
GND	≠0	ISA-PC mode (mode 1)
VDD	all 0	processor mode (mode 2)
GND	all 0	processor mode (mode 3)
pulse	all 0	processor mode (mode 4)

Table 1: Mode selection

1.2.1 ISA-PC mode

Mode 1: ALE = GND, IIOSEL3-0 ≠ 0000

In mode 1 the HFC-S+ is addressed by two successive port addresses on the ISA-PC bus. The port address is selected by the lines SA0 - SA9.
The address with SA0='1' is for register selection and the address with SA0='0' is used for data read/write (see also: 3.1).

1.2.2 Processor interface modes

The processor modes are selected by IIOSEL3-0 = '0000'.
In all processor modes line SA6 must be connected to GND.

Mode 2: Motorola bus with control signals /CS, R/W, /DS is selected by setting ALE to VDD.

Mode 3: Siemens/Intel bus with seperated address bus and databus and control signals /CS, /WR, /RD is selected by setting ALE to GND.

Mode 4: Intel bus with multiplexed address and databus with control signals /CS, /WR, /RD, ALE.
ALE latches the address. The address lines SA0-SA7 must be connected to the data lines BD0-BD7 (except SA6 which must be connected to GND).

The lines SA0-SA7 (except SA6) are used for direct addressing the internal registers of the HFC-S+ (see also 3.3).

2 Pin description

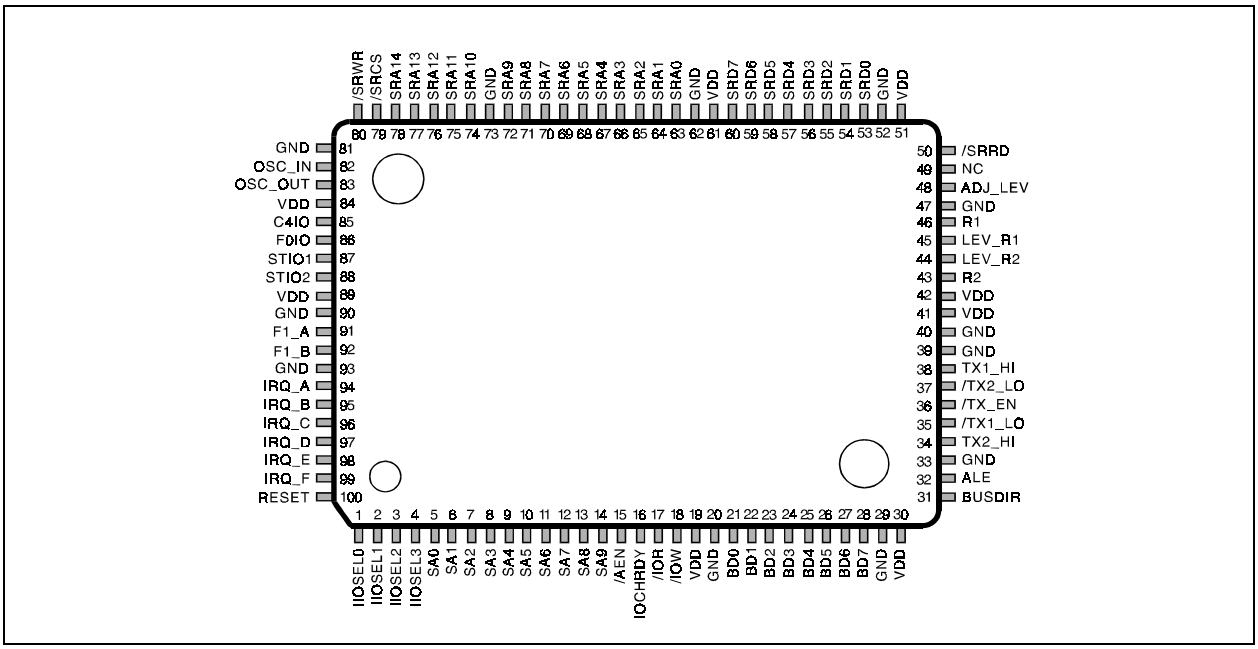


Figure 2: Pin Connection

2.1 ISA-PC bus and microprocessor interface

Pin No.	Pin Name	Input Output	Mode	Function
1	IIOSEL0	I [u)]	1,2,3,4	**Mode/initial I/O address select** bit 0
2	IIOSEL1	I [u)]	1,2,3,4	Mode/initial I/O address select bit 1
3	IIOSEL2	I [u)]	1,2,3,4	Mode/initial I/O address select bit 2
4	IIOSEL3	I [u)]	1,2,3,4	Mode/initial I/O address select bit 3
5	SA0	I	all	**Register/ISA-PC address bus** Address bit 0
6	SA1	I	all	Address bit 1
7	SA2	I	all	Address bit 2
8	SA3	I	all	Address bit 3
9	SA4	I	all	Address bit 4
10	SA5	I	all	Address bit 5
11	SA6	I	all	Address bit 6 (In processer mode SA6 must be connected to GND)
12	SA7	I	all	Address bit 7

[u)] internal pull up

Pin No.	Pin Name	Input Output	Mode	Function
13	SA8 /DMAAK0	I I	1 2,3,4	Address bit 8 DMA acknowledge channel 0 Direct access to GCI/IOM2 bus AUX1 channel data register (low active)
14	SA9 /DMAAK1	I I	1 2,3,4	address bit 9 DMA acknowledge channel 1 direct access on GCI/IOM2 bus AUX2 channel dataregister (low active)

☝ **important!**
If DMA acknowledge signals /DMAAK0 and /DMAAK1 are active, the function of the read/write enables is inverted. This means a read command on the controller databus writes the AUX-Channel register and a write command reads the register. The address on the address bus (SA0-SA7) is ignored.

15	/AEN /CS	I I	1 2,3,4	PC bus address enable chipselect low active
16	IOCHRDY /WAIT	O [1)] O [1)]	1 2,3,4	I/O channel ready low active wait signal for external processor
17	/IOR /DS	I I	1,3,4 2	I/O read enable I/O data strobe
18	/IOW R/W	I I	1,3,4 2	I/O write enable Read/Write select (WR='0')
21	BD0	I/O	all	Databus bit 0 (LSB)
22	BD1	I/O	all	Databus bit 1
23	BD2	I/O	all	Databus bit 2
24	BD3	I/O	all	Databus bit 3
25	BD4	I/O	all	Databus bit 4
26	BD5	I/O	all	Databus bit 5
27	BD6	I/O	all	Databus bit 6
28	BD7	I/O	all	Databus bit 7 (MSB)
31	BUSDIR	O	1,2,3,4	Databus direction signal for external busdriver '0' BD0-BD7 are outputs
32	ALE	I		Address latch enable ALE is also used for mode selection of the HFC-S+. **See Mode selection on page 8 for detailed information.**

[1)] open drain, external pull up resistor required

2.2 S/T interface transmit signals

Pin No.	Pin Name	Input Output	Function
34	TX2_HI	O	Transmit output 2
35	/TX1_LO	O	GND driver for transmitter 1
36	/TX_EN	O	Transmit enable
37	/TX2_LO	O	GND driver for transmitter 2
38	TX1_HI	O	Transmit output 1

See also: 7.2 External transmitter circuitry.

2.3 S/T interface receive signals

43	R2	I	Receive data 2
44	LEV_R2	I	Level detect for R2
45	LEV_R1	I	Level detect for R1
46	R1	I	Receive data 1
48	ADJ_LEV	O	Levelgenerator

See also: 7.1 External receiver circuitry.

2.4 SRAM Interface

Pin No.	Pin Name	Input Output	Function
53	SRD0	I/O	**SRAM data bus** SRAM data bit 0 (LSB)
54	SRD1	I/O	SRAM data bit 1
55	SRD2	I/O	SRAM data bit 2
56	SRD3	I/O	SRAM data bit 3
57	SRD4	I/O	SRAM data bit 4
58	SRD5	I/O	SRAM data bit 5
59	SRD6	I/O	SRAM data bit 6
60	SRD7	I/O	SRAM data bit 7 (MSB)
63	SRA0	O	**SRAM address bus** SRAM address bus bit 0 (LSB)
64	SRA1	O	SRAM address bus bit 1
65	SRA2	O	SRAM address bus bit 2
66	SRA3	O	SRAM address bus bit 3
67	SRA4	O	SRAM address bus bit 4
68	SRA5	O	SRAM address bus bit 5
69	SRA6	O	SRAM address bus bit 6
70	SRA7	O	SRAM address bus bit 7
71	SRA8	O	SRAM address bus bit 8
72	SRA9	O	SRAM address bus bit 9
74	SRA10	O	SRAM address bus bit 10
75	SRA11	O	SRAM address bus bit 11
76	SRA12	O	SRAM address bus bit 12
77	SRA13	O	SRAM address bus bit 13
78	SRA14	O	SRAM address bus bit 14 (MSB)
50	/SRRD	O	**SRAM control signals** Read strobe to external device
79	/SRCS	O	SRAM chip select
80	/SRWR	O	SRAM write enable

2.5 Oscillator

82	OSC_IN	I	Oscillator input or quarz connection 12.288 Mhz or 24.576 MHz
83	OSC_OUT	O	Oscillator output or quarz connection

2.6 GCI/IOM2 bus interface

Pin No.	Pin Name	Input Output	Mode	Function
85	C4IO	I/O [u)]	all	4.096 Mhz clock GCI/IOM2 bus clock master: output GCI/IOM2 bus clock slave: input (reset default)
86	F0IO	I/O [u)]	all	Frame synchronisation, 8kHz pulse for GCI/IOM2 bus frame synchronisation GCI/IOM2 bus master: output GCI/IOM2 bus slave: input (reset default)
87	STIO1	I/O [u)]	all	GCI/IOM2 bus databus I Slotwise programmable as input or output
88	STIO2	I/O [u)]	all	GCI/IOM2 bus databus II Slotwise programmable as input or output

u) internal pull up

2.7 GCI/IOM2 Timeslot enable signals

(e. g. for PCM codecs)

91	F1_A	O	all	enable signal for external CODEC A Programmable as positive (reset default) or negative pulse.
92	F1_B	O	all	enable signal for external CODEC B Programmable as positive (reset default) or negative pulse.

2.8 Interrupt outputs

Pin No.	Pin Name	Input Output	Mode	Function
94	IRQ_A /IRQ_P	I/O O [1]	1 2,3,4	PC bus interrupt request A or interrupt input from external device (see: CIRM register bit description) processor interrupt request low active
95	IRQ_B IRQ_P	O O [2]	1 2,3,4	PC bus interrupt request B processor interrupt request high active
96	IRQ_C /WD_RES	O O [1]	1 2,3,4	PC bus interrupt request C Watchdog expired, external reset low active
97	IRQ_D WD_RES	O O [2]	1 2,3,4	PC bus interrupt request D Watchdog expired, external reset high active
98	IRQ_E DMARQ0	O O	1 2,3,4	PC bus interrupt request E DMA request AUX1 channel register (high active)
99	IRQ_F DMARQ1	O O	1 2,3,4	PC bus interrupt request F DMA request AUX2 channel register (high active)

[1] open drain, external pull up resistor required
[2] open source, external pull down resistor required

2.9 Miscellaneous pins

49	NC			Not connected (leave pin open)
100	RESET	I	all	Reset for HFC-S+ (high active)

2.10 Power supply

Pin No.	Pin Name	Function
19, 30, 41, 42, 51, 61, 84, 89	VDD	VDD (+3V to +5V)
20, 29, 33, 39, 40, 47, 52, 62, 73, 81, 90, 93	GND	GND

☝ **important!**
All power supply pins VDD must be directly connected to each other. Also all pins GND must be directly connected to each other.

To keep VDD and GND bounce to a minimum a bypass capacitor (10 nF to 100 nF) should be placed between each pair of VDD/GND pins.

2.11 RESET characteristics

The reset signal (hardware reset or software reset) must be active for at least 4 clock cycles.

The GCI/IOM2 bus lines STIO1, STIO2 and the interrupt lines are in tristate mode after a reset.

The HFC-S+ is in slave mode after reset. C4IO and F0IO are inputs.

In the processor modes DMARQ1 and DMARQ2 are inactive ('0').

The S/T state machine is stuck to '0' after reset. This means the HFC-S+ does not react to any signal on the S/T interface before the S/T state machine is initialised.

The registers' initial values are described in the Register bit description (section 4 of this data sheet).

After RESET the HFC-S+ is in an initialisation cycle and is therefor busy for a maximum of 160 clock cycles.

3 Functional description

3.1 ISA-PC mode

ISA-PC mode is selected by ALE = GND and IIOSEL0..3≠0.

The HFC-S+ occupies two consecutive addresses in the I/O map of a PC if it is in ISA-PC mode. It decodes only the 10 lower address lines as most slot cards do on the ISA-PC bus. The base I/O address is 2 byte aligned so the lower of both addresses is the one with SA0 = 0 and the higher address is the one with SA0 = 1.

After every hardware reset (RESET = 1) the I/O address select circuit inside the HFC-S+ is in hardware mode. In this mode the HFC-S+ can not be accessed until it is initialised to an I/O address.

At first one of 15 different I/O addresses must be selected by the 4 inputs IIOSEL0 .. IIOSEL3 as Table 2 shows:

IIOSEL 3 2 1 0	Selected I/O address
0 0 0 0	processor mode
0 0 0 1	2E0h
0 0 1 0	2D0h
0 0 1 1	210h
0 1 0 0	2C0h
0 1 0 1	200h
0 1 1 0	2F8h
0 1 1 1	2E8h
1 0 0 0	2B0h
1 0 0 1	3E0h
1 0 1 0	320h
1 0 1 1	278h
1 1 0 0	310h
1 1 0 1	330h
1 1 1 0	300h
1 1 1 1	3E8h

Table 2: Selected I/O address after reset

The hardware selected I/O address might have an address collision with another I/O device in the PC.

After a hardware reset (RESET = 1) you must first write an I/O address into the HFC-S+ to set the I/O address for every further access to the device.

The procedure is as follows:
First you must write the lower 8 bits of the new I/O address you want into the lower address (SA0 = 0) of the hardware selected I/O address. The LSB of the new address is a don't care bit because the HFC-S+ always occupies two I/O addresses.

Then the additional 2 bits of the new I/O address have to be written into the higher address (SA0 = 1) of the hardware selected I/O address. The other 6 bits in the byte must have a special pattern to switch over to the software selected address mode. This pattern must be 0101 01**aa**, whereby **aa** are the 2 higher address bits.

e.g.: wanted I/O address: **3A4h** / **3A5h**

IIOSEL(3:0): 0001
then hardware selected I/O address is: **2E0h** = 10 1110 0000 b

write the value **A4h** or **A5h** into **2E0h**	= 1010 010x b		
write the value **57h** into **2E1h**	= 0101 01 b		pattern
	11 b		address
	0101 0111 b		

x = don't care

All further accesses to the HFC-S+ can only be done on the addresses **3A4h** / **3A5h**. Only a hardware reset will switch back the HFC-S+ into hardware selected address mode.

☝ **hint:**
It's useful to solve a possible address conflict by programming the I/O address as early as possible. It is recommendable to set the address with a simple .SYS driver in a DOS environment.

3.2 ISA-PC bus interface

The HFC-S+ only uses 2 I/O addresses with SA0 switching between data or control information in ISA-PC mode. As normal only 10 bits of the ISA-PC bus address are used for I/O address selection in ISA-PC mode.

SA0	/IOR	/IOW	/AEN	Operation
X	X	X	1	no access
X	1	1	X	no access
0	0	1	0	read data
0	1	0	0	write data
1	0	1	0	read status
1	1	0	0	write control

X = don't care

☝ **important!**
ALE must be connected to GND and at least one of the IIOSEL0-3 must be '1' or open!

The HFC-S+ has no memory or DMA access to any component on the ISA-PC bus.

Because of its power drive characteristic it needs no external driver for the ISA-PC bus data lines.

If necessary an external bus driver can be added. In this case the output BUSDIR determines the driver direction.

BUSDIR = 1 means that data is driven into the HFC-S+;
BUSDIR = 0 means that the HFC-S+ is read and data is driven to the external bus.

3.3 Processor mode

Processor mode is selected by IIOSEL0..3=0.

In the microprocessor mode the HFC-S+ uses 256 I/O addresses (SA0 - SA7).

/IOR /DS	/IOW R/W	/CS	ALE	Operation	Mode
X	X	1	X	no access	all
1	1	X	X	no access	all
0	1	0	1	read data	2
0	0	0	1	write data	2
0	1	0	0	read data	3
1	0	0	0	write data	3
0	1	0	0*)	read data	4
1	0	0	0*)	write data	4

X = don't care

*) 1-pulse latches I/O address.

All registers are directly accessable by their I/O address (see register description).

Except in mode 4 ALE is assumed to be stable after a RESET.

☝ **important!**

For write accesses to the HFC-S+ the data lines must be stable and valid **before** /IOW or /DS get low (see also: Timing diagram 1 on page 51). With Intel compatible processors it may be neccessary to delay the /IOW or /DS signals.

3.3.1 DMA access in processor mode

In processor mode a simple DMA access to the auxiliary channels of the GCI/IOM2 interface is possible. This is useful for tone synthetisation or for voice recording. DMAREQ is asserted every 125µs. DMAREQ is reset when /DMAAK is active.

☝ **note**
If DMA acknowledge signals /DMAAK0 and /DMAAK1 are active, the function of the read/write enables is inverted. This means a read command on the controller databus writes the AUX-Channel register and a write command reads the register. The address on the address bus (SA0-SA7) is ignored.

Mode	/DMAAK0	/DMAAK1	/CS	ALE	/IOR /DS	/IOW R/W	Function
2,3,4	1	1	X	X	X	X	no DMA
2	0	1	X	1	X	1	DMA write AUX1
2	1	0	X	1	X	1	DMA write AUX2
3	0	1	X	0	0	1	DMA write AUX1
3	1	0	X	0	0	1	DMA write AUX2
4	0	1	X	0*)	0	1	DMA write AUX1
4	1	0	X	0*)	0	1	DMA write AUX2

Table 3: DMA access in processor mode

*) 1-pulse latches I/O address.

☝ **important!**
If DMA is not used /DMAAK0 and /DMAAK1 must be connected to VDD.

3.4 Internal HFC-S+ register description

In ISA-PC mode all registers are selected by writing the register address into the Control Internal Pointer (CIP) register. This is done by writing the HFC-S+ on the higher I/O address (SA0 = 1).
All consecutive read or write data accesses (SA0 = 0) are done with the selected register until the CIP register is changed.

In processor mode all registers can be directly accessed. The registers are selected by SA0 - SA7.

3.4.1 FIFO control registers

The FIFO control registers are used to select and control the FIFOs of the HFC-S+. In processor mode the value is the address which directly selects the corresponding register.

The FIFO register selection is independent of the B- or D-channel FIFO number.
The FIFO is selected by the FIFO select register.

3.4.1.1 FIFO select register

CIP / I/O-address		Name	r/w	Function
00010000	10h	FIF_SEL	w	FIFO selection

3.4.1.2 FIFO registers

CIP / I/O-address		Name	r/w	Function
100000xx	80h	FIF_Z1L	r	FIFO input counter (Z1) low byte
100001xx	84h	FIF_Z1H	r	FIFO input counter (Z1) high byte
100010xx	88h	FIF_Z2L	r	FIFO output counter (Z2) low byte
100011xx	8Ch	FIF_Z2H	r	FIFO output counter (Z2) high byte
101010xx	A8h	FIF_INC_F1*)	r	read this register to increment frame counter F1
101011xx	ACh	FIF_DWR	w	data write into FIFO and increment Z1
101100xx	B0h	FIF_F1	r	FIFO input HDLC frame counter (F1)
101101xx	B4h	FIF_F2	r	FIFO output HDLC frame counter (F2)
101110xx	B8h	FIF_INC_F2*)	r	read this register to increment frame counter F2
101111xx	BCh	FIF_DRD	r	data read out of FIFO and increment Z2

*) only in HDLC mode; In transparent mode (see also: 3.7.2) the frame counters F1 and F2 must not be incremented.

☝ **important!**

FIFO change, FIFO reset and F1/F2 incrementation
Changing the FIFO, reseting the FIFO or incrementing the frame counters causes a short BUSY period of the HFC-S+. This means an access to FIFO control registers is NOT allowed until BUSY status is reset (bit 0 of STATUS register). This has a maximum duration of 25 clock cycles (2µs). Status, interrupt and control registers can be read and written at any time.

3.4.2 Registers of the S/T section

CIP / I/O-address		Name	r/w	Function
00110000	30h	STATES	r/w	State of the TE/NT state machine
00110001	31h	SCTRL	w	S/T control register
00110010	32h	SCTRL_E	w	S/T control register (extended)
00110011	33h	SCTRL_R	w	receive enable for B-channels
00110100	34h	SQ_REC SQ_SEND	r w	receive register for S/Q bits send register for S/Q bits
00110111	37h	CLKDEL	w	setup of the delay time between receive and send direction (TE) receive data sample time (NT)
00111100	3Ch	B1_REC*) B1_SEND*)	r w	B1-channel receive register B1-channel transmit register
00111101	3Dh	B2_REC*) B2_SEND*)	r w	B2-channel receive register B2-channel transmit register
00111110	3Eh	D_REC*) D_SEND*)	r w	D-channel receive register D-channel transmit register
00111111	3Fh	E_REC*)	r	E-channel receive register

*) These registers are read/written automatically by the HDLC FIFO controller (HFC) or GCI/IOM2 bus controller and need not be accessed by the user. To read/write data the FIFO registers should be used.

3.4.3 Registers of the GCI/IOM2 bus section

GCI/IOM2 bus timeslot selection registers

CIP / I/O-address		Name	r/w	Function
00000010	02h	C/I	r/w	C/I command/indication register
00000011	03h	TRxR	r	Monitor Tx ready handshake
00001010	0Ah	MON1_D	r/w	first monitor byte
00001011	0Bh	MON2_D	r/w	second monitor byte

GCI/IOM2 bus timeslot selection registers

CIP / I/O-address		Name	r/w	Function
00100000	20h	B1_SSL	w	B1-channel transmit slot (0..31)
00100001	21h	B2_SSL	w	B2-channel transmit slot (0..31)
00100010	22h	AUX1_SSL	w	AUX1-channel transmit slot (0..31)
00100011	23h	AUX2_SSL	w	AUX2-channel transmit slot (0..31)
00100100	24h	B1_RSL	w	B1-channel receive slot (0..31)
00100101	25h	B2_RSL	w	B2-channel receive slot (0..31)
00100110	26h	AUX1_RSL	w	AUX1-channel receive slot (0..31)
00100111	27h	AUX2_RSL	w	AUX2-channel receive slot (0..31)

GCI/IOM2 bus data registers

CIP / I/O-address		Name	r/w	Function
00101000	28h	B1_D*)	r/w	GCI/IOM2 bus B1-channel data register
00101001	29h	B2_D*)	r/w	GCI/IOM2 bus B2-channel data register
00101010	2Ah	AUX1_D**)	r/w	AUX1-channel data register
00101011	2Bh	AUX2_D**)	r/w	AUX2-channel data register

*) These registers are read/written automatically by the HDLC FIFO controller (HFC) or by the S/T controller and need not be accessed by the user.

**) These registers can also be accessed by DMA

GCI/IOM2 bus configuration registers

CIP / I/O-address		Name	r/w	Function
00101101	2Dh	MST_EMOD	w	extended mode register for GCI/IOM2 bus
00101110	2Eh	MST_MODE	w	mode register for GCI/IOM2 bus
00101111	2Fh	CONNECT	w	connect functions for S/T, HFC, GCI/IOM2

3.4.4 Interrupt and status registers

CIP / I/O address		Name	r/w	Function
00010010	12h	TRM	w	transparent mode interrupt mode register
00010011	13h	B_MODE	w	mode of B-channels
00010110	16h	CHIP_ID	r	register for chip identification
00011000	18h	CIRM	w	interrupt selection and softreset register
00011001	19h	CTMT	w	transparent mode and timer control register
00011010	1Ah	INT_M1	w	interrupt mask register 1
00011011	1Bh	INT_M2	w	interrupt mask register 2
00011110	1Eh	INT_S1	r	interrupt status register 1
00011111	1Fh	INT_S2	r	interrupt status register 2
00011100	1Ch	STATUS	r	common status register

3.5 Timer

The HFC-S+ includes a timer with interrupt capability. The timer counts F0IO pulses. So the timer counter is incremented every 125µs. It can be reset by bit 7 of of the CTMT register. Furthermore the timer is reset at every HFC-S+ access when bit 5 of the CTMT register is set. Seven different timer values can be selected.

3.6 Watchdog
(only available in processor mode)

The watchdog outputs of the HFC-S+ are activated if the timer interrupt bit is active (not reset by reading INT_S1) and the timer elapses a second time.
The reset of the timer counter itself and the watchdog value can be programmed in the CTMT register. In automatic reset mode the watchdog/timer is reset by every access to the HFC-S+.

3.7 FIFOs

There are 6 FIFOs with 6 HDLC-Controllers in the HFC-S+. The HDLC circuits are located on the S/T device side of the HFC-S+. So always plain data is stored in the FIFO. Zero insertion and deletion is done in HDLC mode:

– if the data goes to the S/T or GCI/IOM device in send FIFOs and
– when the HDLC data comes from the S/T device or GCI/IOM2 bus in receive operation.

There are a send and a receive FIFO for each of the two B-channels and for the D-channel.

The FIFOs are realized as ring buffers in the external SRAM. To control them there are some counters.

	B-channel	D-channel
Z1: FIFO input counter	13 Bit	9 Bit
Z2: FIFO output counter	13 Bit	9 Bit

Each counter points to a byte position in the SRAM. On a FIFO input operation Z1 is incremented. On an output operation Z2 is incremented.

After every pulse on the F0IO signal two HDLC-bytes are written into the S/T interface (FIFOs No. 0 and 2) and two HDLC-bytes are read from the S/T interface (FIFOs No. 1 and 3).
D-channel data is handled in a similar way but only 2 bits are processed.

> ☝ **important!**
> Instead of the S/T interface also GCI/IOM2 bus is selectable for each B-channel (see CONNECT register).

If Z1 = Z2 the FIFO is empty.

Additionally there are two counters F1 and F2 for every FIFO channel (5Bit for B-channel, 4Bit for D-channel). They count the HDLC-frames in the FIFOs and form a ring buffer as Z1 and Z2 do, too.

F1 is incremented when a complete frame has been received and stored in the FIFO. F2 is incremented when a complete frame has been read from the FIFO.

If F1 = F2 there is no complete frame in the FIFO.

When the RESET line is active or software reset is active Z1, Z2, F1 and F2 are all initialized to all 1s.

The access to a FIFO is selected by writing the FIFO number into the FIFO select register (FIF_SEL).

☝ **important!**

FIFO change, FIFO reset and F1/F2 incrementation
Changing the FIFO, reseting the FIFO or incrementing the frame counters causes a short BUSY period of the HFC-S+. This means an access to FIFO control registers is NOT allowed until BUSY status is reset (bit 0 of STATUS register). This has a maximum duration of 25 clock cycles (2µs). Status, interrupt and control registers can be read and written at any time.

☝ **important!**
The counter state 0200h of the Z-counters follows counter state 1FFFh in the B-channel FIFOs.
If 8k RAM mode is selected counter state 1A00h of the Z-counters follows counter state 1FFFh in the B-channel FIFOs.
The counter state 000h of the Z-counters follows counter state 1FFh in the D-channel FIFOs.

The counter state 00h of the F-counters follows counter state 1Fh in the B-channel FIFOs.
The counter state 10h of the F-counters follows counter state 1Fh in the D-channel FIFOs.

3.7.1 FIFO channel operation

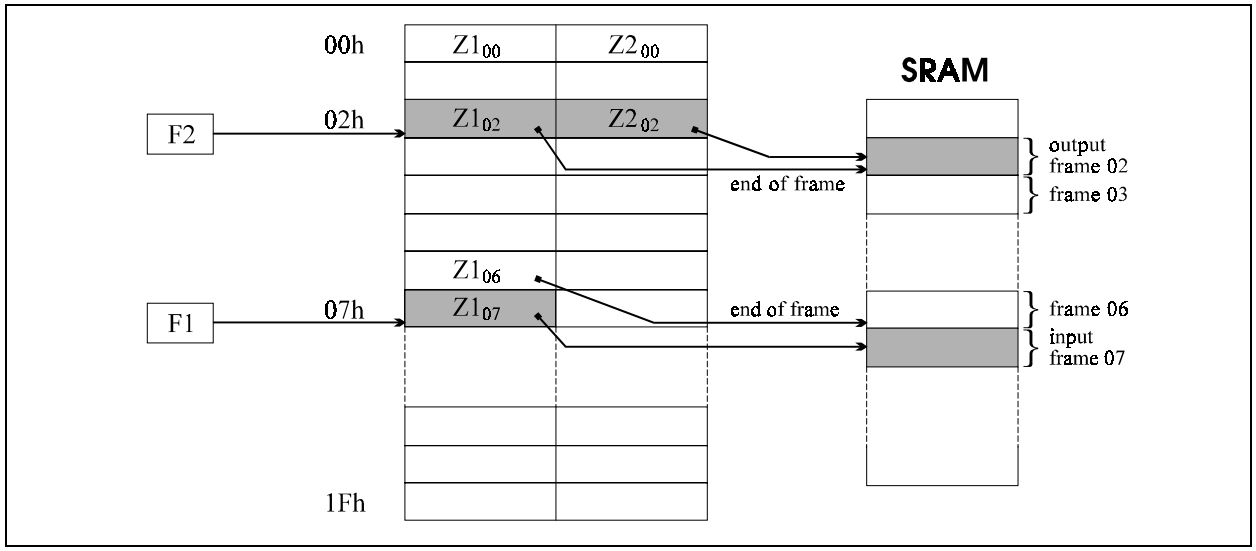


Figure 3: FIFO Organisation (shown for B-channel, similar for D-channel)

3.7.1.1 Send channels (B1, B2 and D transmit)

The send channels send data from the host bus interface to the FIFO and the HFC-S+ converts the data into HDLC code and tranfers it from the FIFO into the S/T or/and the GCI/IOM2 bus interface write registers.

The HFC-S+ checks Z1 and Z2. If Z1=Z2 (FIFO empty) the HFC-S+ generates a HDLC-Flag (01111110) and sends it to the S/T device. In this case Z2 is not incremented. If also F1=F2 only HDLC flags are sent to the S/T interface and all counters remain unchanged. If the frame counters are unequal F2 is incremented and the HFC-S+ tries to send the next frame to the output device. After the end of a frame (Z2 reaches Z1) it automatically generates the 16 bit CRC checksum and adds the ending flag. If there is another frame in the FIFO (F1≠F2) the F2 counter is incremented.

With every byte being sent from the host bus side to the FIFO Z1 is incremented automatically. If a complete frame has been sent F1 must be incremented to send the next frame. If the frame counter F1 is incremented also the Z-counters may change because Z1 and Z2 are functions of F1 and F2. So there are Z1(F1), Z2(F1), Z1(F2) and Z2(F2) (see Figure 3).
Z1(F1) is used for the frame which is just written from the PC-bus side. Z2(F2) is used for the frame which is just beeing transmitted to the S/T device side of the HFC-S+. Z1(F2) is the end of frame pointer of the current output frame.

In the send channels F1 is only changed from the PC interface side if the software driver wants to say „end of send frame“. Then the current value of Z1 is stored, F1 is incremented and Z1 is used as start address of the next frame. Z1(F2) and Z2(F2) can not be accessed.

3.7.1.2 Automatically D-channel frame repetition

The D-channel send FIFO has a special feature. If the S/T interface signals a D-channel contention before the CRC is sent the Z2 counter is set to the starting address of the current frame and the HFC-S+ tries to repeat the frame automatically.

> ☝ **important!**
> The HFC-S+ begins to transmit the bytes from a FIFO at the moment the FIFO is changed or the F1 counter is incremented. Also changing to the FIFO that is already selected starts the transmission. So by selecting the same FIFO again transmission can be started.

3.7.1.3 FIFO full condition in send channels

Due to the limited number of registers in the HFC-S+ the driver software must maintain a list of frame start and end addresses to calculate actual FIFO size and check FIFO full condition. Because there are a maximum of 32 frame counter values and the start address of a frame is the incremented value of the end address of the last frame the memory table must have only 32 values of 16 bits (13 bits) instead of 64.

Remember that an increment of Z-value 1FFFh is 0200h in the B-channels!

There are two different FIFO full conditions. The first one is met when the FIFO contents comes up to 31 frames (B-channel) or 15 frames (D-channel). There is no possibility for the HFC-S+ to manage more frames even if the frames are very small.

The second limitation is the size of the FIFO which is 512 byte for the D-channel and 7.5 KByte for the B-channels.

3.7.1.4 Receive Channels (B1, B2 and D receive)

The receive channels receive data from the S/T or GCI/IOM2 bus interface read registers. The data is converted from HDLC into plain data and sent to the FIFO. The data can then be read via the host bus interface.

The HFC-S+ checks the HDLC data coming in. If it finds a flag or more than 5 consecutive 1s it does not generate any output data. In this case Z1 is not incremented. Proper HDLC data being received is converted by the HFC-S+ into plain data. After the ending flag of a frame the HFC-S+ checks the HDLC CRC checksum. If it is correct one byte with all 0s is inserted behind the CRC data in the FIFO named STAT. This last byte of a frame in the FIFO is different from all 0s if there is no correct CRC field at the end of the frame.

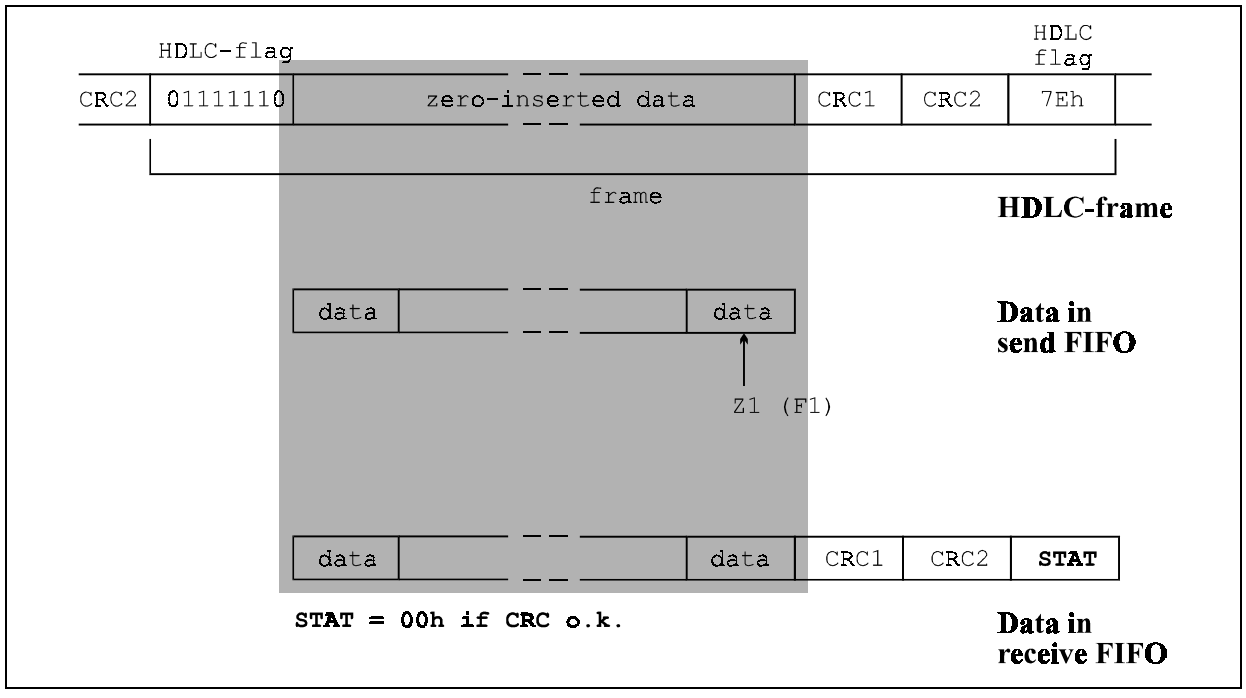


Figure 4: FIFO Data Organisation

The ending flag of a HDLC-frame can also be the starting flag of the next frame.

After a frame is received completely F1 is incremented by the HFC-S+ automatically and the next frame can be received.

After reading a frame via the host bus interface F2 must be incremented. If the frame counter F2 is incremented also the Z-counters may change because Z1 and Z2 are functions of F1 and F2. So there are Z1(F1), Z2(F1), Z1(F2) and Z2(F2) (see Figure 3).
Z1(F1) is used for the frame which is just received from the S/T device side of the HFC. Z2(F2) is used for the frame which is just beeing transmitted to the host bus interface. Z1(F2) is the end of frame pointer of the current output frame.

To calculate the length of the current receive frame the software has to evaluate Z1-Z2+1. When Z2 reaches Z1 the complete frame has been read.

In the receive channels F2 must be incremented from the host interface side after the software detects an end of receive frame (Z1=Z2) and F1≠F2. Then the current value of Z2 is stored, F2 is incremented and Z2 is copied as start address of the next frame. If Z1 = Z2 and F1 = F2 the FIFO is totally empty. Z1(F1) can not be accessed.

☝ **important!**
Before reading a FIFO a change FIFO operation (see also: FIF_SEL register) must be done even if the desired FIFO is already selected. The change FIFO operation is required to update the internal buffer of the HFC-S+. Otherwise the first byte of the FIFO will be taken from the internal buffer and may be invalid.

3.7.1.5 FIFO full condition in receive channels

Because the ISDN-B-channels and the ISDN-D-channels have no hardware based flow control there is no possibility to stop input data if a receive FIFO is full.

So there is no FIFO full condition implemented in the HFC-S+. The HFC-S+ assumes that the FIFOs are so deep that the host processor hard- and software is able to avoid any overflow of the receive FIFOs. Overflow conditions are again more than 31 input frames (15 frames for D-channel) or a real overflow of the FIFO because of excessive data.

Because HDLC procedures only know a window size of 7 frames no more than 7 frames are sent without software intervention. Due to the great size of the FIFOs of the HFC-S+ it is easy to poll the HFC-S+ even in large time intervalls without having to fear a FIFO overflow condition.

However to avoid any undetected FIFO overflows the software driver should check the number of frames in the FIFO which is F1-F2. An overflow exists if the number (F1-F2) is less than the number in the last reading even if there was no reading of a frame in between.

After a detected FIFO overflow condition this FIFO must be reset by setting the FIFO reset bit in the CIRM register.

3.7.1.6 FIFO reset

All counters Z1, Z2, F1 and F2 of all FIFOs are initialized to all 1s after a RESET.

Then the result is Z1 = Z2 = 1FFFh and F1 = F2 = 1Fh for the B-channels
and Z1 = Z2 = 1FFh and F1 = F2 = 1Fh for the D-channel.

Please mask bit 4 of D-channel from counter F1, F2.

The same initialisation is done if the bit 3 in the CIRM register is set (soft reset).

Individual FIFOs can be reset by bit 7 of CIRM register.

3.7.2 Transparent mode of HFC-S+

You can switch off HDLC operation for each B-channel independently. There is one bit for each B-channel in the CTMT control register. If this bit is set data in the FIFO is sent directly to the S/T or GCI/IOM2 bus interface and data from the S/T or GCI/IOM2 bus interface is sent directly to the FIFO.

Be sure to switch into transparent mode only if F1=F2. Being in transparent mode the Fx counters remain unchanged. Z1 and Z2 are the input and output pointers respectively. Because F1=F2 both Z-counters are always accessable and have valid data.

Because always one Z-counter is changed by the HFC-S+ and only 8 bits of a counter can be read at a time the counter should be read twice to check for a counter incrementation between low and high byte accesses.

If a send FIFO channel changes to FIFO empty condition no CRC is generated and the last data byte written into the FIFO is repeated until there is new data.

In receive channels there is no check on flags or correct CRCs and no status byte is added.

The byte bounderies are not arbitrary like in HDLC mode where byte synchronisation is achieved with HDLC-flags. The data is just the same as it comes from the S/T or GCI/IOM2 bus interface or is sent to this.

Send and receive transparent data can be handled in two ways. The usual way is tranporting B-channel data with the LSB first as it is usual in HDLC mode. The second way is sending the bytes in reverse bit order as it is usual for PWM data. So the first bit is the MSB. The bit order can be reversed by setting bit 7 of the FIF_SEL register when the FIFO is selected.

3.8 External SRAM

For the FIFO data an 32K x 8 external SRAM is used. A 8K x 8 external SRAM is also possible but not recommended.

The required access time is 80 ns or below.

1024 Bytes of the external SRAM are reserved for internal HFC-SP use.

External SRAM	B-channel FIFO size per channel and direction	D-channel FIFO size per direction
8K x 8	1536 Bytes	512 Bytes
32K x 8	7680 Byte	512 Byte

Table 4: SRAM and FIFO size

To initialise the HFC-S for 8K x 8 SRAM use:
- write 18h to the CIRM register
- wait at least 4 clock cycles
- write 10h to the CIRM register

For all further accesses to the CIRM register bit 4 must be set.

☝ **hint!**
If you connect the HFC-S+ with the SRAM you can simplify PCB layout if you permutate address lines and data lines. If you connect data lines of the SRAM with data lines of the HFC-S+ and SR-address lines of the HFC-S+ with address lines of the SRAM you can do this in any order.

3.9 Power down considerations

For very low power consumption the oscillator of the HFC-S+ can be stopped. Furthermore the external SRAM is disabled (/SR_CS=1). To avoid current generated by floating inputs the data bus of the SRAM and all other inputs must be put to GND or VDD. So it is useful to connect the SRAM data bus to a resistor array of about 1MΩ. If the HFC-S+ is operated in processor mode the unused interrupt lines (and watchdog lines) should not be left open. They should be connected to VDD or GND over a resistor to reduce current.
If the oscillator is stopped and the awake option is disabled the supply current is reduced to less than 1mA.

3.10 Configuring test loops

For electrical tests of layer 1 it is useful to create a S/T test loop for the B1/B2 channel. The test loop described here transmits the data that has been received on the B1 or B2 channel to the same channel on the S/T interface. To configure this loop the following must be done:

- write **0Fh** to register CLKDEL (**37h**) // Adjust the phase offset between receive and transmit direction (the value depends on the external circuitry).
- write **43h** to register SCTRL (**31h**) // 03h is to enable B1, B2 at the S/T interface for transmission // 40h is for TX_LO setup (capacitive line mode)
- write **00h** to register STATES (**30h**) // Release S/T state machine for activation over the S/T interface by incoming INFO 2 or INFO 4.
- write **03h** to register SCTRL_R (**33h**) // Configure S/T B1 and B2 channel to normal receive operation.
- write **36h** to register CONNECT (**2Fh**) // Configure CONNECT register for B1/B2 channel test loop.
- write **80h** to register B1_SSL (**20h**) // Enable transmit channel for GCI/IOM2 bus, pin STIO1 is used as output, use time slot #0.
- write **C0h** to register B1_RSL (**24h**) // Enable receive channel for GCI/IOM2 bus, pin STIO1 is used as input, use time slot #0.
- write **81h** to register B2_SSL (**21h**) // Enable transmit channel for GCI/IOM2 bus, pin STIO1 is used as output, use transmission slot #1.
- write **C1h** to register B2_RSL (**25h**) // Enable receive channel for GCI/IOM2 bus, pin STIO1 is used as input, use time slot #1.
- write **01h** to register MST_MODE (**2Eh**) // Configure HFC-S+ as GCI/IOM2 bus master.

4 Register bit description

4.1 Register bit description of the FIFO select register

Name	Addr.	Bits	r/w	Function
FIF_SEL	10h	2..0	w	select FIFO and operation bit 2 bit 1 bit 0 selected operation 0 0 0 B1 transmit 0 0 1 B1 receive 0 1 0 B2 transmit 0 1 1 B2 receive 1 x 0 D transmit 1 x 1 D receive
		6..3		unused, should be '0'
		7	w	select data transmission bit order '0' normal read/write data operation '1' reverse bit order read/write data operation

4.2 Register bit description of S/T section

Name	Addr.	Bits	r/w	Function
STATES	30h	3..0	r	binary value of actual state (NT: Gx, TE: Fx)
(read)		4	r	Frame-Sync ('1'=synchronized)
		5	r	'1' timer T2 expired (NT mode only, see also 8.1 S/T interface activation/deactivation layer 1 for finite state matrix for NT on page 61)
		6	r	'1' receiving INFO0
		7	r	'0' no operation '1' in NT mode allows transition from G2 to G3. This bit is automatically cleared after the transition.
STATES	30h	3..0	w	binary value of new state (NT: Gx, TE: Fx) (bit 4 must also be set to load the state).
(write)		4	w	'1' loads the prepared state (bit 3..0) and stops the state machine.This bit needs to be set for a minimum period of 5.21µs and must be cleared by software. (reset default) '0' enables the state machine (bits 3..0 are ignored). After writing an invalid state the state machine goes to deactivated state (G1, F2)
		6..5	w	'00' no operation '01' no operation '10' start deactivation '11' start activation The bits are automatically cleared after activation/deactivation.
		7	w	'0' no operation '1' in NT mode allows transition from G2 to G3. This bit is automatically cleared after the transition.

☝ **important!**
The state machine is stuck to '0' after a reset. Writing a '0' to bit 4 of the STATES register restarts the state machine.
In this state the HFC-S+ sends no signal on the S/T-line and it is not possible to activate it by incoming INFOx.

NT mode:
The NT state machine does not change automatically from G2 to G3 if the TE side sends INFO3 frames. This transition must be activated each time by bit 7 of the STATES register.

Fix the NT state machine to state G3 when activated (by writing 13h into STATES register). This prevents deactivation of NT mode S/T interface due to sporadically errors on NT input data.

Name	Addr.	Bits	r/w	Function
SCTRL	31h	0	w	'0' B1 send data disabled (permanent 1 sent in activated states, reset default) '1' B1 data enabled
		1	w	'0' B2 send data disabled (permanent 1 sent in activated states, reset default) '1' B2 data enabled
		2	w	S/T interface mode '0' TE mode (reset default) '1' NT mode
		3	w	D-channel priority '0' high priority 8/9 (reset default) '1' low priority 10/11
		4	w	S/Q bit transmission '0' S/Q bit disable (reset default) '1' S/Q bit and multiframe enable
		5	w	'0' normal operation (reset default) '1' send 96kHz transmit test signal (alternating zeros)
		6	w	TX_LO line setup This bit must be configured depending on the used S/T module and circuitry to match the 400Ω pulse mask test. '0' capacitive line mode (reset default) '1' non capacitive line mode
		7	w	Power down '0' power up, oscillator active (reset default) '1' power down, oscillator stopped This bit is not cleared by a soft reset.
SCTRL_E	32h	0	w	Power down mode bit '0' S/T awake disable (reset default) Power up can only be programmed by register access (SCTRL bit 7). '1' S/T awake enable. Oscillator starts on every non INFO0 S/T signal.
		1	w	must be '0'
		2	w	D reset '0' normal operation (reset default) '1' D bits are forced to '1'
		3	w	D_U enable '0' normal operation (reset default) '1' D channel is always send enabled regardless of E receive bit
		4	w	force E=0 (NT mode) '0' normal operation (reset default) '1' E-bit send is forced to 0
		6..5	w	must be '0'
		7	w	'1' swap B1 and B2-channel in the S/T interface

Name	Addr.	Bits	r/w	Function
SCTRL_R	33h	0	w	B1-channel receive enable
		1	w	B2-channel receive enable '0' B-receive bits are forced to '1' '1' normal operation
		7..2	w	unused
SQ_REC	34h	3..0	r	TE mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4) NT mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4)
		4	r	'1' a complete S or Q multiframe has been received Reading SQ_REC clears this bit.
		6..5	r	not defined
		7	r	'1' ready to send a new S or Q multiframe Writing to SQ_SEND clears this bit.
SQ_SEND	34h	3..0	w	TE mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4) NT mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4)
		7..4	w	not defined
CLKDEL	37h	3..0	w	TE: 4 bit delay value to adjust the 2 bit time between receive and transmit direction. The delay of the external S/T-interface circuit can be compensated. The lower the value the smaller the delay between receive and transmit direction (see also Figure 10) NT: Data sample point. The lower the value the earlier the input data is sampled. The steps are 163ns.
		6..4	w	NT mode only early edge input data shaping Low pass characteristic of extended bus configurations can be compensated. The lower the value the earlier input data pulse is sampled. No compensation means a value of 6 (110b). Step size is the same as for bits 3-0.
		7	w	unused

☝ **note!**
The register is not initialized with a '0' after reset. The register should be initialized as follows before activating the TE/NT state machine:
TE mode: 0Dh .. 0Fh NT mode: 6Ch

4.3 Register bit description of GCI/IOM2 bus section

Timeslots for transmit direction

Name	Addr.	Bits	r/w	Function
B1_SSL	20h	4..0	w	select GCI/IOM2 bus transmission slot (0..31)
B2_SSL	21h	5	w	unused
AUX1_SSL AUX2_SSL	22h 23h	6	w	select GCI/IOM2 bus data lines '0' STIO1 output '1' STIO2 output
		7	w	transmit channel enable for GCI/IOM2 bus '0' disable (reset default) '1' enable

☝ **important!**
Enabling more than one channel on the same slot causes undefined output data.

Timeslots for receive direction

Name	Addr.	Bits	r/w	Function
B1_RSL	24h	4..0	w	select GCI/IOM2 bus receive slot (0..31)
B2_RSL	25h	5	w	unused
AUX1_RSL AUX2_RSL	26h 27h	6	w	select GCI/IOM2 bus data lines '0' STIO2 is input '1' STIO1 is input
		7	w	receive channel enable for GCI/IOM2 bus '0' disable (reset default) '1' enable

Data registers

Name	Addr.	Bits	r/w	Function
B1_D B2_D AUX1_D AUX2_D	28h 29h 2Ah 2Bh	0..7	r/w	read/write data registers for selected timeslot data

☝ **note!**
Auxiliary channel handling
If the data registers AUX1_D and AUX2_D are not overwritten, the transmisson slots AUX1_SSL and AUX2_SSL mirror the data received in AUX1_RSL and AUX2_RSL slots. This is useful for an internal connection between two CODECs. This mirroring is disabled by setting bit 1 in MST_EMOD register
In ISA-PC mode: To use the AUX1 channel the address pin SA8 must be '1' at every access to the HFC-S+. To use the AUX2 channel the address pin SA9 must be '1' at every access to the HFC-S+.

Name	Addr.	Bits	r/w	Function
MST_MODE	2Eh	0	w	GCI/IOM2 bus mode '0' slave (reset default) (C4IO and F0IO are inputs) '1' master (C4IO and F0IO are outputs)
		1	w	polarity of C4- and C2O-clock '0' F0IO is sampled on negative clock transition '1' F0IO is sampled on positive clock transition
		2	w	polarity of F0-signal '0' F0 positive pulse '1' F0 negative pulse
		3	w	duration of F0-signal '0' F0 active for one C4-clock (244ns) (reset default) '1' F0 active for two C4-clocks (488ns)
		5, 4	w	time slot for codec-A signal F1_A '00' B1 receive slot '01' B2 receive slot '10' AUX1 receive slot '11' signal C2O → pin F1_A (C2O is 2048 kHz clock)
		7, 6	w	time slot for codec-B signal F1_B '00' B1 receive slot '01' B2 receive slot '10' AUX1 receive slot '11' AUX2 receive slot

The pulse shape and polarity of the codec signals F1_A and F1_B is the same as the pulseshape of the F0IO signal. The polatity of C2O can be changed by bit 1.

RESET sets register MST_MODE to all '0's.

Name	Addr.	Bits	r/w	Function
MST_EMOD	2Dh	0	w	slow down C4IO clock adjustment (see Figure 13) '0' C4IO clock is adjusted in the 31th time slot twice for one half clock cycle (reset default) '1' C4IO clock is adjusted in the 31th time slot once for one half clock cycle
		1	w	enable/disable AUX channel mirroring '0' mirror AUX receive to AUX transmit (reset default) '1' disable AUX channel data mirroring
		2	w	unused
		5..3	w	select D-channel data flow (see also: CONNECT register) destination ← source bit 3: '0' D-HFC ← D-S/T '1' D-HFC ← D-GCI/IOM2 bit 4: '0' D-S/T ← D-HFC '1' D-S/T ← D-GCI/IOM2 bit 5: '0' D-GCI/IOM2 ← D-HFC '1' D-GCI/IOM2 ← D-S/T
		6	w	unused
		7	w	enable GCI/IOM2 write slots '0' disable GCI/IOM2 write slots; slot #2 and slot #3 may be used for normal data '1' enables slot #2 and slot #3 as master, D- and C/I-channel
C/I	02h	3..0	r/w	on read: indication on write: command
		7..4		unused
TRxR	03h	0	r	reserved
		1	r	'1' Monitor transmitter ready Writing on MON2_D starts transmisssion and resets this bit.
		5..2	r	reserved
		6	r	STIO2 in
		7	r	STIO1 in

4.4 Register bit description of CONNECT register

Name	Addr.	Bits	r/w	Function
CONNECT	2Fh	2..0	w	select B1-channel data flow destination ← source bit 0: '0' B1-HFC ← B1-S/T '1' B1-HFC ← B1-GCI/IOM2 bit 1: '0' B1-S/T ← B1-HFC '1' B1-S/T ← B1-GCI/IOM2 bit 2: '0' B1-GCI/IOM2 ← B1-HFC '1' B1-GCI/IOM2 ← B1-S/T
		5..3	w	select B2-channel data flow destination ← source bit 3: '0' B2-HFC ← B2-S/T '1' B2-HFC ← B2-GCI/IOM2 bit 4: '0' B2-S/T ← B2-HFC '1' B2-S/T ← B2-GCI/IOM2 bit 5: '0' B2-GCI/IOM2 ← B2-HFC '1' B2-GCI/IOM2 ← B2-S/T
		7..6	w	unused

RESET sets CONNECT register to all '0's.

The following figure shows the different options for switching the B-channels with the CONNECT register (similar for D-channel: see MST_EMOD register).

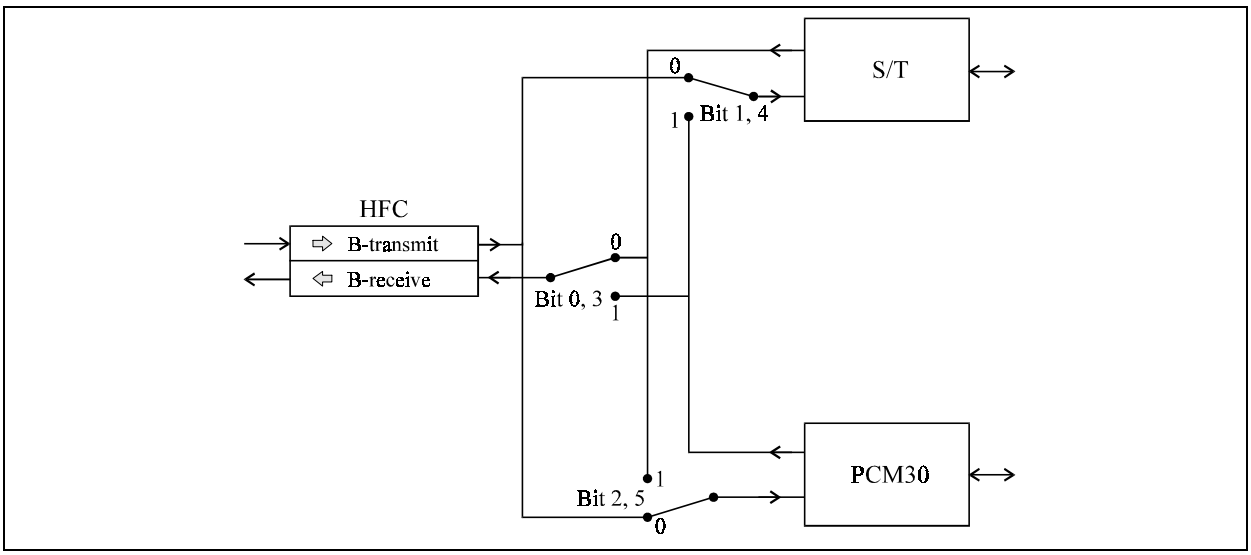


Figure 5: Function of the CONNECT register bits

4.5 Register bit description of interrupt, status and control registers

Name	Addr.	Bits	r/w	Function
CIRM	18h	2..0	w	select IRQ channel in PC mode '000' IRQ disable '001' IRQ_A '010' IRQ_B '011' IRQ_C '100' IRQ_D '101' IRQ_E '110' IRQ_F '111' IRQ disable
		3	w	soft reset, similar as hardware reset; the registers CIP, CIRM and CTMT are not changed so selected I/O address is kept in ISA-PC mode. The reset is active until the bit is cleared. '0' deactivate reset (reset default) '1' activate reset
		4	w	select memory '0' 32K x 8 external RAM (reset default) '1' 8K x 8 external RAM
		5	w	external interrupt enable '0' ext. interrupt disable, IRQ_A is output (reset default) '1' ext. interrupt enable IRQ_A is input and ored to IRQ output
		6	w	double clock mode (24.576 MHz external oscillator required) when set, all RAM accesses are double speed
		7	w	FIFO reset The currently selected FIFO is initialised. This bit is automatically cleared.

Name	Addr.	Bits	r/w	Function
CTMT	19h	0	w	HDLC/transparent mode for B1-channel '0' HDLC mode (reset default) '1' transparent mode
		1	w	HDLC/transparent mode for B2-channel '0' HDLC mode (reset default) '1' transparent mode
		4..2	w	select timer and watchdog (bit 4 = MSB) timer watchdog '000' off off '001' 3.125ms 6.25ms '010' 6.25ms 12.5ms '011' 12.5ms 25ms '100' 25ms 50ms '101' 50ms 100ms '110' 400ms 800ms '111' 800ms 1600ms
		5	w	timer/watchdog reset mode '0' reset timer/WD by CTMT bit 7 (reset default) '1' automatically reset timer/WD at each access to HFC-S+
		6	w	ignored
		7	w	reset timer/WD '1' reset timer/WD This bit is automatically cleared.
CHIP_ID	16h	3..0	r	reserved
		7..4	r	Chip identification 0001b HFC-S+
B_MODE	13h	1..0	w	unused
		2	w	in 64 kbit/s mode: bit is ignored in 56 kbit/s mode: value of the LSB in 7-bit mode
		3	w	unused
		4	w	56 kbit/s mode selection bit for B1-channel '0' 64 kbit/s mode (reset default) '1' 56 kbit/s mode
		5	w	56 kbit/s mode selection bit for B2-channel '0' 64 kbit/s mode (reset default) '1' 56 kbit/s mode
		6	w	'0' Data not inverted for B1-channel (reset default) '1' Data inverted for B1-channel
		7	w	'0' Data not inverted for B2-channel (reset default) '1' Data inverted for B2-channel

Name	Addr.	Bits	r/w	Function
INT_M1	1Ah	0	w	interrupt mask for channel B1 in transmit direction
		1	w	interrupt mask for channel B2 in transmit direction
		2	w	interrupt mask for channel D in transmit direction
		3	w	interrupt mask for channel B1 in receive direction
		4	w	interrupt mask for channel B2 in receive direction
		5	w	interrupt mask for channel D in receive direction
		6	w	interrupt mask for state change of TE/NT state machine
		7	w	interrupt mask for timer

For mask bits a '1' enables and a '0' disables interrupt. RESET clears all bits to '0'.

Name	Addr.	Bits	r/w	Function
INT_M2	1Bh	0	w	interrupt mask for processing/non processing phase transition
		1	w	interrupt mask for GCI I-change
		2	w	interrupt mask for GCI monitor receive
		3	w	enable for interrupt output ('1' = enable)
		4	w	interrupt output is reversed
		5	w	interrupt from external device is reversed
		7..6	w	unused

For mask bits a '1' enables and a '0' disables interrupt. RESET clears all bits to '0'.

Name	Addr.	Bits	r/w	Function
TRM	12h	1..0	w	interrupt in transparent mode is generated if Z1 in receive FIFOs or Z2 in transmit FIFOs change from: 00: x xxxx x011 1111 → x xxxx x100 0000 01: x xxxx 0111 1111 → x xxxx 1000 0000 10: x xxx0 1111 1111 → x xxx1 0000 0000 11: x 0111 1111 1111 → x 1000 0000 0000
		4..2	w	must be '0'
		5	w	E → B2 receive channel When set the E receive channel of the S/T interface is connected to the B2 receive channel.
		6	w	B1+B2 mode '0' normal operation (reset default) '1' B1+B2 are combined to one HDLC or transparent channel. All settings for data shape and connect are derived from B1.
		7	w	IOM test loop When set MST output data is looped to the MST input.

Name	Addr.	Bits	r/w	Function
INT_S1	1Eh	0	r	B1-channel interrupt status in transmit direction
		1	r	B2-channel interrupt status in transmit direction in HDLC mode: '1' a complete frame has been transmitted, the frame counter F2 has been incremented in transparent mode: '1' interrupt as selected in TRM register bits 1..0
		2	r	D-channel interrupt status in transmit direction '1' a complete frame was transmitted, the frame counter F2 was incremented
		3	r	B1-channel interrupt status in receive direction
		4	r	B2-channel interrupt status in receive direction in HDLC mode: '1' a complete frame has been transmitted, the frame counter F1 has been incremented in transparent mode: '1' interrupt as selected in TRM register bits 1..0
		5	r	D-channel interrupt status in receive direction '1' a complete frame was received, the frame counter F1 was incremented
		6	r	TE/NT state machine interrupt status '1' state of state machine changed
		7	r	timer interrupt status '1' timer is elapsed
INT_S2	1Fh	0	r	processing/non processing transition interrupt status '1' The HFC-S+ has changed from processing to non processing state.
		1	r	GCI I-change interrupt '1' a different I-value on GCI was detected
		2	r	receiver ready (RxR) of monitor channel '1' 2 monitor bytes have been received
		7	r	unused, '0'

☝ **important!**
Reading the INT_S1 or INT_S2 register resets all active read interrupts in the INT_S1 or INT_S2 register. New interrupts may occur during read. These interrupts are reported at the next read of INT_S1 or INT_S2.
All interrupt bits are reported regardless of the mask registers settings (INT_M1 and INT_M2). The mask register settings only influence the interrupt output condition.
The interrupt output goes inactive during the read of INT_S1 or INT_S2. If interrupts occur during this read the interrupt line goes active immediately after the read is finished. So processors with level or transition triggered interrupt inputs can be connected.

Name	Addr.	Bits	r/w	Function
STATUS	1Ch	0	r	BUSY/NOBUSY status '1' the HFC-S+ is BUSY after initialising Reset FIFO, increment F or change FIFO '0' the HFC-S+ is not busy, all accesses are allowed
		1	r	processing/non processing status '1' the HFC-S+ is in processing phase (every 125µs) '0' the HFC-S+ is not in processing phase
		2	r	processing/non processing transition interrupt status '1' The HFC-S+ has finished internal processing phase (every 125µs)
		3	r	unused, '0'
		4	r	timer status '0' timer not elapsed '1' timer elapsed
		5	r	TE/NT state machine interrupt state '1' state of state machine has changed
		6	r	FRAME interrupt has occured (any data channel interrupt) all masked D-channel and B-channel interrupts are "ored"
		7	r	ANY interrupt all masked interrupts are "ored"

Reading the STATUS register clears no bit.

5 Electrical characteristics

Absolute maximum ratings

Parameter	Symbol	Rating
Supply voltage	V_{DD}	-0.3V to +7.0V
Input voltage	V_I	-0.3V to V_{CC} + 0.3V
Output voltage	V_O	-0.3V to V_{CC} + 0.3V
Operating temperature	T_{opr}	-10°C to +85°C
Storage temperature	T_{stg}	-40°C to +125°C

Recommended operating conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.
Supply voltage	V_{DD}	V_{DD}=5V V_{DD}=3.3V	4.75V 3.15V	5.0V 3.3V	5.25V 3.45V
Operating temperature	T_{opr}		0°C		+70°C
Supply current normal power down	I_{DD}	f_{CLK}=12.288MHz V_{DD} = 5V, running oscillator: V_{DD} = 3.3V, running oscillator: oscillator stopped*):		25mA 8mA < 1mA	

*) see also: 3.9 Power down considerations

Electrical characteristics for 5V power supply

V_{DD} = 4.75V to 5.25V, T_{opr} = 0°C to +70°C

Parameter	Symbol	Condition	TTL level			CMOS level		
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Input LOW voltage	V_{IL}				0.8V			1.0V
Input HIGH voltage	V_{IH}		2.0V			3.5V		
Output LOW voltage	V_{OL}				0.4V			0.4V
Output HIGH voltage	V_{OH}		4.3V			4.3V		
Output leakage current	$\lvert I_{OZ} \rvert$	High Z			10µA			10µA
Pull-up resistor input current	$\lvert I_{IL} \rvert$	$V_I = V_{SS}$		50µA			50µA	

Electrical characteristics for 3.3V power supply

V_{DD} = 3.15V to 3.45V, T_{opr} = 0°C to +70°C

Parameter	Symbol	Condition	TTL level			CMOS level		
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Input LOW voltage	V_{IL}				0.8V			1.0V
Input HIGH voltage	V_{IH}		2.0V			2.3V		
Output LOW voltage	V_{OL}				0.4V			0.4V
Output HIGH voltage	V_{OH}		2.4V			2.4V		

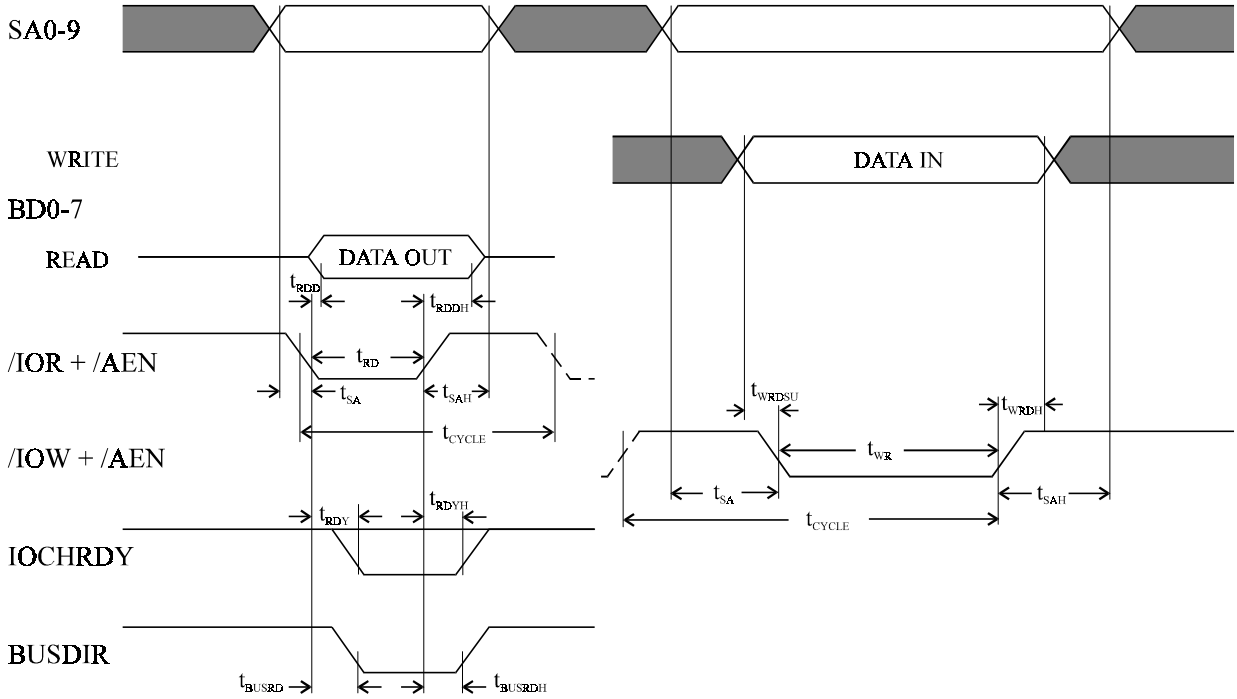
I/O Characteristics

Input	Interface Level
IIOSEL0-3	TTL, internal pull-up resistor
SA0-9	TTL
/AEN	TTL
/IOR	TTL
/IOW	TTL
BD0-7	TTL
ALE	TTL
SRD0-7	TTL
C4IO	TTL, internal pull-up resistor
F0IO	TTL, internal pull-up resistor
STIO1-2	TTL, internal pull-up resistor
IRQ_A	TTL (as IRQ input)
RESET	CMOS Schmitt Trigger

	Driver Capability		
	Low		High
Output	**0.4V**	**0.6V**	**V_{DD} - 0.4V**
IOCHRDY	6mA		
BD0-7	18mA	24mA	8mA
BUSDIR	4mA		2mA
TX2_HI	4mA		2mA
/TX1_LO	12mA		
/TX_EN	4mA		2mA
/TX2_LO	12mA		
TX1_HI	4mA		2mA
ADJ_LEV	1mA		0.5mA
SRD0-7	4mA		2mA
SRA0-14	2mA		1mA
/SRRD	4mA		2mA
/SRCS	4mA		2mA
/SRWE	4mA		2mA
C4IO	6mA		3mA
F0IO	6mA		3mA
STIO1-2	6mA		3mA
F1_A-B	6mA		3mA
IRQA-F	6mA		3mA

6 Timing characteristics

6.1 ISA-PC bus or processor access



Timing diagram 1: ISA-PC bus or microprocessor access

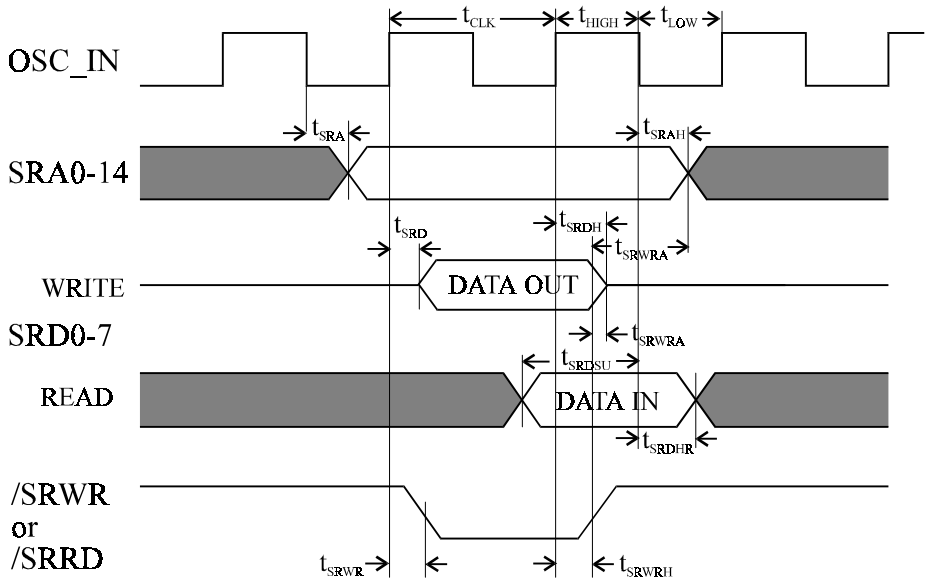
SYMBOL	CHARACTERISTICS	MIN.	MAX.
t_{RDD}	/IOR Low to Read Data Out Time	3ns	25ns
t_{RDDH}	/IOR High to Data Buffer Turn Off Time	2ns	15ns
t_{SA}	Address to /IOR or /IOW Low Setup Time	20ns	–
t_{SAH}	Address Hold Time after /IOR or /IOW High	20ns	–
t_{RD}	Read Time	50ns	∞
t_{WR}	Write Time	50ns	∞
t_{WRDSU}	Write Data Setup Time to /IOW Low	30ns	∞
t_{WRDH}	Write Data Hold Time from /IOW High	10ns	–
t_{RDY}	Delay Time from /IOR or /IOW Low to IOCHRDY Low	3ns	30ns
t_{RDYH}	Delay Time from /IOR Low or /IOW High to IOCHRDY High	3ns	30ns
t_{BUSRD}	Delay Time from /IOR Low to BUSDIR Low	3ns	25ns
t_{BUSRDH}	Delay Time from /IOR High to BUSDIR High	2ns	15ns

SYMBOL	CHARACTERISTICS	MIN.	MAX.
t_{CYCLE}	Read/Write cycle	6 x t_{CLK}	–

important!

For write accesses to the HFC-S+ the data lines must be stable and valid **before** /IOW or /DS get low. With Intel compatible processors it may be neccessary to delay the /IOW or /DS signals.

6.2 SRAM access



Timing diagram 2: SRAM access

SYMBOL	CHARACTERISTICS	MIN.	MAX.
f_{CLK}	OSC_IN frequency	12.288MHz	24.576MHz *)
$\Delta f_{CLK} / f_{CLK}$	Relative OSC_IN frequency deviation	0	$\pm 10^{-4}$
t_{CLK}	OSC_IN Cycle Time	$1/ f_{CLK}$	–
t_{LOW} **)	OSC_IN Low Level Width	$t_{CLK} / 3$	–
t_{HIGH} **)	OSC_IN High Level Width	$t_{CLK} / 3$	–
t_{SRA}	Address Stable after OSC_IN ↓	2ns	15ns
t_{SRAH}	Address Stable Hold Time after OSC_IN ↓	1ns	–
t_{SRD}	Data Out Stable after OSC_IN ↑	10ns	30ns

SYMBOL	CHARACTERISTICS	MIN.	MAX.
t_{SRDH}	Data Out Stable Hold Time after OSC_IN ↑	5ns	–
t_{SRDSU}	Data In Setup Time to OSC_IN ↓	20ns	–
t_{SRDHR}	Data In Hold Time after OSC_IN ↓	0ns	–
t_{SRWR}	Delay Time OSC_IN ↑ to /SRWR Low	5ns	15ns
t_{SRWRH}	Delay Time OSC_IN ↑ to /SRWR High	5ns	15ns
t_{SRWRA}	Data Hold Time after /SRWR ↑	1ns	–
t_{SRWRA}	Address Hold Time after /SRWR ↑	t_{CLK} / 3	–

*) Double clock mode with 24.576MHz
**) OSC_IN should be symmetrical so $t_{LOW} = t_{HIGH}$

6.3 GCI/IOM2 bus clock and data alignment for Mitel ST™ bus

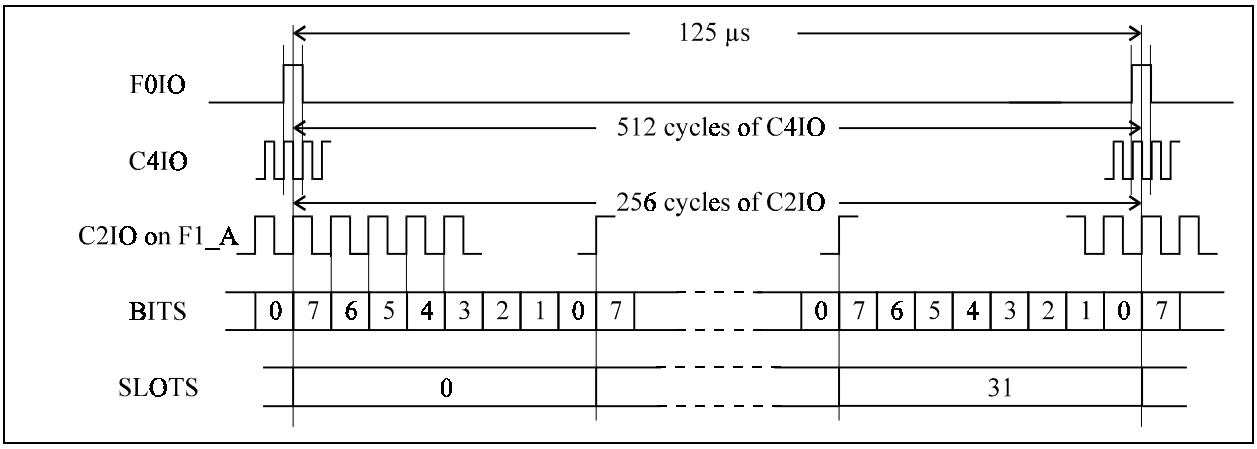
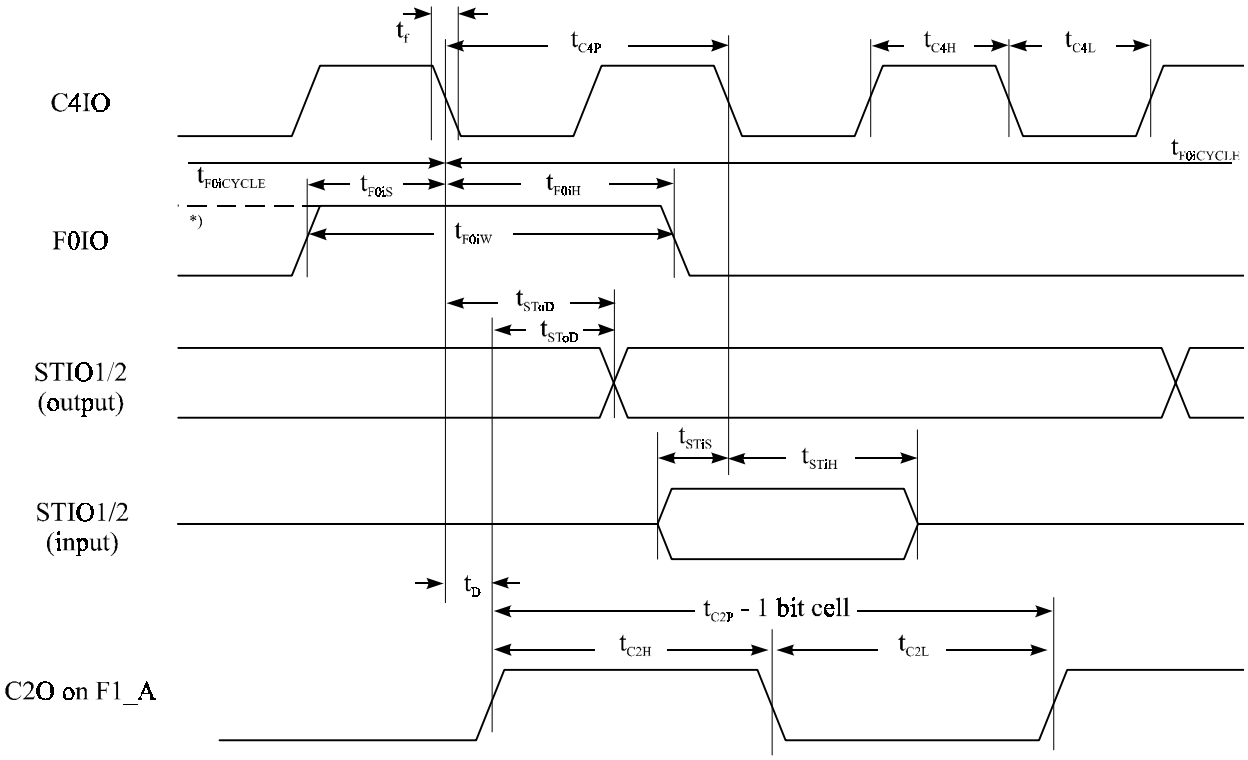


Figure 6: GCI/IOM2 bus clock and data alignment

6.4 GCI/IOM2 timing



Timing diagram 3: GCI/IOM2 timing

*) F0IO starts one C4IO clock earlier if bit 3 in MST_MODE register is set. If this bit is set F0IO is also awaited one C4IO clock cycle earlier.

6.4.1 Master mode

To configure the HFC-S+ as GCI/IOM2 bus master bit 0 of the MST_MODE register must be set. In this case C4IO and F0IO are outputs.

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.
t_{C4P}	Clock C4IO period (4.096 MHz)	180 ns *)	244.14 ns*)	308 ns*)
t_{C4H}	Clock C4IO High Width	78 ns *)	122 ns *)	166 ns*)
t_{C4L}	Clock C4IO Low Width	78 ns *)	122 ns *)	166 ns *)
t_{C2P}	Clock C2O Period	360 ns	488.28 ns	616 ns
t_{C2H}	Clock C2O High Width	180 ns	244.14 ns	308 ns
t_{C2L}	Clock C2O Low Width	180 ns	244.14 ns	308 ns

SYMBOL	CHARACTERISTICS		MIN.	TYP.	MAX.
t_{F0iW}	F0IO Width	Short F0IO	230 ns	244 ns	260 ns
		Long F0IO	460 ns	488 ns	520 ns
t_{SToD}	STIO1/2 Delay fom C4IO ↓ Level 1 Output			10 ns	25 ns
$t_{F0iCYCLE}$	F0IO Cycle Time	1 half clock adjust	124.955 us	125.000 us	125.045 us
		2 half clocks adjust	124.910 us	125.000 us	125.090 us

All specifications are for 2.048 Mb/s Streams and f_{CLK} = 12.288 Mhz.

*) Time depends on accuracy of OSC_IN frequency. Because of clock adjustment in the 31st time slot these are the worst case timings when C4IO is adjusted.

6.4.2 Slave mode

To configure the HFC-S+ as GCI/IOM2 bus slave bit 0 of the MST_MODE register must be cleared (reset default). In this case C4IO and F0IO are inputs.

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.
t_{C4P}	Clock C4IO period (4.096 MHz)		244.14 ns*)	
t_{C4H}	Clock C4IO High Width	20 ns		
t_{C4L}	Clock C4IO Low Width	20 ns		
t_{C2P}	Clock C2O Period		488.28 ns*)	
t_{C2H}	Clock C2O High Width	25 ns		
t_{C2L}	Clock C2O Low Width	25 ns		
t_{F0iS}	F0IO Setup Time to C4IO ↓	20 ns		
t_{F0iH}	F0IO Hold Time after C4IO ↓	20 ns		
t_{F0iW}	F0IO Width	40 ns		
t_{STiS}	STIO2 Setup Time	20 ns		
t_{STiH}	STIO2 Hold Time	20 ns		

All specifications are for 2.048 Mb/s Streams and f_{CLK} = 12.288 Mhz.

*) If the S/T interface is synchronized from C4IO (NT mode) the frequency must be stable to $\pm 10^{-4}$.

7 S/T interface circuitry

In order to comply to the physical requirements of ITU-T recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the HFC-S+ needs some additional circuitry, which are shown in the following figures.

7.1 External receiver circuitry

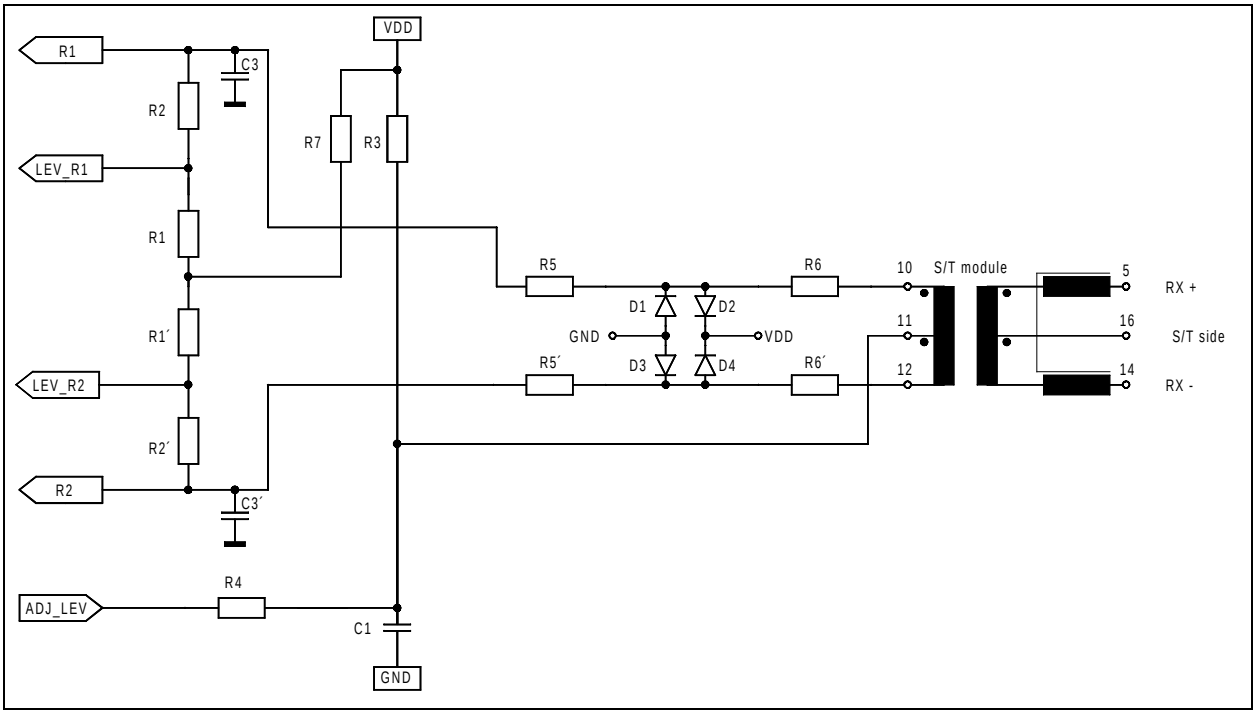


Figure 7: External receiver circuitry

Part list

VDD	**5V**	**3.3V**
R1, R1'	33 kΩ	
R2, R2'	100 kΩ	
R3	1 MΩ	680 kΩ
R4	3.9 kΩ	
R5, R5'	4.7 kΩ	
R6, R6'	4.7 kΩ	
R7	1.8 MΩ	1.2 MΩ

C1	47 nF
C3, C3'	22 pF
D1, D2	1N4148 or LL4148
D3, D4	1N4148 or LL4148
S/T module	see Table 5 on page 59

C3, C3' are for reduction of high frequency input noise and should be located as close as possible to the HFC-S+.

7.2 External transmitter circuitry

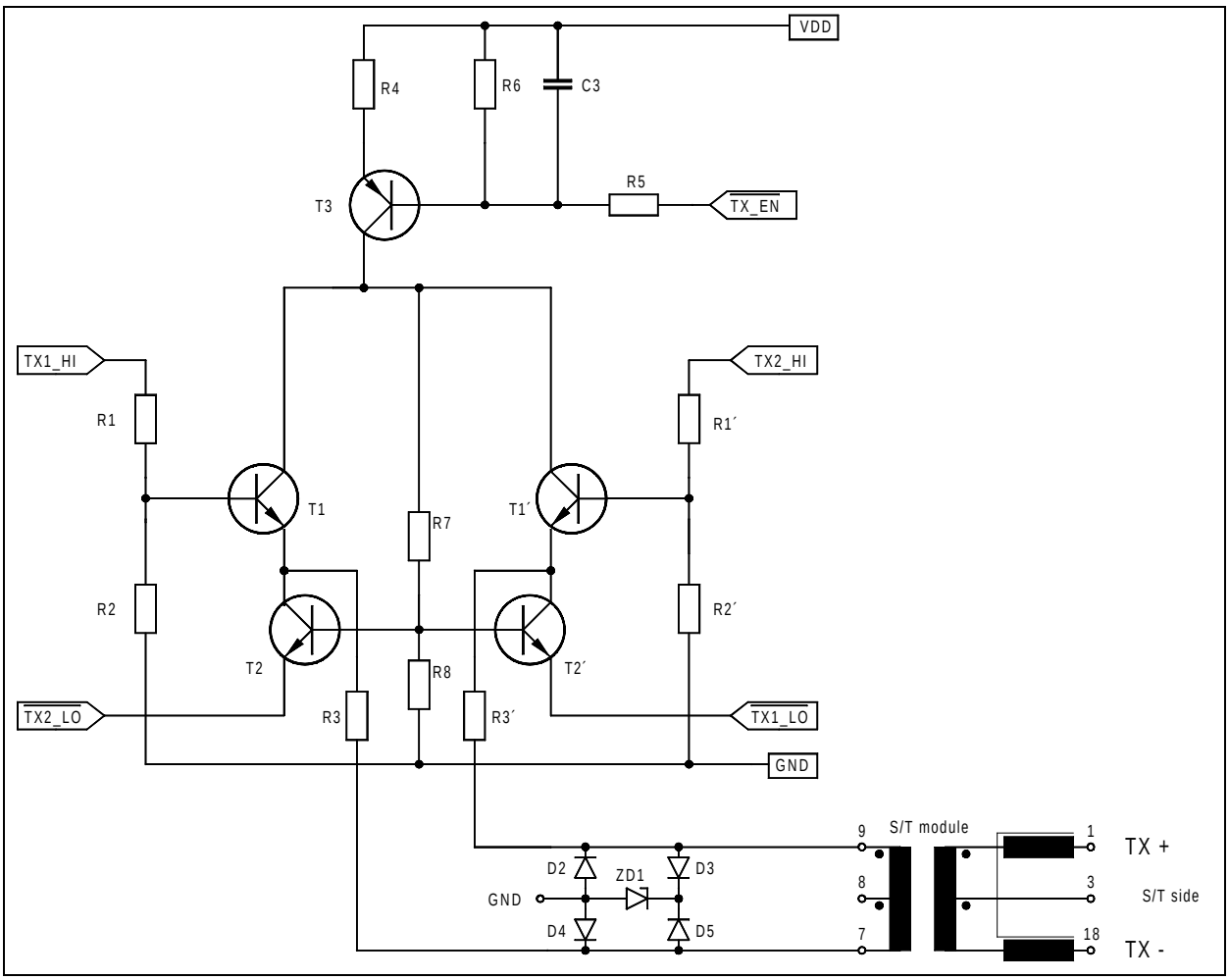


Figure 8: External transmitter circuitry

Part List

VDD	**5V**	**3.3V**
R1	2.2 kΩ ± 1%	560 Ω
R2	3.0 kΩ ± 1%	3.9 kΩ ± 1%
R3, R3' *)	18 Ω	18 Ω
R4	100 Ω	50 Ω
R5	5.6 kΩ	3.3 kΩ
R6	3.3 kΩ	2.2 kΩ
R7	3.3 kΩ	1.8 kΩ
R8	2.2 kΩ	2.2 kΩ

C3	470 pF
D2, D3	1N4148 or LL4148
D4, D5	1N4148 or LL4148
ZD1	Z-Diode 2.7 V (e. g. BZV 55C 2V7)
T1, T1'	BC550C, BC850C or similar
T2, T2'	BC550C, BC850C or similar
T3	BC560C, BC860C or similar
S/T module	see Table 5 on page 59

*) value is depending on the used S/T module

S/T module part number	manufacturer
APC 56624-1 S-Hybrid modules with receiver and transmitter circuitry included: APC 5568-3V APC 5568-5V APC 5568DS-3V APC 5568DS-5V	**Advanced Power Components** *United Kingdom* Phone: +44 1634-290-588 Fax: +44 1634-290-591 http://www.apcisdn.com
FE 8131-55Z	**FEE GmbH** *Singapore* Phone: +65 741-5277 Fax: +65 741-3013 *Bangkok* Phone: +662 718-0726-30 Fax: +662 718-0712 *Germany* Phone: +49 6106-82980 Fax: +49 6106-829898
transformers: PE-64995 PE-64999 PE-65795 PE-65799 PE-68995 PE-68999 T5006 T5007 S_0-modules: T5012 T5034 T5038	**Pulse Engineering, Inc.** *United States* Phone: +1-619-674-8100 Fax: +1-619-674-8262 http://www.pulseeng.com
transformers: SM TC-9001 SM ST-9002 SM ST-16311F S_0-modules: SM TC-16311 SM TC-16311A	**Sun Myung** *Korea* Phone: +82-348-943-8525 Fax: +82-348-943-8527 http://www.sunmyung.com
transformers UT21023 S_0-modules: UT 21624 UT 28624 A	**UMEC GmbH** *Germany* Phone: +49 7131-7617-0 Fax: +49 7131-7617-20 *Taiwan* Phone: +886-4-359-009-6 Fax: +886-4-359-012-9 *United States* Phone: +1-310-326-7072 Fax: +1-310-326-7058 http://www.umec.de

S/T module part number	manufacturer
T 6040... transformers: 3-L4021-X066 3-L4025-X095 3-L5024-X028 3-L4096-X005 3-L5032-X040 S_0-modules: 7-L5051-X014 7-M5051-X032 7-L5052-X102 7-M5052-X110 7-M5052-X114	**VAC GmbH** *Germany* Phone: +49 6181/ 38-0 Fax: +49 6181/ 38-2645 http://www.vacuumschmelze.de
transformers: ST5069 S_0-modules: PT5135 ST5201 ST5202	**Valor Electronics, Inc.** *Asia* Phone: +852 2333-0127 Fax: +852 2363-6206 *North America* Phone: +1 800 31VALOR Fax: +1 619 537-2525 *Europe* Phone: +44 1727-824-875 Fax: +44 1727-824-898 http://www.valorinc.com
543 76 009 00	**Vogt electronic AG** *Germany* Phone: +49 8591/ 17-0 Fax: +49 8591/ 17-240 http://www.vogt-electronic.com

Table 5: S/T module part numbers and manufacturer

7.3 Oscillator circuitry

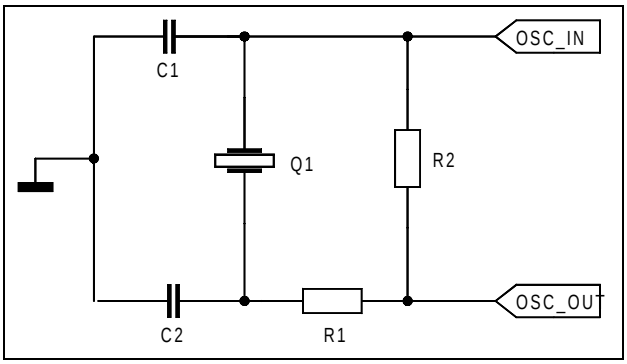


Figure 9: Oscillator Circuitry

Part list:

Q1	12.288 MHz quartz
R1	0..50 Ω
R2	1 MΩ
C1, C2	47 pF

The values of C1, C2 and R1, R2 depend on the used quartz.

For a load-free check of the oscillator frequency the C4O clock of the GCI/IOM2 bus should be measured (HFC-S+ as master, S/T interface deactivated, 4.096 MHz frequency intented on the C4IO).

The input signal on OSC_IN should be as big as possible.

8 State matrices for NT and TE

8.1 S/T interface activation/deactivation layer 1 for finite state matrix for NT

State name / State number / Event / INFO sent	Reset G0 INFO 0	Deactive G1 INFO 0	Pending activation G2 INFO 2	Active G3 INFO 4	Pending deactivation G4 INFO 0
State machine release (Note 3)	G2	|	|	|	|
Activate request	G2 (Note 1)	G2 (Note 1)	|	|	G2 (Note 1)
Deactivate request	—	|	Start timer T2 G4	Start timer T2 G4	|
Expiry T2 (Note 2)	—	—	—	—	G1
Receiving INFO 0	—	—	—	G2	G1
Receiving INFO 1	—	G2 (Note 1)	—	/	—
Receiving INFO 3	—	/	G3 (Note 1)	—	—

Table 6: Activation/deactivation layer 1 for finite state matrix for NT

— No state change
/ Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons
| Impossible by the definition of the physical layer service

Note 1: Timer 1 (T1) is not implemented in the HFC-S+ and must be implemented in software.

Note 2: Timer 2 (T2) prevents unintentional reactivation. Its value is 32ms (256 x 125µs). This implies that a TE has to recognize INFO 0 and to react on it within this time.

Note 3: After reset the state machine is fixed to G0.

☝ **hint!**

Fix the NT state machine to state G3 when activated (by writing 13h into STATES register). This prevents deactivation of NT mode S/T interface due to sporadically errors on NT input data.

8.2 Activation/deactivation layer 1 for finite state matrix for TE

Event \ State name		Reset	Sensing	Deactivated	Awaiting signal	Identifying input	Synchronized	Activated	Lost framing
Event \ State number		F0	F2	F3	F4	F5	F6	F7	F8
Event \ Info sent		INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
State machine release (Note 1)		F2	/	/	/	/	/	/	/
Activate Request	Receiving any signal	—	|	F5	|	|	—	|	—
	Receiving INFO 0	—	|	F4	|	|	—	|	—
Expiry T3 (Note 5)		—	/	—	F3	F3	F3	—	—
Receiving INFO 0		—	F3	—	—	—	F3	F3	F3
Receiving any signal (Note 2)		—	—	—	F5	—	/	/	—
Receiving INFO 2 (Note 3)		—	F6	F6	F6	F6	—	F6	F6
Receiving INFO 4 (Note 3)		—	F7	F7	F7	F7	F7	—	F7
Lost framing (Note 4)		—	/	/	/	/	F8	F8	—

Table 7: Activation/deactivation layer 1 for finite state matrix for TE

— No change, no action
| Impossible by the definition of the layer 1 service
/ Impossible situation

Notes

Note 1: After reset the state machine is fixed to F0.

Note 2: This event reflects the case where a signal is received and the TE has not (yet) determined wether it is INFO 2 or INFO 4.

Note 3: Bit- and frame-synchronisation achieved.

Note 4: Loss of Bit- or frame-synchronisation.

Note 5: Timer 3 (T3) is not implemented in the HFC-S+ and must be implemented in software.

9 Binary organisation of the frames

9.1 S/T frame structure

The frame structures on the S/T interface are different for each direction of transmission. Both structures are illustrated in Figure 10.

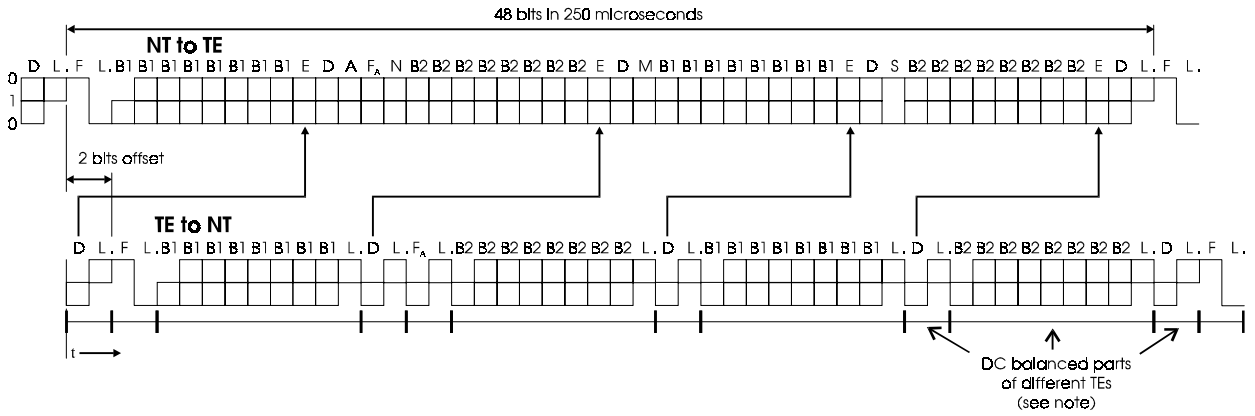


Figure 10: Frame structure at reference point S and T

F	Framing bit	N	Bit set to a binary value N = $\overline{F}_A$ (NT to TE)
L	D.C. balancing bit	B1	Bit within B-channel 1
D	D-channel bit	B2	Bit within B-channel 2
E	D-echo-channel bit	A	Bit used for activation
F_A	Auxiliary framing bit	S	S-channel bit
M	Multiframing bit		

☝ **note!**
Lines demarcate those parts of the frame that are independently d.c.-balanced.
The F_A bit in the direction TE to NT is used as Q bit in every fifth frame if S/Q bit transmission is enabled (see SCTRL register).
The nominal 2-bit offset is as seen from the TE. The offset can be adjusted with the CLKDEL register in TE mode. The corresponding offset at the NT may be greater due to delay in the interface cable and varies by configuration.
HDLC-B-channel data start with the LSB, PCM-B-channel data start with the MSB.

9.2 GCI frame structure

The binary organistation of a single GCI channel frame is described below. C4IO clock frequency is 4.096MHz.

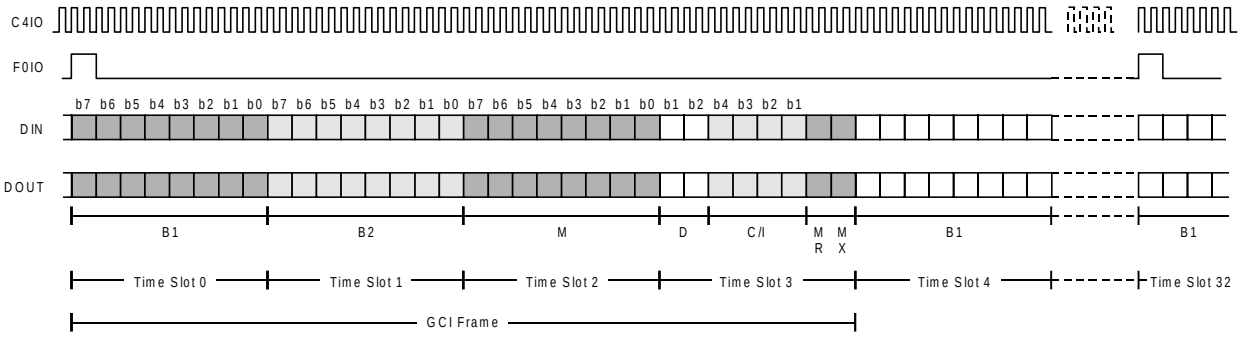


Figure 11: Single channel GCI format

B1 B-channel 1 data
B2 B-channel 2 data
M Monitor channel data
D D-channel data
C/I Command/indication bits for controlling activation/deactivation and for additional control functions
MR Handshake bit for monitor channel
MX Handshake bit for monitor channel

10 Clock synchronisation

10.1 Clock synchronisation in NT-mode

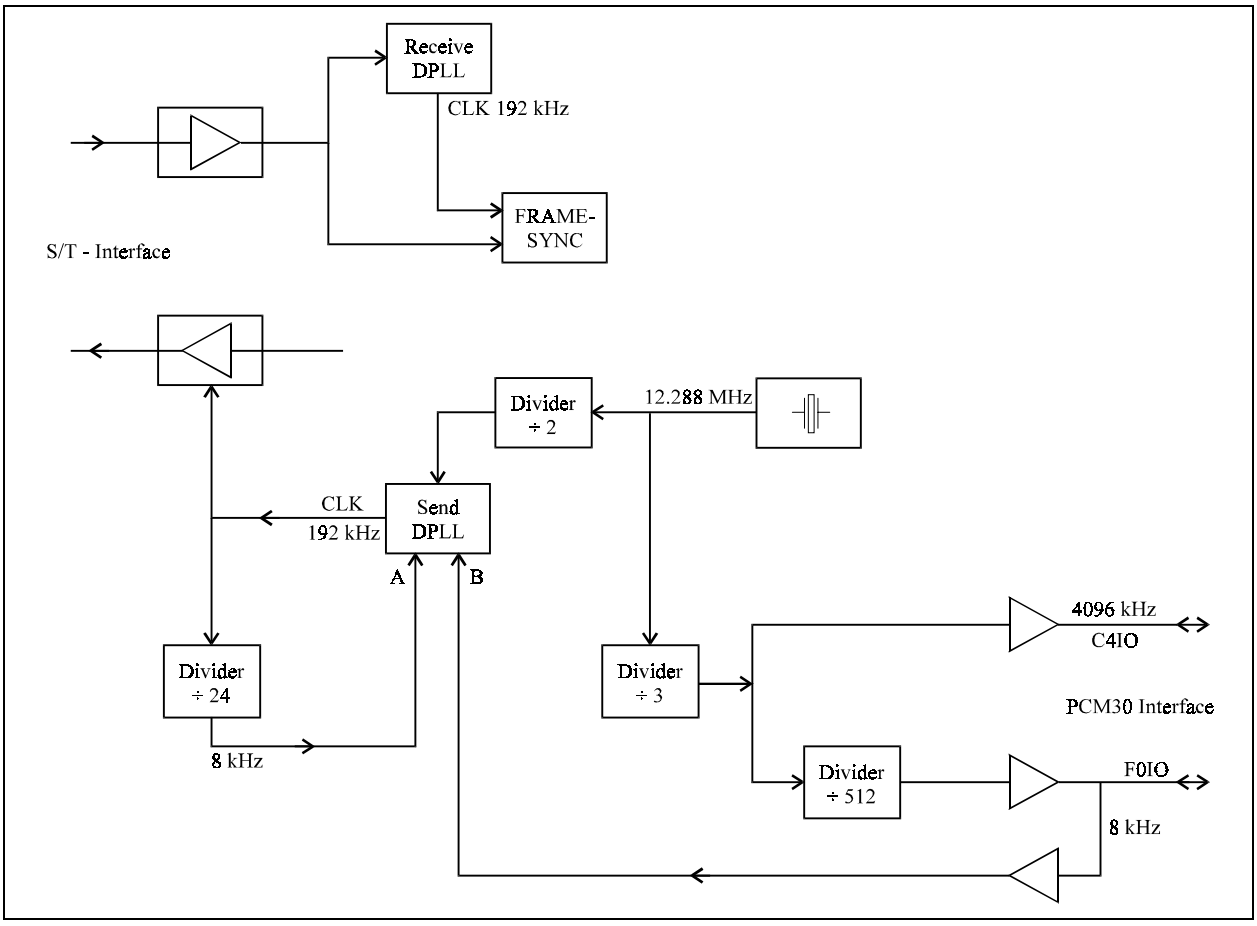


Figure 12: Clock synchronisation in NT-mode

10.2 Clock synchronisation in TE-mode

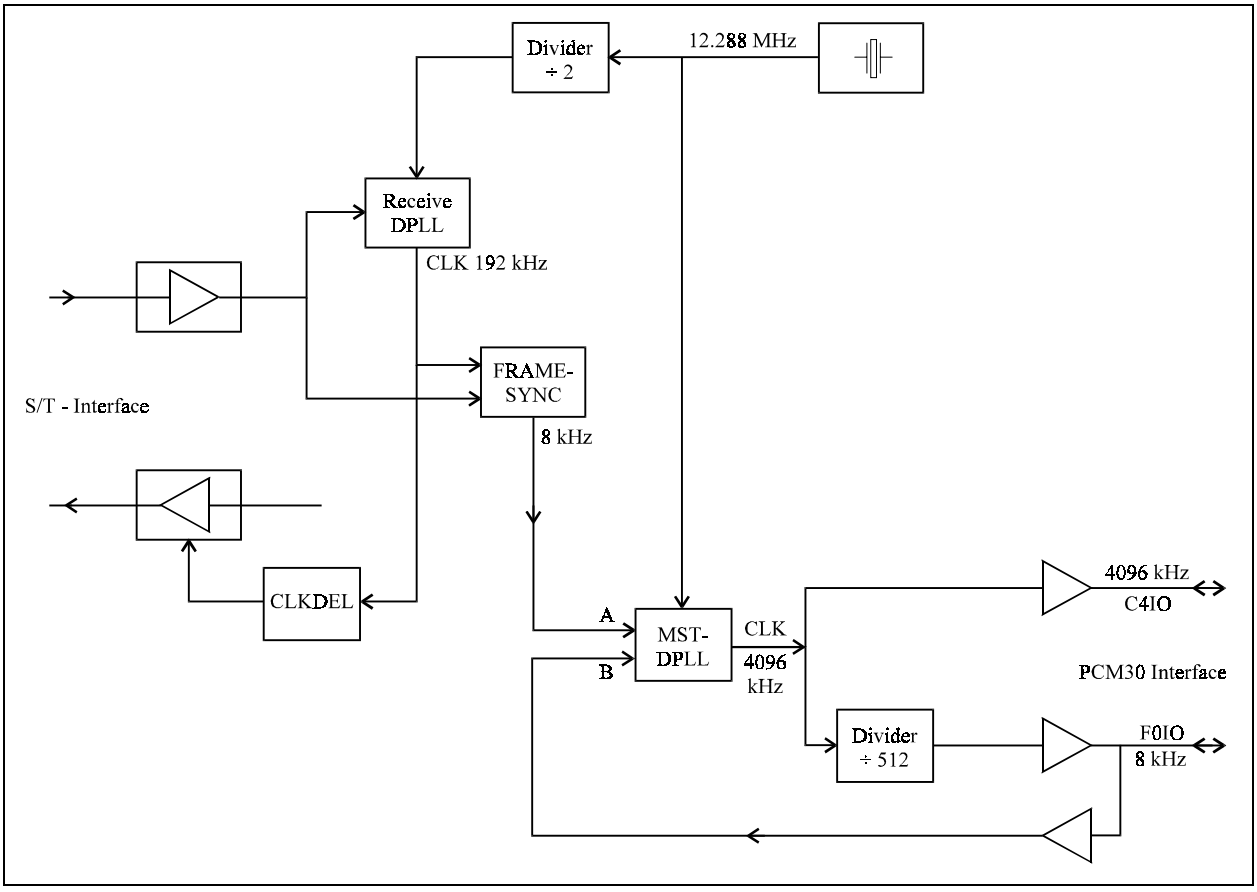


Figure 13: Clock synchronisation in TE-mode

The C4IO clock is adjusted in the 31th time slot at the GCI/IOM bus twice for one half clock cycle. This can be reduced to one adjustment of a half clock cycle. This is useful if another HFC-S, HFC-SP or HFC-S+ is connected as slave in NT mode to the GCI/IOM2 bus.

11 HFC-S+ package dimensions

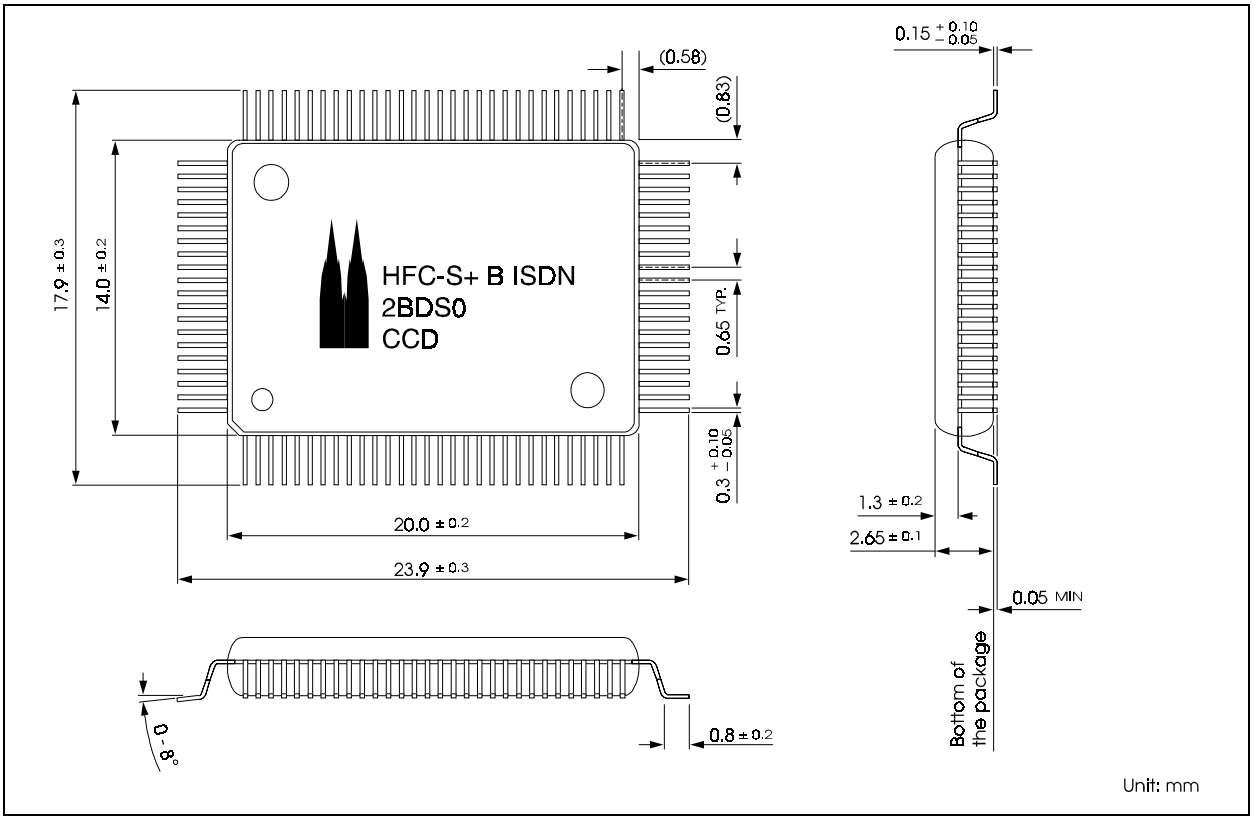
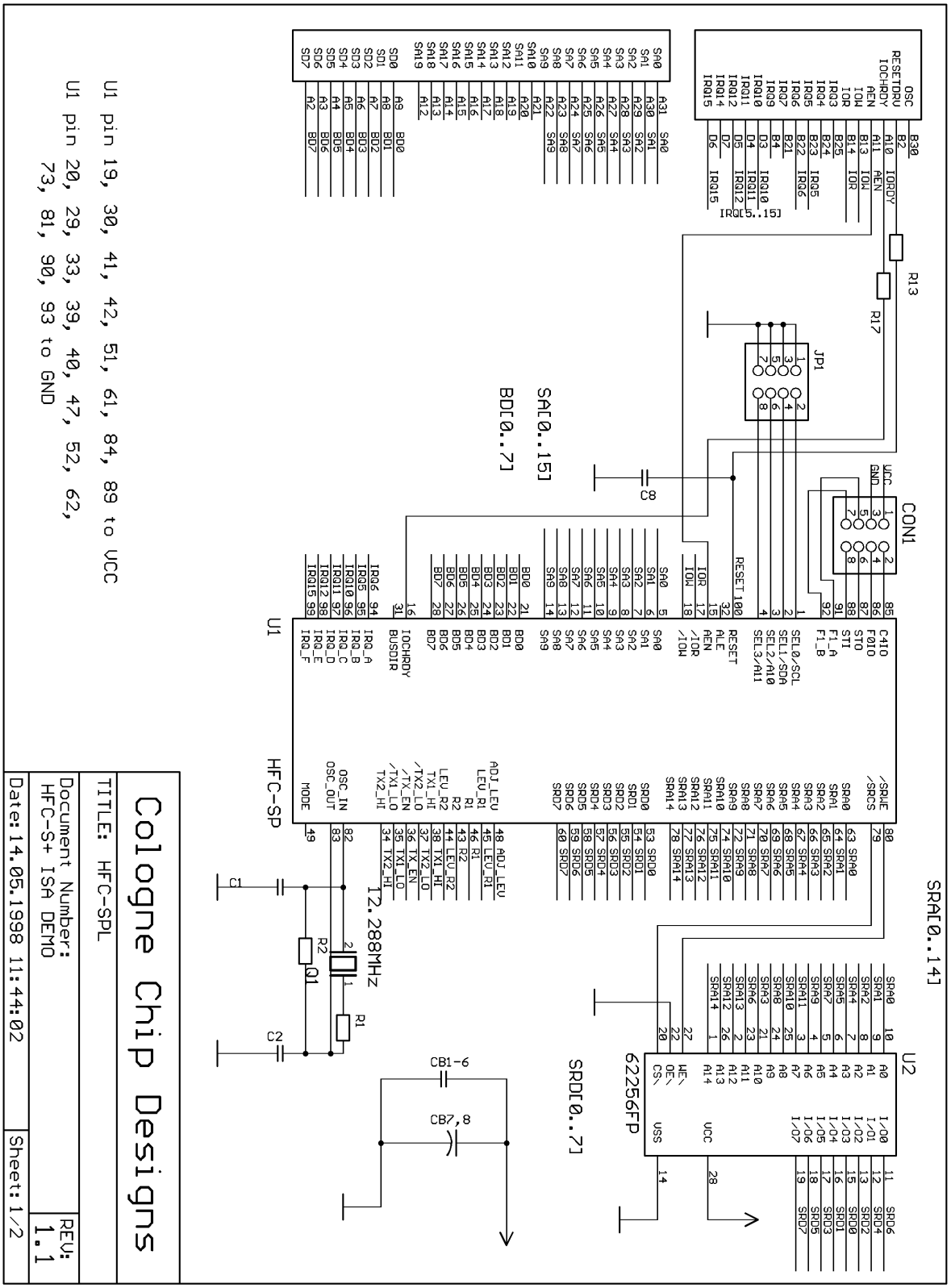
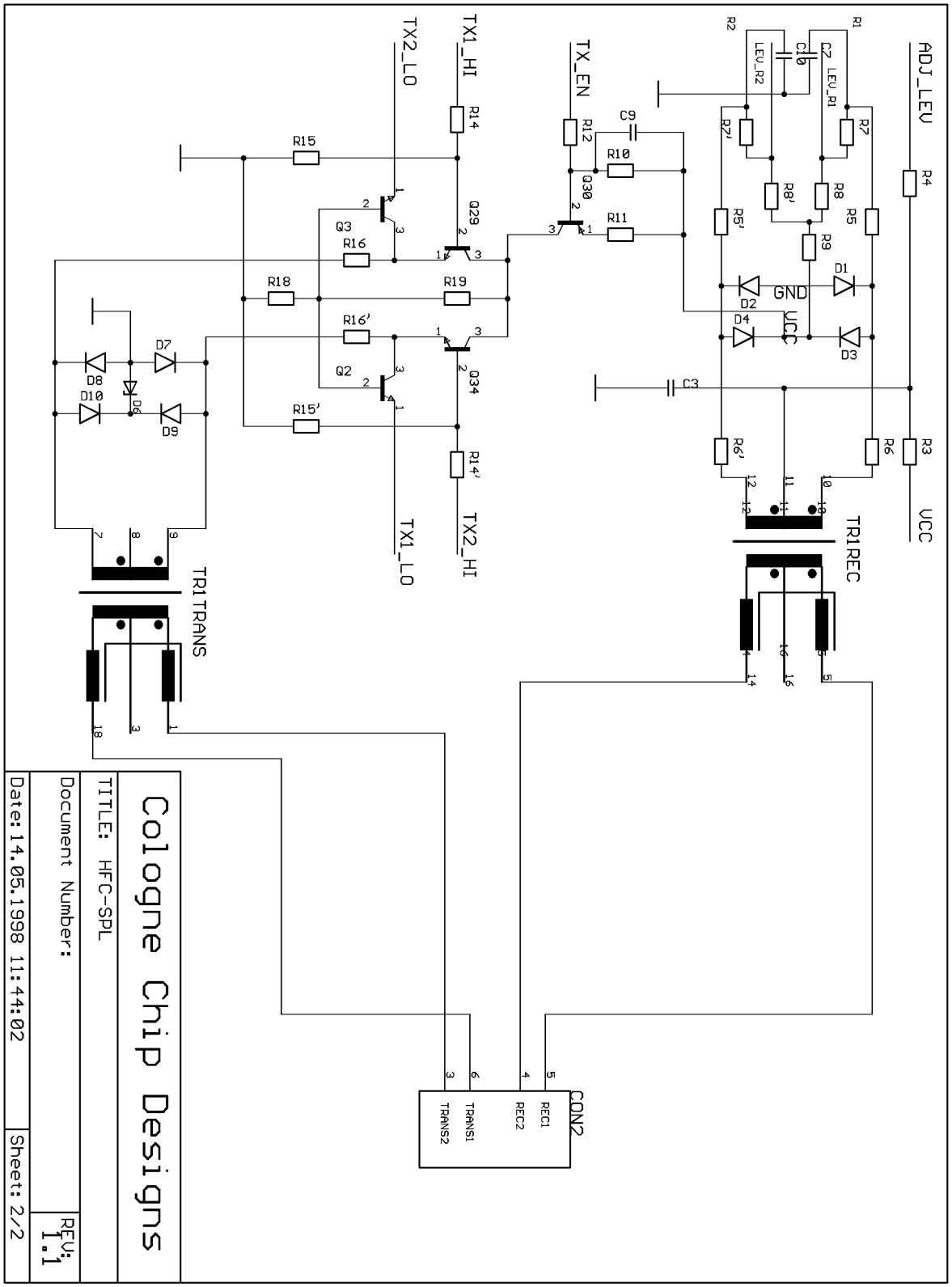


Figure 14: HFC-S+ package dimensions

12 ISDN PC card sample circuitry with HFC-S+




ADJ_LEV
VCC
TX_EN
TX1_HI
TX2_LO
TX1_LO
TX2_HI
GND
VCC
TR1REC
TR1TRANS
CON2
REC1
REC2
TRANS1
TRANS2
Cologne Chip Designs
TITLE: HFC-SPL
Document Number:
Date: 14.05.1998 11:44:02
Sheet: 2/2
REV: 1.1

Part List

Part	Value
C1	47pF *)
C2	47pF *)
C3	47nF
C7	optional
C8	1nF
C9	470pF
C10	optional
CB1	33nF
CB2	33nF
CB3	33nF
CB4	33nF
CB5	33nF
CB6	33nF
CB7	22µF
CB8	22µF
D1	LL4148
D2	LL4148
D3	LL4148
D4	LL4148
D6	2V7
D7	LL4148
D8	LL4148

Part	Value
D9	LL4148
D10	LL4148
Q1	12.288MHz
Q2	BC850C
Q3	BC850C
Q29	BC850C
Q30	BC860C
Q34	BC850C
R1	50Ω *)
R2	1MΩ *)
R3	1MΩ
R4	3.9kΩ
R5	4.7kΩ
R5'	4.7kΩ
R6	4.7kΩ
R6'	4.7kΩ
R7	100kΩ
R7'	100kΩ
R8	33kΩ
R8'	33kΩ
R9	1.8MΩ
R10	3.3kΩ

Part	Value
R11	100Ω
R12	5.6kΩ
R13	100kΩ
R14	2.2kΩ ±1%
R14'	2.2kΩ ±1%
R15	3.0kΩ ±1%
R15'	3.0kΩ ±1%
R16	18Ω
R16'	18Ω
R17	15Ω
R18	2.2kΩ
R19	3.3kΩ
TR1	S/T module
JP1	PINHD-2X4
CON1	PINHD-2X4
CON2	WESTERN
CON3	ISA
U1	HFC-S+
U2	62256FP

*) values are depending on the used quarz oscillator