Preliminary Data Sheet
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Lucent Technologies
Bell Labs Innovations

T7903 ISA Multiport Wide Area Connection (ISA-MWAC) Device

Features

- Three wide area connection ports. Each port can be configured as a basic rate ISDN TE or NT or as a synchronous serial port supporting data rates of 56 kbits/s, 64 kbits/s, and 128 kbits/s.

  BRI configuration:
  - — Supports ITU-T (formerly CCITT) I.430, ETSI 300-012, and ANSI T1.605 standards for four-wire ISDN 2B+D basic access at the S/T reference point.
  - — Multiframing support: S & Q channel operation.
  - — Autoactivation and deactivation.
  - — Automatic synchronization of ISDN interfaces.
  - — TE/NT network port configurations support point-to-point and point-to-multipoint arrangement.
  - — TE/NT both use 2768B dual 2:1 turns ratio transformer or 2798B dual, surface-mount transformer for North American deployment, or 2776E 2:1 turns ratio transformer providing electrical isolation as required by European standards EN60950 and EN41003.

  Synchronous serial configuration:
  - — Supports data rates of 56 kbits/s, 64 kbits/s, and 128 kbits/s.
  - — Supports master and slave timing modes.
  - — Provides a simple connection to switched services (e.g., switched 56) CSUs/DSUs.
- Direct connection to *PC/AT* * (16-bit) expansion slot.
  - — Supports programmed I/O bus slave mode.
  - — Supports *Microsoft*† Version 1.0a Plug and Play Specification, providing jumperless software allocation of I/O and interrupt resources.
- On-chip, eight-channel (full-duplex) HDLC formatter.
  - — HDLC framing for all ISDN D channels.
  - — Optional HDLC for CHI, synchronous and B channels or subchannels.
- Memory-based interrupt queue and command queue.
- Linked list buffer management scheme.
- Flexible loopback and test modes.
- Flexible configuration and routing of channels.
- On-chip, 16-channel address generator and buffer manager to local (private) DRAM (1 Mbyte maximum).
  - — Deeply buffered FIFOs (128 bytes per channel).
  - — SRAM can replace DRAM using minimal interface logic.
- Full support of concentration highway interface (CHI).
  - — Direct connection to video interface chip for videoconferencing application.
  - — Supports both master and slave modes.
  - — Automatic synchronization of CHI frame strobe with network (CHI master mode).
  - — *MVIP*‡ compatible.
- Can be programmed to resolve up to 15 ms delays in multiple independent B channels or synchronous 56/64 kbits/s channels.
- Eight programmable I/O (PIO) pins.
  - — Two PIOs can be configured as chip select outputs that become active when associated sections of the T7903's I/O space are accessed.
- Powerdown capability.
- JTAG boundary scan on all digital pins.
- Other:
  - — CMOS technology.
  - — Single +5 V (±5%) supply.
  - — 0 °C to 70 °C.
  - — 132-pin JEDEC BQFP package.

Description

The Lucent Technologies Microelectronics Group T7903 ISA Multiport Wide Area Connection (ISA-MWAC) device has three network ports (NP0, NP1, and NP2) capable of supporting various types of wide area connections. Each port can operate as an ISDN terminal endpoint (TE), network termination (NT), or synchronous serial 56 kbits/s, 64 kbits/s, or 128 kbits/s interface. The T7903 allows flexible routing between the three network ports, a serial concentration highway interface (CHI), and the *PC/AT* industry-standard architecture (ISA) system bus.

* *PC/AT* is a registered trademark of International Business Machines Corporation.
† *Microsoft* is a registered trademark of Microsoft Corporation.
‡ *MVIP* is a registered trademark of Natural Microsystems Corporation.

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Description (continued)

The device allows flexible configuration of its ISDN/serial channels. For example, when using BRI-configured network ports, multiple ISDN B channels can be used to allow higher bandwidth operation. B channels can be subdivided into subchannels to allow multiple virtual connections over one physical B channel. HDLC formatting to and from memory is provided on all D channels and can be used on up to five other bidirectional channels or subchannels. The network ports can be bypassed or used in conjunction with the CHI. The CHI is a user-programmable TDM highway. External devices with compatible serial interfaces (audio/video codecs, DSPs, PRI chips, etc.) can be connected to the CHI allowing the chip to operate as a multiple channel ISA I/O interface controller.

When the network ports are configured in synchronous serial mode and external transceivers are used, the ISA-MWAC can support switched 56 kbits/s, 64 kbits/s, or 128 kbits/s service. See application examples (Figures A-1 and A-2). The ISA-MWAC uses a single +5 V power supply and is available in a 132-pin JEDEC quad flat pack (BQFP) package.

Pin Information

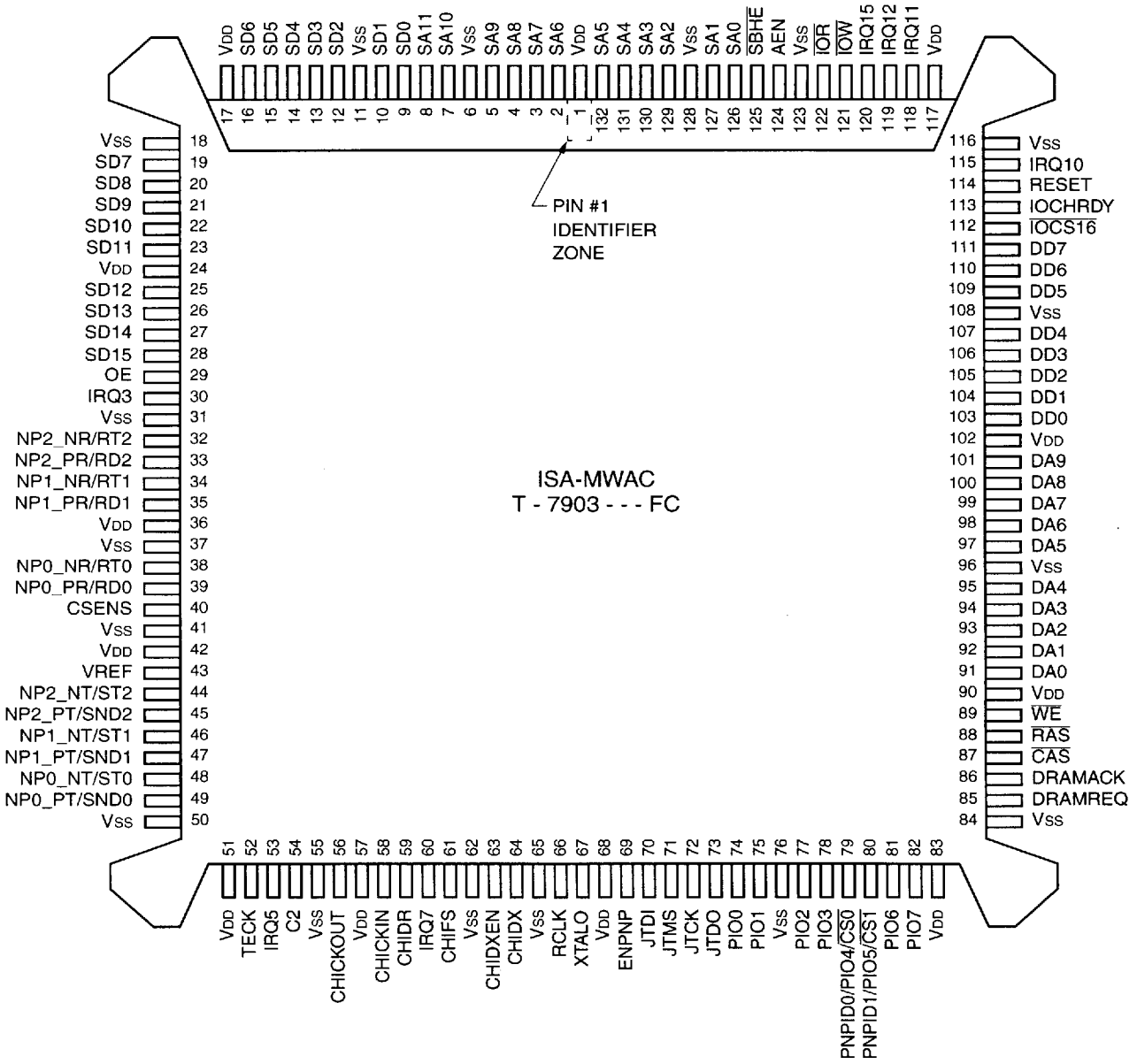

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Figure 1. Pin Diagram

Pin Information (continued)

Tables 1—7 list the location, name, and function of each pin on the ISA-MWAC.

Note: Beginning with version FC4, the T7903 is no longer pin-compatible with earlier versions of the T7903 device. The pin differences are shown below:

Pin Number	T7903-FC1—3	T7903-FC4 and Later
30	$\overline{TO}$	IRQ3
53	CHICKEN	IRQ5
60	Vss	IRQ7
69	ENPUR	ENPNP

See Tables 4 and 6 for more information on the new pins. Note that the sanity timer function is no longer supported.

Table 1. Network Port Pin Descriptions

Pin	Symbol	Type*	Name/Function
49	NP0_PT/ SND0	O	**Positive Transmit Output for Network Port 0.** If NPMODE = 0 (BRI mode) in the NP0 command (see Commands section), this pin is the positive transmit output for network port 0. **Send Data for Network Port 0.** If NPMODE = 1 (synchronous serial mode) in the NP0 command, this pin is the send data output for network port 0. Data bits are transmitted on the rising edge of ST0.
48	NP0_NT/ ST0	B	**Negative Transmit Output for Network Port 0.** If NPMODE = 0 (BRI mode) in the NP0 command (see Commands section), this pin is the negative transmit output for network port 0. **Send Timing for Network Port 0.** If NPMODE = 1 (synchronous serial mode) in the NP0 command, this pin is the send timing pin for network port 0. Data bits are transmitted on SND0 on the rising edge of this clock. Bits CKM1 and CKM0 of the NP0 command select the clock mode for this pin. Available clock modes are slave-standard, slave-terminal, and master timing. See NP0 command description for more information.
39	NP0_PR/ RD0	I	**Positive Receive Input for Network Port 0.** If NPMODE = 0 (BRI mode) in the NP0 command (see Commands section), this pin is the positive receive input for network port 0. **Receive Data for Network Port 0.** If NPMODE = 1 (synchronous serial mode) in the NP0 command, this pin is the receive data input for network port 0.
38	NP0_NR/ RT0	I	**Negative Receive Input for Network Port 0.** If NPMODE = 0 (BRI mode) in the NP0 command (see Commands section), this pin is the negative receive input for network port 0. **Receive Timing for Network Port 0.** If NPMODE = 1 (synchronous serial mode) in the NP0 command, this pin is the receive timing input for network port 0. Data bits on RD0 are sampled on the falling edge of this clock.
47	NP1_PT/ SND1	O	**Positive Transmit Output for Network Port 1.** If NPMODE = 0 (BRI mode) in the NP1 command (see Commands section), this pin is the positive transmit output for network port 1. **Send Data for Network Port 1.** If NPMODE = 1 (synchronous serial mode) in the NP1 command, this pin is the send data output for network port 1. Data bits are transmitted on the rising edge of ST1.

* I = input, O = output, B = bidirectional.

Pin Information (continued)

Table 1. Network Port Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
46	NP1_NT/ ST1	B	**Negative Transmit Output for Network Port 1.** If NPMODE = 0 (BRI mode) in the NP1 command (see Commands section), this pin is the negative transmit output for network port 1. **Send Timing for Network Port 1.** If NPMODE = 1 (synchronous serial mode) in the NP1 command, this pin is the send timing pin for network port 1. Data bits are transmitted on SND1 on the rising edge of this clock. Bits CKM1 and CKM0 of the NP1 command select the clock mode for this pin. Available clock modes are slave-standard, slave-terminal, and master timing. See NP1 command description for more information.
35	NP1_PR/ RD1	I	**Positive Receive Input for Network Port 1.** If NPMODE = 0 (BRI mode) in the NP1 command (see Commands section), this pin is the positive receive input for network port 1. **Receive Data for Network Port 1.** If NPMODE = 1 (synchronous serial mode) in the NP1 command, this pin is the receive data input for network port 1.
34	NP1_NR/ RT1	I	**Negative Receive Input for Network Port 1.** If NPMODE = 0 (BRI mode) in the NP1 command (see Commands section), this pin is the negative receive input for network port 1. **Receive Timing for Network Port 1.** If NPMODE = 1 (synchronous serial mode) in the NP1 command, this pin is the receive timing input for network port 1. Data bits on RD1 are sampled on the falling edge of this clock.
45	NP2_PT/ SND2	O	**Positive Transmit Output for Network Port 2.** If NPMODE = 0 (BRI mode) in the NP2 command (see Commands section), this pin is the positive transmit output for network port 2. **Send Data for Network Port 2.** If NPMODE = 1 (synchronous serial mode) in the NP2 command, this pin is the send data output for network port 2. Data bits are transmitted on the rising edge of ST2.
44	NP2_NT/ ST2	B	**Negative Transmit Output for Network Port 2.** If NPMODE = 0 (BRI mode) in the NP2 command (see Commands section), this pin is the negative transmit output for network port 2. **Send Timing for Network Port 2.** If NPMODE = 1 (synchronous serial mode) in the NP2 command, this pin is the send timing pin for network port 2. Data bits are transmitted on SND2 on the rising edge of this clock. Bits CKM1 and CKM0 of the NP2 command select the clock mode for this pin. Available clock modes are slave-standard, slave-terminal, and master timing. See NP2 command description for more information.
33	NP2_PR/ RD2	I	**Positive Receive Input for Network Port 2.** If NPMODE = 0 (BRI mode) in the NP2 command (see Commands section), this pin is the positive receive input for network port 2. **Receive Data for Network Port 2.** If NPMODE = 1 (synchronous serial mode) in the NP2 command, this pin is the receive data input for network port 2.

* I = input, O = output, B = bidirectional.

Pin Information (continued)

Table 2. Concentration Highway Interface (CHI) Pin Descriptions

Pin	Symbol	Type*	Name/Function
32	NP2_NR/ RT2	I	**Negative Receive Input for Network Port 2.** If NPMODE = 0 (BRI mode) in the NP2 command (see Commands section), this pin is the negative receive input for network port 2. **Receive Timing for Network Port 2.** If NPMODE = 1 (synchronous serial mode) in the NP2 command, this pin is the receive timing input for network port 2. Data bits on RD2 are sampled on the falling edge of this clock.
56	CHICKOUT	O	**CHI Clock Output.** When the CHICM (CHI clock mode) field of the CGM command is 3 or greater (CHI master mode), this pin is the CHI clock output. **CHICKOUT must be connected to CHICKIN when using CHI master mode.** The edges used to transmit and receive data are determined by the XCE and RCE bits in the CDM command. When the CHICM field is 0 or 1 (CHI slave mode), this output is 3-stated. See CDM and CGM command descriptions for more information.
58	CHICKIN	I	**CHI Clock Input.** When the CHICM (CHI clock mode) field of the CGM command is 0 or 1 (CHI slave mode), this pin is the CHI clock input. The edges used to transmit and receive data are determined by the XCE and RCE bits in the CDM command. **When CHI master mode is used, CHICKIN must be connected to CHICKOUT.**
59	CHIDR	I	**CHI Receive Data.** If RHI = 0 in the CDM command, this pin is the CHI data input. If RHI = 1, this pin is not used.
64	CHIDX	B†	**CHI Transmit Data.** This pin is the CHI data output. If RHI = 1 in the CDM command, this pin is also the CHI data input, allowing for CHI local loopbacks.
61	CHIFS	B	**CHI Frame Strobe.** When the CHI is in slave mode, this pin is the CHI frame strobe input. When the CHI is in master mode, this pin is the CHI frame strobe output. See the CHI command for more information.
63	CHIDXEN	O	**CHI Transmit Data Enable (Active-High).** This signal is an envelope of the active time slots on the CHIDX output. It can be used as a 3-state control when buffering CHIDX.
54	C2	O	**CHICKOUT Divided by 2—*MVIP* Clock.** When the CHI is in master mode, this clock is a divide-by-two version of CHICKOUT. Every falling edge of C2 is coincident with every other falling edge of CHICKOUT. In Multi-Vendor Integration Protocol (*MVIP*) compatible systems, this signal is used as the *MVIP* signal C2 and CHICKOUT is used as the *MVIP* signal $\overline{C4}$. Note that in *MVIP* systems, CHICKOUT must be programmed in two clocks per bit mode (see CDM command description). When the CHI is in slave mode, C2 is 3-stated.

* I = input. O = output, B = bidirectional.
† CHIDX is also programmable as an open drain output (see OD bit of CGM command).

Pin Information (continued)

Table 3. JTAG Pin Descriptions

Pin	Symbol	Type*	Name/Function
72	JTCK	I	**JTAG TAP Clock.** It is recommended that this pin be externally pulled to VDD.
71	JTMS	I	**JTAG TAP Mode Select.** This pin is internally pulled to VDD through approximately 20 kΩ.
70	JTDI	I	**JTAG Serial Data Input.** This pin is internally pulled to VDD through approximately 20 kΩ.
73	JTDO	O	**JTAG Serial Data Output.**

* I = input, O = output.

Table 4. Miscellaneous Pin Descriptions

Pin	Symbol	Type*	Name/Function
40	CSENS	A	**Current Sense.** Connect an 11.5 kΩ, 1% tolerance 1/8 W resistor from this pin to VSS.
43	VREF	A	**Voltage Sense.** Connect a 22.1 kΩ, 1% tolerance 1/8 W resistor from this pin to VDD.
66	RCLK	I	**Reference Clock Input; 24.592 MHz.** This input can be driven by either an external oscillator or a crystal. If an oscillator is used, it must have a total frequency tolerance of 100 ppm or less. If a crystal is used, connect it between RCLK and XTALO and connect 33 pF, 5% capacitors from RCLK and XTALO to VSS. See the Crystal Oscillator section for more information.
67	XTALO	O	**Crystal Output Feedback.** If a crystal is used, connect it between RCLK and XTALO and connect 33 pF, 5% capacitors from RCLK and XTALO to VSS. See the Crystal Oscillator section for more information. If an oscillator is used to drive RCLK, this pin must be left unconnected.
52	TECK	B	**Network Sync.** If ENTECK = 1 in the CGM command, TECK is a 4 kHz output. It will synchronize to the first activated network port that is configured as a TE or slave serial port. If no network ports of this type are active, TECK will free-run. If ENTECK = 0, TECK is an input to which CHI and the network ports can be synchronized. See the Device Synchronization section and CGM command description for more information.
29	OE	I	**Output Enable (Active-High).** When OE is high, the chip outputs are enabled. When low, the chip outputs are 3-stated, except for XTALO and JTDO.
69	ENPNP	I	**Enable Plug and Play (Active-High).** If ENPNP is strapped to VDD, ISA Plug and Play support is enabled (see the Plug and Play Support section of this data sheet). If this pin is strapped to VSS, Plug and Play support is disabled (see Appendix G).
74—75 77—78 81—82	PIO[0:1] PIO[2:3] PIO[6:7]	B	**General-Purpose Programmable I/O.** These pins are general-purpose programmable I/O pins. They can be read and independently written. The host can also be interrupted when the PIO's input state changes. See the Programmable I/O Pins section for more information.

* A = analog, I = input, O = output, B = bidirectional.

Pin Information (continued)

Table 4. Miscellaneous Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
79	PNPID0/ PIO4/$\overline{CS0}$	B	**PNPID0.** This pin should be tied to either VDD or VSS through a 10 kΩ resistor. During Plug and Play initialization, the logic state of PNPID0 and PNPID1 is sampled by the T7903 and reported to the host as part of the Plug and Play serial identifier. This allows multiple cards of the same type to be differentiated by the Plug and Play software. **PIO4.** If either PNPID0 or PNPID1 is tied to VSS during Plug and Play initialization, these pins will be configured for PIO functionality. See the PIO[0:3] and PIO[6:7] description above. **$\overline{CS0}$ (Active-Low).** If, during Plug and Play initialization, both PNPID0 and PNPID1 are tied high, the PIO function of these pins is disabled. Instead, they become active-low chip select outputs that assert when the host accesses I/O locations within specified blocks. See the Programmable I/O Pins section for more information.
80	PNPID1/ PIO5/$\overline{CS1}$	B	**PNPID1.** This pin should be tied to either VDD or VSS through a 10 kΩ resistor. During Plug and Play initialization, the logic state of PNPID0 and PNPID1 is sampled by the T7903 and reported to the host as part of the Plug and Play serial identifier. This allows multiple cards of the same type to be differentiated by the Plug and Play software. **PIO5.** If either PNPID0 or PNPID1 is tied to VSS during Plug and Play initialization, these pins will be configured for PIO functionality. See the PIO[0:3] and PIO[6:7] description above. **$\overline{CS1}$ (Active-Low).** If, during Plug and Play initialization, both PNPID0 and PNPID1 are tied to VDD, the PIO function of these pins is disabled. Instead, they become active-low chip select outputs that assert when the host accesses I/O locations within specified blocks. See the Programmable I/O Pins section for more information.

* A = analog, I = input, O = output, B = bidirectional.

Table 5. DRAM Interface

Pin	Symbol	Type*	Name/Function
103—107 109—111	DD[0:4] DD[5:7]	B B	**DRAM Data.** This bidirectional data bus connects to the local DRAM data pins.
91—95 97—101	DA[0:4] DA[5:9]	O O	**DRAM Address.** These outputs connect to the local DRAM address pins.
87	$\overline{CAS}$	O	**Column Address Strobe (Active-Low).**
88	$\overline{RAS}$	O	**Row Address Strobe (Active-Low).**
89	$\overline{WE}$	O	**Write Enable (Active-Low).**
85	DRAMREQ	I	**Request for Access to DRAM (Active-High).** Normally, the host accesses the data structures that are stored in the T7903's local DRAM via I/O-mapped registers (I/O slave access). If local DRAM is shared with the host processor, the host must drive DRAMREQ high to request DRAM access. DRAMREQ must remain high for the entire host access. **This pin must be tied low for conventional I/O slave operation.**
86	DRAMACK	O	**Permission to Access to DRAM.** This signal is used when the T7903's local DRAM is shared with the host. A high on this output indicates that the DRAM is available for access by the host.

* I = input, O = output, B = bidirectional.

Pin Information (continued)

Table 6. ISA Bus Interface Pin Descriptions

Pin	Symbol	Type*	Name/Function
114	RESET	I	**Reset (Active-High).** This signal resets the entire T7903. RESET must be asserted for at least 120 ns. RCLK must be active during RESET assertion. This pin can be connected to the ISA signal RESET_DRV.
115	IRQ10	O	**Interrupt Request 10 (Active-High).** Connect this pin to ISA bus signal IRQ10. The T7903 connects to seven ISA bus interrupt signals: IRQ3, IRQ5, IRQ7, IRQ10, IRQ11, IRQ12, and IRQ15. During Plug and Play initialization of the T7903, only one interrupt pin will be enabled. The other six will be 3-stated.
118	IRQ11	O	**Interrupt Request 11 (Active-High).** Connect this pin to ISA bus signal IRQ11.
119	IRQ12	O	**Interrupt Request 12 (Active-High).** Connect this pin to ISA bus signal IRQ12.
120	IRQ15	O	**Interrupt Request 15 (Active-High).** Connect this pin to ISA bus signal IRQ15.
30	IRQ3	O	**Interrupt Request 3 (Active-High).** Connect this pin to ISA bus signal IRQ3.
53	IRQ5	O	**Interrupt Request 5 (Active-High).** Connect this pin to ISA bus signal IRQ5.
60	IRQ7	O	**Interrupt Request 7 (Active-High).** Connect this pin to ISA bus signal IRQ7.
125	$\overline{\text{SBHE}}$	I	**System Byte High Enable (Active-Low).** $\overline{\text{SBHE}}$ and SA0 are used by the T7903 to determine the type of access that the host is requesting (16-bit access, 8-bit to access an even address or 8-bit to access an odd address).
126—127 129—132 2—5 7—8	SA[0:1] SA[2:5] SA[6:9] SA[10:11]	I I I I	**System Address Bus.** Connect these input pins to the ISA address bus.

* I = input, O = output, B = bidirectional.

Pin Information (continued)

Table 6. ISA Bus Interface Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
9—10 12—16 19—23 25—28	SD[0:1] SD[2:6] SD[7:11] SD[12:15]	B B B B	**System Data Bus.** Connect these bidirectional pins to the ISA data bus.
112	$\overline{\text{IOCS16}}$	OD	**I/O Chip Select 16 (Active-Low).** This open drain output informs the host that 16-bit accesses are supported by the T7903. An access to any address within the T7903's I/O-mapped address space (the I/O block allocated to the T7903 during Plug and Play initialization) will cause $\overline{\text{IOCS16}}$ to assert. Note that $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ are not included in the decoding of $\overline{\text{IOCS16}}$ by the T7903. Thus, $\overline{\text{IOCS16}}$ will assert for memory and I/O accesses that fall within the initialized I/O space.
113	IOCHRDY	OD	**I/O Channel Ready (Active-High).** This open drain output is driven low by the T7903 to extend the current bus cycle. When requiring an extended bus cycle, the T7903 will request a minimum of one extra wait state. The maximum extension is 5.53 µs.
122	$\overline{\text{IOR}}$	I	**I/O Read (Active-Low).** This input indicates to the T7903 that the current access is an I/O read.
121	$\overline{\text{IOW}}$	I	**I/O Write (Active-Low).** This input indicates to the T7903 that the current access is an I/O write.
124	AEN	I	**Address Enable.** This input to the T7903 indicates that a DMA access is in progress. The T7903 3-states SD[0:15] when AEN is high.

* I = input, O = output, OD = open-drain output, B = bidirectional.

Table 7. Power and Ground Pin Descriptions

Pin	Symbol	Type*	Name/Function
6, 11, 18, 31, 37, 41, 50, 55, 62, 65, 76, 84, 96, 108, 116, 123, 128	V_{SS}	G	**Ground.** The 17 V_{SS} pins are tied together internally.
1, 17, 24, 36, 42, 51, 57, 68, 83, 90, 102, 117	V_{DD}	P	**Power.** 5 V ± 5%. The 12 V_{DD} pins are tied together internally.

* G = ground, P = power.

Application Overview

The T7903 ISA-MWAC is intended for use in desktop equipment such as personal computers (PCs), PC plug-in cards, workstations, or anywhere that single or multiple network connections are used. Applications include desktop video, ISDN modems, and PC/workstation network cards for either ISDN or switched service connections. The T7903 is also well suited for stand-alone applications including room videoconferencing systems, WAN-to-LAN bridging, and leased line backup units. In desktop applications, configuring one of the network ports as an ISDN network termination (NT) allows the PC or workstation to terminate a desktop ISDN bus in either point-to-point or point-to-multipoint configuration.

In the simplest application, the ISA-MWAC provides multiple network connections for voice, data, or video communication over ISDN or switched service networks. One (or more) of the network ports can be configured as an ISDN NT. In this configuration, the PC or workstation can be used to enhance the usefulness and usability of the desktop telephone or facsimile machine. By connecting customer premises equipment (CPE) to the NT port (forming a desktop ISDN bus), the workstation can provide menu-based dialing, answering machine functionality, etc. This configuration is shown in Figure 2.

In videoconferencing applications, the ISA-MWAC can act as a data conduit, piping audio and video data between the CHI and the network ports via user-defined time slots. One example would be accepting 112 kbits/s of video on one time slot of the CHI and 16 kbits/s of compressed audio on another time slot of the CHI and sending 128 kbits/s of merged audio and video over two ISDN B channels. The 112 kbits/s video and 16 kbits/s audio rates are just one example. Any other bit rate combination of video, voice, or data can be concatenated and transmitted over from one to six ISDN B channels or from one to three synchronous serial channels for switched service connections.

Another application for the T7903 is as a 16-channel HDLC controller for formatting data passed between the DRAM and the CHI. Note that all network ports could be disabled in this application.

The ISA-MWAC can also support 15 ms of delay equalization over multiple B channels (up to six) or 56/64 kbits/s synchronous channels (up to three). See delay equalization section.

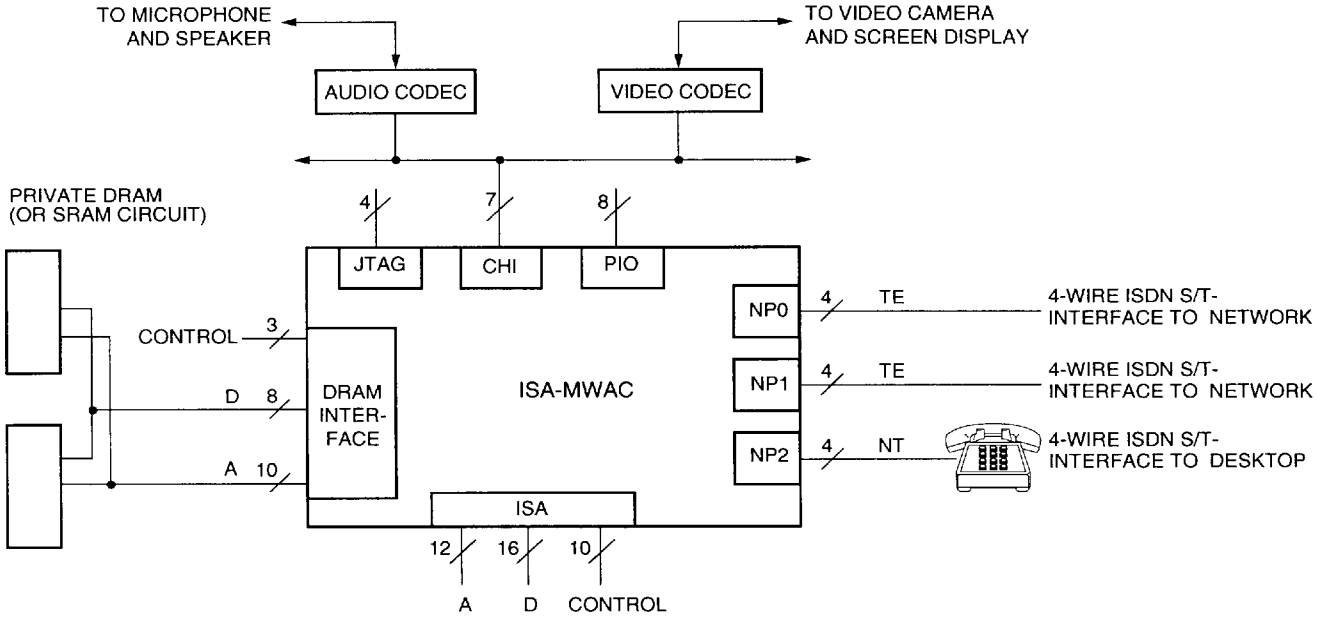


Figure 2. T7903 Application with Two TE Ports and One NT Port Used as a Desktop Bus

Functional Overview

At the highest level, the ISA-MWAC is an integrated circuit with five interfaces to the external world: three network interfaces, an ISA bus interface to the PC or microprocessor host, and a concentration highway interface (CHI) that connects to external devices. The ISA-MWAC serves as a highly flexible conduit for communication between these points.

The T7903's ISA interface is a 16-bit parallel host bus that connects gluelessly to the standard ISA PC bus. It complies to the *Microsoft* Version 1.0a Plug and Play specification, allowing jumperless allocation of I/O address space and interrupt resources. The device is a bus slave and is mapped into the PC's I/O address space. The T7903 can also be connected to general-purpose 8- or 16-bit microprocessors. Plug and Play can be disabled if desired. In this case, an external address decoder must be used to chip select the device. (See Appendix G for more information.)

The three network ports can be independently configured as basic rate ISDN (BRI), terminal endpoint (TE), BRI network termination (NT), or synchronous serial interfaces. When a network port is configured as a synchronous serial interface, external transceivers (for example V.35 type) can be used to provide connections to switched or dedicated service data lines via DSUs/CSUs. Data rates of 56 kbits/s, 64 kbits/s, and 128 kbits/s can be selected. Synchronous serial network port operation provides three timing options: slave-standard, slave-terminal, and master timing.

The CHI is a serial time-division multiplexed (TDM) bus that is highly configurable. Information can be passed between devices on the CHI and any of the network ports or to local DRAM. Examples of external devices that can be connected to the ISA-MWAC via the CHI are voice codecs, high-fidelity audio codecs, and video codecs.

The ISA-MWAC is controlled through sequences of instructions stored in local DRAM. Local DRAM also holds data that is sent out and received from the serial interfaces (the CHI and the three network ports). Also stored in DRAM are the transmit and receive descriptors and the interrupt queue. The descriptors contain status and linking information for the data buffers. The interrupt queue holds the status information for all T7903 interrupts reported to the host. Note that DRAM can be replaced by SRAM using minimal interface logic, as described in Appendix H.

The T7903 has several internal registers that are programmed by the host. These registers, along with a DRAM address pointer register and a DRAM data port register, are mapped into the host's I/O address space. The DRAM address pointer and data port registers are used by the host to access all data structures stored in local DRAM.

Serial Interface Overview

The ISA-MWAC views the three network ports (NP0, NP1, NP2) and CHI as independent, time-division multiplexed (TDM) serial interfaces. In most configurations, the interfaces transmit and receive data with specific frame and bit timing (note that network ports configured for synchronous serial operation do not have the notion of frame timing). A serial interface frame is generally 125 µs long (although the CHI can be operated at other frame rates). The instances that deviate from these generalizations will be described in detail later.

The serial interfaces transmit and receive information over groups of bits called time slots. Internally to the chip, time slots can be passed between serial interfaces or between a serial interface and DRAM.

Time Slots and Data Pipes

A time slot is a variable length bit string derived from any of the four serial interfaces. A time slot on a network port configured for basic rate ISDN can be from 1 bit to 16 bits long; a time slot on the CHI can be from 1 bit to 255 bits long. Within the ISA-MWAC, time slots are shuttled about using a series of 32 internal data pipes. There are 16 short, or shallow buffered, data pipes that are used for connection between serial ports. There are 16 long, or deeply buffered, data pipes that are usually used to interface between a serial port and a data structure in local DRAM, although they can be used between serial ports. The setup data pipe (SDP) command is used to initialize the data pipes (define interrupts, select data mode, etc.).

Data pipes are usually used in pairs—one in each direction. This means that any bidirectional data transfer between any of the interfaces requires two data pipes. Each data pipe will have two time slots defined for it; one entering the pipe and one leaving it. These time slots are defined using the define time slot (DTS) command. The DTS command defines whether the time slot is at the input or the output of a pipe, its connectivity to other time slots, where in the serial stream the time slot is located, its length, etc.

Multiple time slots from the same interface can connect to the same data pipe, in the same direction. These time slots may or may not be contiguous (for noncontiguous mode, see DTS (0x7): Define Time-Slot Command section).

Data transmitted by a serial interface does not have to come from another interface or a DRAM data buffer. Using fixed data mode (see SDP (0x5): Setup Data Pipe Command and SSP (0x8): Set Short Pipe Data Command sections), constant data patterns can be transmitted on a time slot.

Serial Interface Overview (continued)

Time Slots and Data Pipes (continued)

Similarly, data received by a serial interface does not have to be sent to another interface; it can simply be monitored. Changes in the received patterns can be reported to the host via interrupt. The ISDN S and Q channels are supported on the basic rate interfaces by the use of short data pipes in fixed data mode. SSP commands can be used to set a value for S and Q, which is output repeatedly until changed. If an incoming S or Q channel changes, the change is reported on the interrupt queue, if this interrupt is enabled. Figure 3 highlights the use of short and long data pipes. In this application (an ISDN voice call), two short data pipes are used for connecting an NT-configured network port to a TE port and four long data pipes carry the D channels.

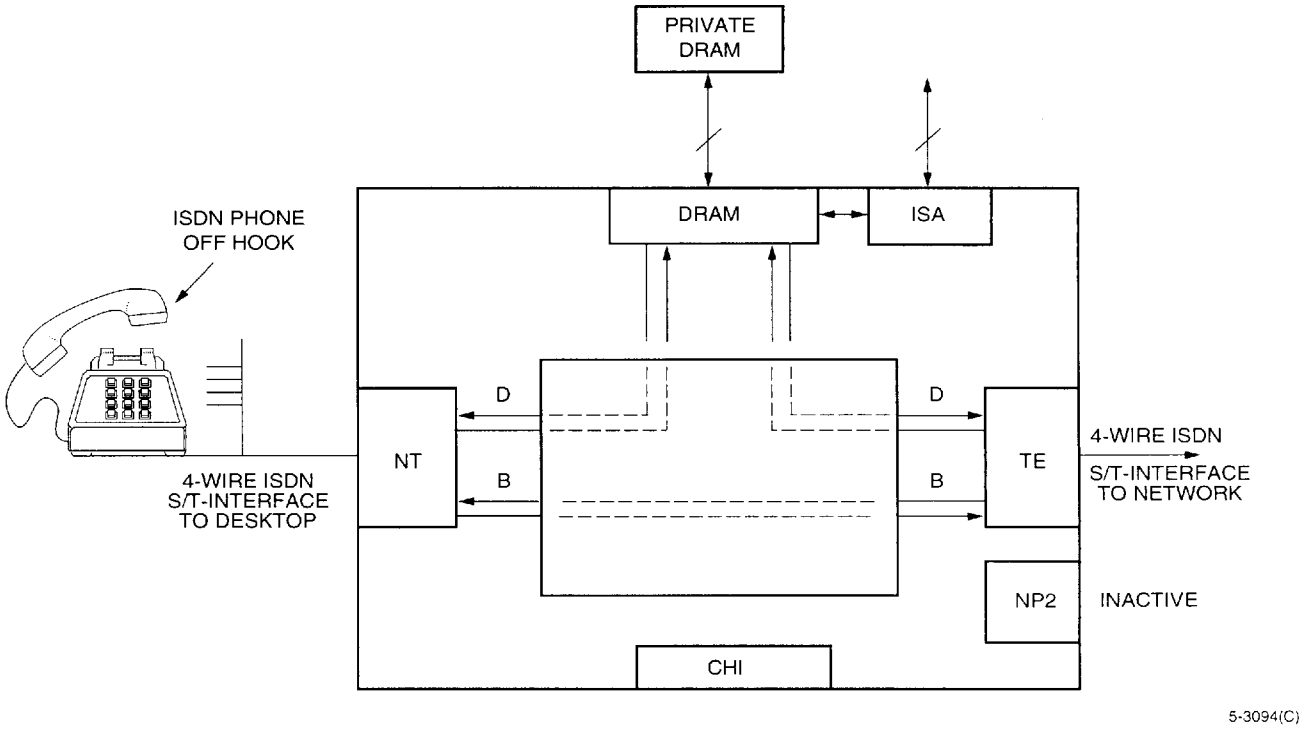


Figure 3. Short and Long Data Pipes

Serial Interface Overview (continued)

Time Slots and Data Pipes (continued)

Time Slots on Network Ports in BRI Mode

A network port in BRI TE or NT mode is viewed as a 19-bit long bit string consisting of the B1 and B2 channels (8 bits each), followed by a Q or S channel bit (Q in the TE transmit/NT receive direction or S in the TE receive/NT transmit direction) and then 2 bits of D channel. This is shown in Figure 4. Time slots are defined for these interfaces by using DTS commands and specifying the time slot length and starting location, referenced to cycle 0 shown in Figure 4. A time slot on a basic rate interface can be from 1 bit to 16 bits long. Thus, B1 and B2 can be concatenated and viewed as a single 16-bit time slot. Multiple DTS commands can be used to define overlapping transmit and receive time slots for the B1 and B2 channels.

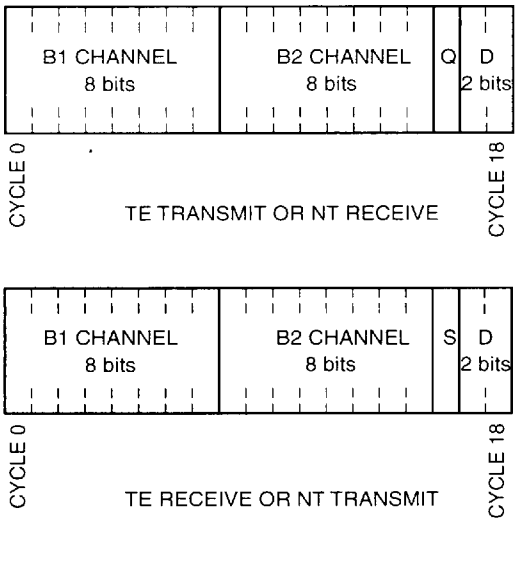


Figure 4. Bit Positions on the TE and NT Ports

Time Slots on Network Ports in Synchronous Serial Mode

A network port in synchronous serial mode is viewed as a 7-bit, 8-bit, or 16-bit long string, depending on the data rate (56 kbits/s, 64 kbits/s, or 128 kbits/s). Time slots are defined for a synchronous port by using the DTS commands and specifying the time slot length and starting location, referenced to cycle 0 shown in Figure 5.

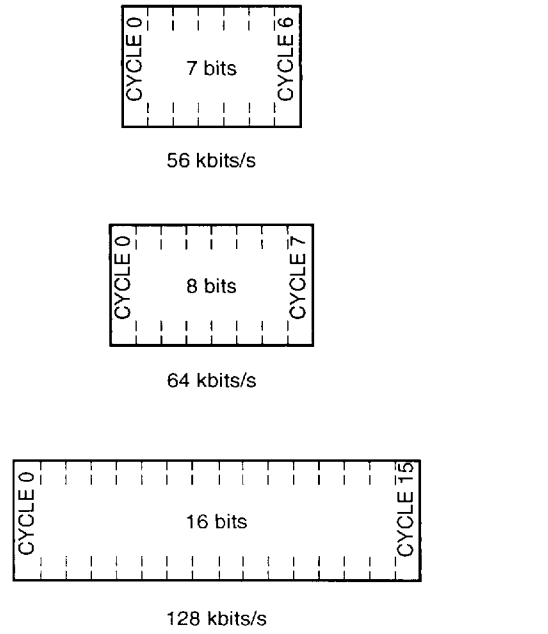


Figure 5. Bit Positions on a Synchronous Port

CHI Time Slots

A time slot on the CHI can be from 1 bit to 255 bits long.

When an 8 kHz CHIFS is used, the CHI is viewed as a 125 µs pulse train on CHICKIN/CHICKOUT. When CHIFS is a non-8 kHz input, the pulse train repetition rate is set by CHIFS (see the CGM (0x9): CHI Global Mode Command section).

Restrictions on Time Slots

The following is a list of restrictions on the use of time slots.

Caution: The ISA-MWAC does not enforce these restrictions, but peculiar actions result from their violation.

- Time slots from different interfaces cannot be connected to the same data pipe in the same direction. But, a single incoming time slot may be assigned to two data pipes.
- For the CHI, the time-slot descriptors must not define overlapping time slots.
- CHI time slots that are greater than 32 bits long must connect to long data pipes.
- No CHI time slot can start within 0.975 µs **after** the **start** of the previous time slot.

The Network Ports

The T7903 has three network ports: NP0, NP1, and NP2. These ports are used to connect the PC, workstation, or other T7903-based system to wide area networks such as ISDN or switched services. Additionally, the ports can be configured to operate like the network side of a wide area interface. In this way, telephones, FAX machines, or even video terminal equipment can connect to the T7903, providing enhanced, host-controlled operation.

The network ports are configured by the NP0, NP1, and NP2 commands. These commands set up the port mode, its timing, interrupts, loopbacks, and other parameters. The three possible network port modes are basic rate ISDN terminal endpoint (BRI TE) mode, BRI network termination (BRI NT) mode, and synchronous serial mode. Each port consists of four pins, the function of which is determined by the port's mode (BRI or synchronous).

Basic Rate TE and NT Modes

The ISA-MWAC network ports can be independently programmed as ISDN NT or TE interfaces. As a TE, the port can connect to the ISDN to provide 2B+D voice/data capability. Higher bandwidth applications can use multiple TE ports. The only requirement for multiple TE connections is that each of the ISDN lines must originate from the same switch to ensure proper synchronization. The NT configuration allows the system to support a local ISDN bus. Multiple NT ports can provide switching functions.

A network port is configured for BRI mode by setting NPMODE = 0 (bit 23) and RLEVEL/TLEVEL = 0 (bit 22 and 20) in the NP0, NP1, or NP2 command. TE or NT mode is selected by the ISNT bit (bit 13) as described in the next two sections. In TE or NT mode, the port pins become differential pairs; one pair for the transmit direction and one pair for the receive direction.

TE Mode

A network port is configured as a BRI TE by setting NPMODE = 0, RLEVEL/TLEVEL = 0, and ISNT = 0 in the NP command for that port. This mode enables systems to meet all international requirements for a TE at the S/T reference point. All timing is extracted from the signal received from the ISDN network. The NP0, NP1, and NP2 commands control the various TE mode functions such as activation, framing parameters, and multiframing. The complete description of these bits is given in the NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands section.

NT Mode

A network port is configured as a BRI NT by setting NPMODE = 0, RLEVEL/TLEVEL = 0, and ISNT = 1 in the NP command for that port. This mode enables systems to meet all international requirements for an NT at the S/T reference point.

Timing for an NT port is extracted as follows. If a TE-configured port is active and synchronized to the network prior to the NT port becoming active, the NT port's frame timing is synchronous with the TE port (and thus to the network). If the TE port is not synchronized prior to the NT port becoming active, then the NT port's frame timing is free-running. If the TE port synchronizes after the NT is already active, then the NT port will frequency-lock to the TE port but no specific phase relationship is maintained.

The NP command controls the various NT mode functions such as activation and framing parameters, echo channel control, timing modes, and multiframing. The complete description of these bits is given in the NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands section.

BRI Interface Circuitry Requirements

Figure 6 shows the required line interface circuitry for a network port configured as a TE and as an NT. Note that the use of ports NP0 and NP1 in Figure 6 is just an example. There are no restrictions on port definition. When used in BRI mode (either as a TE or an NT), the T7903 ISA-MWAC requires 2:1 turns ratio transformers connected between the device receive and transmit pins and the S/T interface. Lucent Technologies makes four 2:1 turns ratio transformers for use with the T7903: the 2768B, 2800B, 2798B, and 2776E. All work with NT or TE mode ports. The 2768B, 2800B, and 2798B are dual transformer designs (only one is required per network port) and incorporate operational isolation between primary and secondary coils. The 2768B is a through-hole component and the 2798B is a surface mount. The 2800B is suitable for PCMCIA Type II applications. The 2776E is a single transformer (two required per port) and uses reinforced isolation between its primary and secondary coils. Current North American requirements allow operational isolation in basic rate ISDN designs. International standards have historically required reinforced isolation. Therefore, the 2768B, 2800B, and 2798B are recommended for systems sold in North America and the 2776E is recommended for systems sold internationally. For more information, see safety standards *UL** 1950, EN60950, and EN14003. It should be noted that changes to international requirements for safety at the basic rate ISDN interfaces are currently under consideration. Proposed changes may eliminate the need for reinforced isolation at the S/T reference point making the 2768B, 2800B, and 2798B transformers acceptable in most European countries. Consult with regional standards organizations for current regulations.

* *UL* is a registered trademark of Underwriters Laboratories, Inc.

The Network Ports (continued)

Basic Rate TE and NT Modes (continued)

BRI Interface Circuitry Requirements (continued)

All of the Lucent Technologies transformers are low-capacitance designs that enable systems to conform to the ITU-T I.430 TE and NT impedance templates. Design of protection and noise suppression circuitry is simplified because of the margins to these templates.

The actual requirements for these circuits are highly environment (country and system) dependent. For example, the design requirements for common-mode noise suppression circuitry depend on system parameters such as signal rise/fall times and clock frequencies, as well as the specific emissions limits used by various testing agencies (FCC class A or B, VDE, etc.). Generally, a common-mode choke is used to limit both emissions out onto the line as well as susceptibility to externally applied common-mode noise. Common-mode noise can also be reduced by connecting capacitors from the transformer center taps to ground.

Surge protection circuitry is dependent upon overvoltage requirements of the testing agency. A diode bridge is usually used to shunt excessive voltage levels to ground. It should be noted that any parasitic capacitance on the device side of the transformer is increased by a factor of 4 (2 squared) when reflected to the line side. Therefore, protection circuitry capacitance may impact margin to I.430 impedance specifications.

Transformer breakdown voltage requirements also vary between regulatory agencies. The Lucent Technologies 2768B, 2798B, and 2800B transformers are designed to withstand 2400 Vrms for 2 s and the 2776E is designed to withstand 3000 Vrms for 2 s.

Detailed information on line interface circuitry can be found in the Application Brief section of this document.

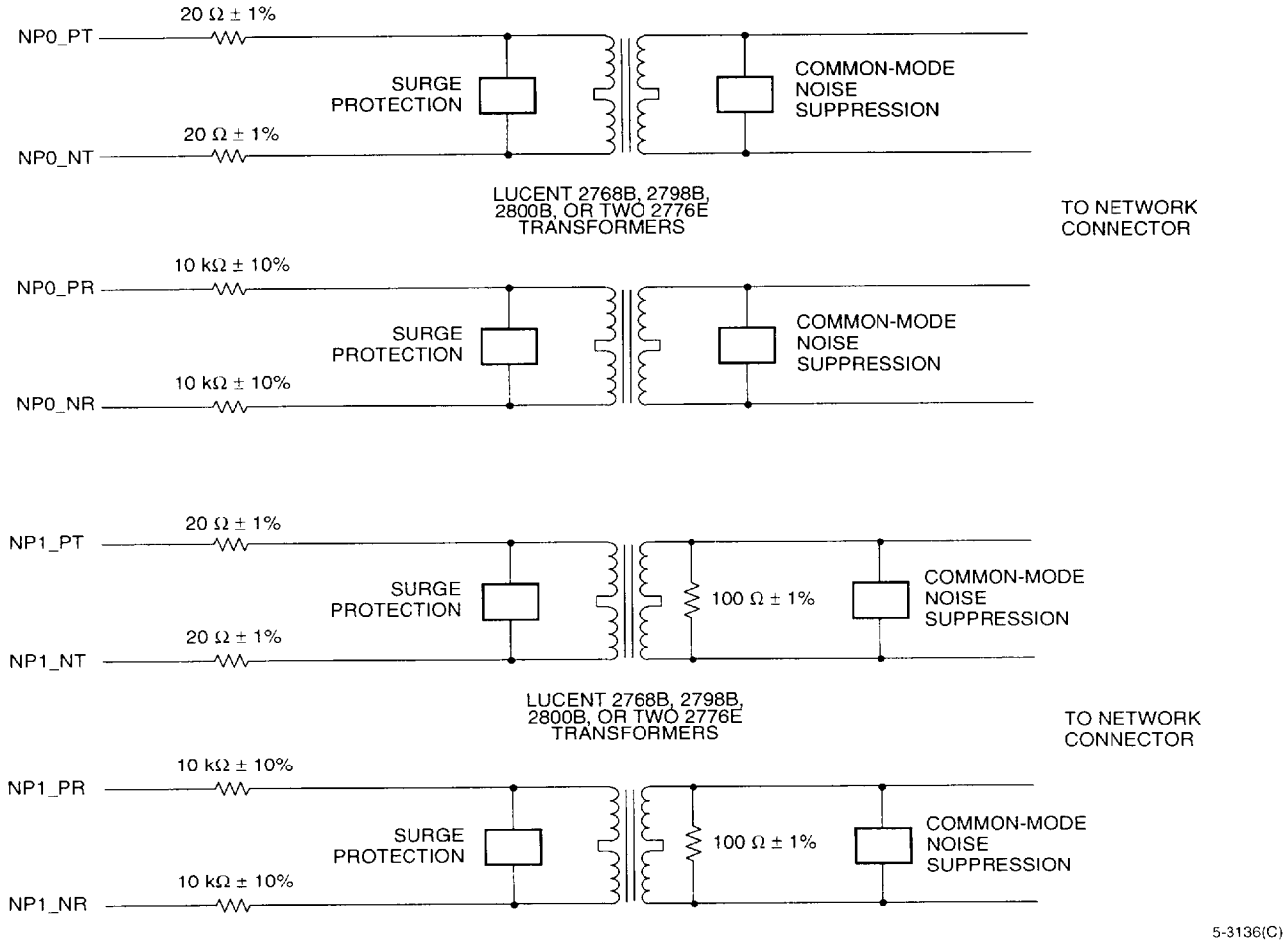


Figure 6. Network Port Interfaces Using NP0 as a TE and NP1 as an NT

The Network Ports (continued)

Synchronous Serial Modes

The ISA-MWAC network ports can be independently programmed as synchronous serial data ports. In the synchronous modes, the analog section of the chip is bypassed and the network port pins become single-ended digital inputs and outputs. These signals are send data (SNDx), send timing (STx), receive data (RDx), and receive timing (RTx). A data bit is clocked out of SNDx on every rising edge of STx. A data bit is clocked into RDx on every falling edge of RTx.

With the use of external line transceivers and data service units/channel service units (DSUs/CSUs) or specialized network interface ICs, the synchronous ports provide a simple connection to switched or dedicated data networks such as switched 56. Three data rate options are available: 56 kbits/s, 64 kbits/s, and 128 kbits/s. Three timing modes are available: slave-standard, slave-terminal, and master timing. When in one of the synchronous slave modes, the port can connect to switched or dedicated data networks to provide data transport capability to the PC or workstation. Higher bandwidth applications can use multiple slave ports. The choice of standard or terminal timing determines where the ISA-MWAC gets its transmit timing signal from (described in detail below). The master timing mode allows the T7903 to be the source of network timing to support connections to external customer premises equipment such as video terminals. One application of master mode would be in a terminal adapter for connecting switched service terminals (for example, a video terminal) to the ISDN via the T7903 (see Appendix A).

The network ports are configured for synchronous mode by setting NPMODE = 1 (bit 23), RLEVEL/TLEVEL = 1 (bit 22 and 20), and ISNT = 0 (bit 13) in the NP0, NP1, and NP2 commands. Note that ISNT is used for BRI modes only and must be set to zero for synchronous operation. The data rate is selected by the SWM0 and SWM1 bits (bits 11 and 12), and the timing modes are selected by the CKM0 and CKM1 bits (bits 16 and 17). See the NP0, NP1, and NP2 commands section for full details.

Slave Mode: Standard and Terminal Timing

Synchronous slave mode is used when a T7903 network port must derive data transport timing from a synchronous network. Slave mode has two timing options: standard and terminal timing. In slave-standard mode, the timing for both send and receive data comes from the network (STx and RTx are inputs to the ISA-MWAC). This mode is enabled by CKM0 = 0 and CKM1 = 0 in the NP0, NP1, and NP2 commands.

In slave-terminal timing mode, the timing for the receive data comes from the network on RTx. Thus, the T7903 is slaved to the network. The T7903 internally steers this clock to the STx pin, which is configured as an output. The network DSU/CSU then uses this signal as the clock for sampling the data out of the T7903 on SNDx. This timing mode is used to compensate for long delays between the slave and the network DSU/CSU and is enabled by CKM0 = 1 and CKM1 = 0.

Master Timing Mode

In master mode, the T7903 is the source for network port timing. STx is an output and is the timing for the data transmitted on SNDx. **The receive timing pin, RTx, is an input and must be connected externally to STx to provide a clock for the data bits received on RDx.** Master mode is enabled by CKM0 = 1 and CKM1 = 1.

Concentration Highway Interface (CHI)

The CHI is a full-duplex, serial time-division multiplexed (TDM) interface for digital data transfer between ICs in communication systems. The CHI can be programmed to interface with a variety of other TDM interfaces supported by various commercial products and can operate as either the timing master or slave. The CHI consists of five main signals: CHICKIN, the slave mode data clock input; CHICKOUT, the master mode data clock output; CHIFS, the bidirectional frame synchronization signal; CHIDX, the data transmit lead; CHIDR, the data receive lead. The clocks, CHICKIN and CHICKOUT, can be run between 64 kHz and 4.096 MHz. The frame synchronization signal, CHIFS, can range from 8 kHz to 50 kHz for CHI slave mode (CHIFS in an input) and is always an 8 kHz output for CHI master mode. Two other CHI signals, CHIDXEN and C2, are described in Table 2.

Two T7903 commands are used to configure the CHI: the CHI global mode (CGM) and CHI data mode (CDM) commands. In the CGM command, bit field CHICM (CHI clock mode) is used to enable either master or slave mode as well as to program clock and CHIFS rates. It functions as follows:

- If CHICM = 0, CHI slave mode is enabled and the CHIFS input must be 8 kHz,
- If CHICM = 1, CHI slave mode is enabled and the CHIFS input can be from 8 kHz to 50 kHz,
- If CHICM ≥ 3, CHI master mode is enabled, CHIFS is an 8 kHz output and the CHICKOUT rate is 12.288 MHz divided by CHICM.

Data can be transmitted on any clock edge following recognition of the frame sync pulse. In slave mode, CHIFS can be sampled on either the rising or a falling edge of CHICKIN as determined by FE in the CGM command (bit 12). In master mode, CHIFS can be driven on either the rising or a falling edge of CHICKOUT as determined by FD in the CGM command (bit 11). The CHI can transmit and receive data on either the rising or falling edge of the clock, as determined by the XCE and RCE bits of the CDM command (bits 2 and 6). See the CGM and CDM command descriptions for more details.

The CHI can be divided into logical time slots from 1 bit to 255 bits in length. Several devices can be connected to the CHI, each with its own transmit and receive time slots assigned. In a videoconferencing example, the ISA-MWAC can be connected via the CHI to a video compression chip and an audio chip. The ISA-MWAC can read 14 bits of video from one time slot and 2 bits of audio from another time slot. The ISA-MWAC can then be programmed to concatenate that data onto two B channels and send them out over the TE interface toward the network. The location and duration of a time slot on the CHI are programmed by using the DTS (0x7): Define Time-Slot Command described in the Commands section of this document.

The CHI also has a double-clock mode. See the CHI Double-Clock Mode and *MVIP* Compatibility section for more detailed information.

Note: Do not define time slots that wrap around the CHI frame boundary.

CHI Slave Mode

In CHI slave mode, CHICKIN is the data clock input, CHICKOUT is 3-stated, and CHIFS is the frame synchronization input. In this mode, CHIFS frequency can range from 8 kHz to 50 kHz. Frequencies other than 8 kHz may be useful when connected to high-fidelity audio codecs.

Important: **When data is being transferred between the CHI and a network port configured as a basic rate ISDN interface, the CHIFS frequency must be 8 kHz.**

When an 8 kHz CHIFS is used (CHICM = 0), the CHI is viewed as a 125 µs pulse train. When CHIFS is a non-8 kHz input (CHICM = 1), the pulse train repetition rate is set by CHIFS (see the CGM: CHI Global Mode Command section of this document).

Figures 7 through 10 show the CHI slave mode timing and how clock edges are counted in cycles. Cycles are defined as always beginning (with cycle 0) on a rising clock edge relative to the clock edge on which CHIFS is sampled. Data transmission can begin on any clock cycle relative to cycle 0 by programming the appropriate CYCLE value in the define time-slot command, described in the DTS (0x7): Define Time-Slot Command section of this document. The actual position (relative to CHIFS being sampled high) of cycle 0 depends on the CHI mode (master or slave) and FE (the clock edge that CHIFS is sampled on).

Figure 7 shows slave mode transmit timing when CHIFS is sampled on the rising edge of CHICKIN (FE = 1 in CGM command). Note that cycle 0 begins on the CHICKIN edge labeled 0.

Figure 8 shows transmit timing with CHIFS sampled on the falling edge of CHICKIN (FE = 0). Figure 9 and Figure 10 show slave mode receive timing for FE = 1 and FE = 0, respectively.

Concentration Highway Interface (CHI) (continued)

CHI Slave Mode (continued)

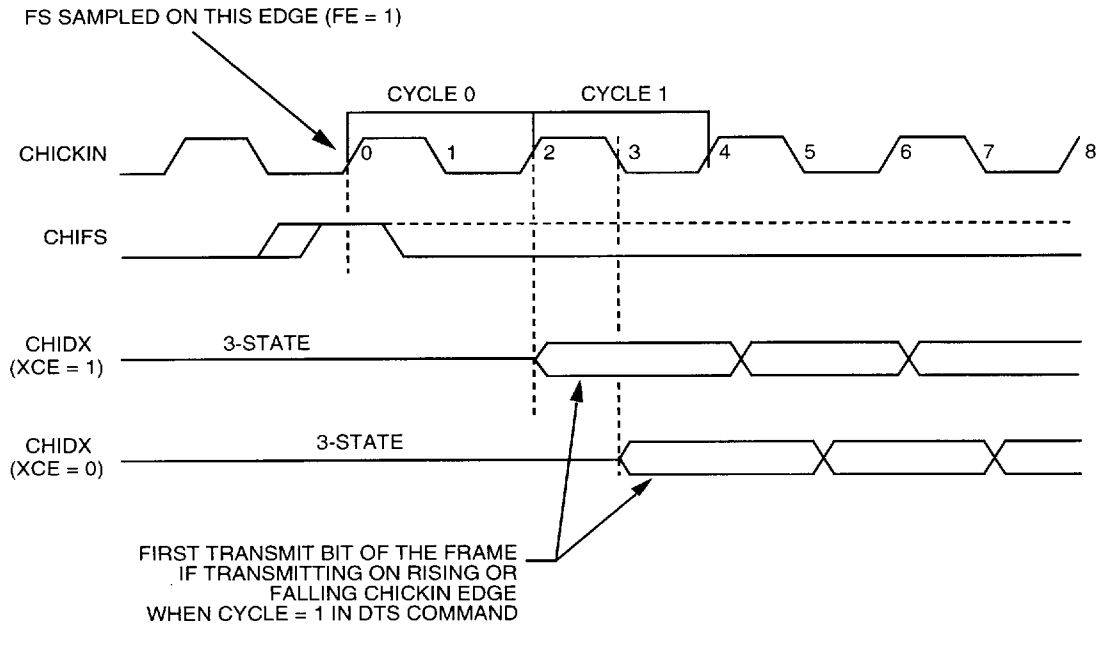


Figure 7. Transmit Timing (FE = 1)—CHI Slave Mode

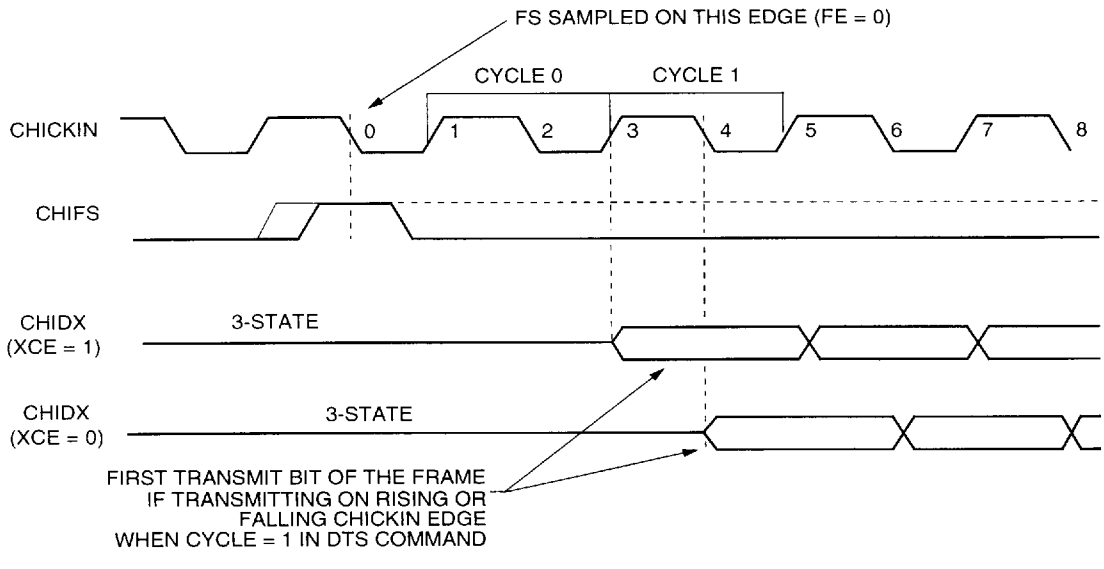


Figure 8. Transmit Timing (FE = 0)—CHI Slave Mode

Concentration Highway Interface (CHI) (continued)

CHI Slave Mode (continued)

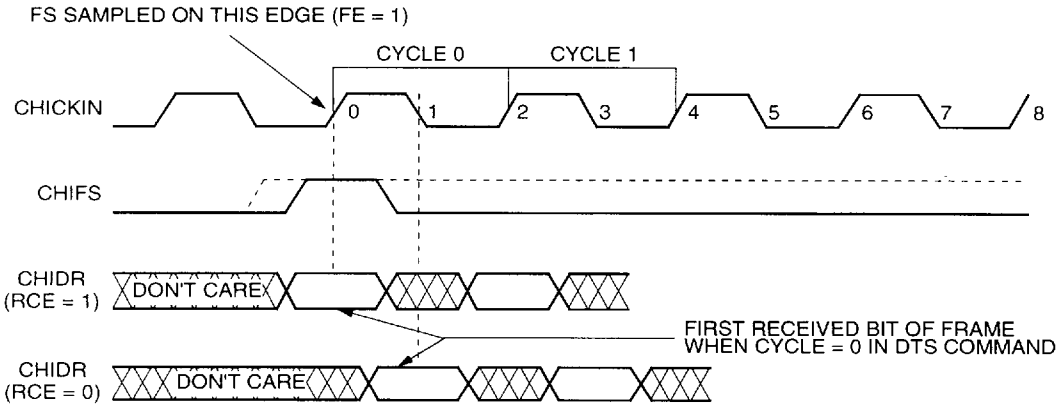


Figure 9. Receive Timing (FE = 1)—CHI Slave Mode

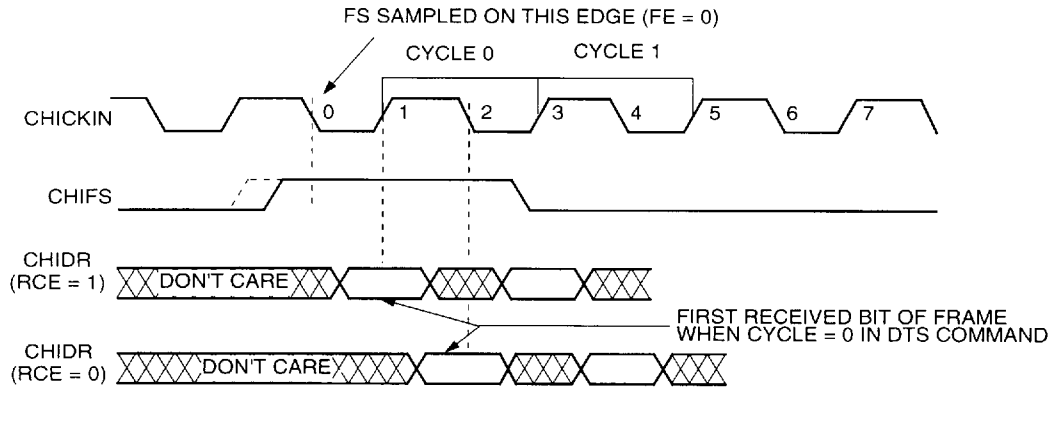


Figure 10. Receive Timing (FE = 0)—CHI Slave Mode

Concentration Highway Interface (CHI)

(continued)

CHI Master Mode

In CHI master mode, CHICKOUT is enabled as the CHI output clock. **CHICKIN must be connected to CHICKOUT when using CHI master mode.** CHIFS is an output that signals the beginning of each CHI frame by going high for one CHICKOUT cycle every 125 µs (CHIFS frequency is always 8 kHz for CHI master mode). The CHI will synchronize to the first synchronous slave or TE-configured network port to become active (active means receiving INFO 4 from the network in the case of a TE, or getting receive timing from the network for a synchronous slave). The CHI can also synchronize to an external 8 kHz signal applied to the TECK pin. See the Device Synchronization section for more details. The BPF field of the CGM command determines the number of CHICKOUT cycles that are output every 125 µs frame. If BPF = 0, CHICKOUT outputs continuous clock pulses through the entire frame. When BPF is greater than 0, CHICKOUT outputs BPF + 1 pulses. The first pulse occurs during the period that CHIFS is active (the cycle immediately preceding cycle 0).

Figures 11 through 14 show CHI master mode timing. As was the case for slave mode, cycles are defined as always beginning on a rising clock edge (cycle 0) relative to the clock edge on which CHIFS is sampled. Data transmission can begin on any clock cycle relative to cycle 0 by programming the appropriate value into the CYCLE field of the DTS command, described in the DTS (0x7): Define Time Slot Command section of this document.

Note that FE (bit 12, CGM command), which determines the clock edge that samples CHIFS, must be considered for master mode as well as slave mode.

Figure 11 shows master mode transmit timing when CHIFS is sampled on the rising edge of CHICKOUT (FE = 1 in CGM command). Figure 12 shows transmit timing with CHIFS sampled on the falling edge of CHICKOUT (FE = 0). Figure 13 and Figure 14 show master mode receive timing for FE = 1 and FE = 0, respectively.

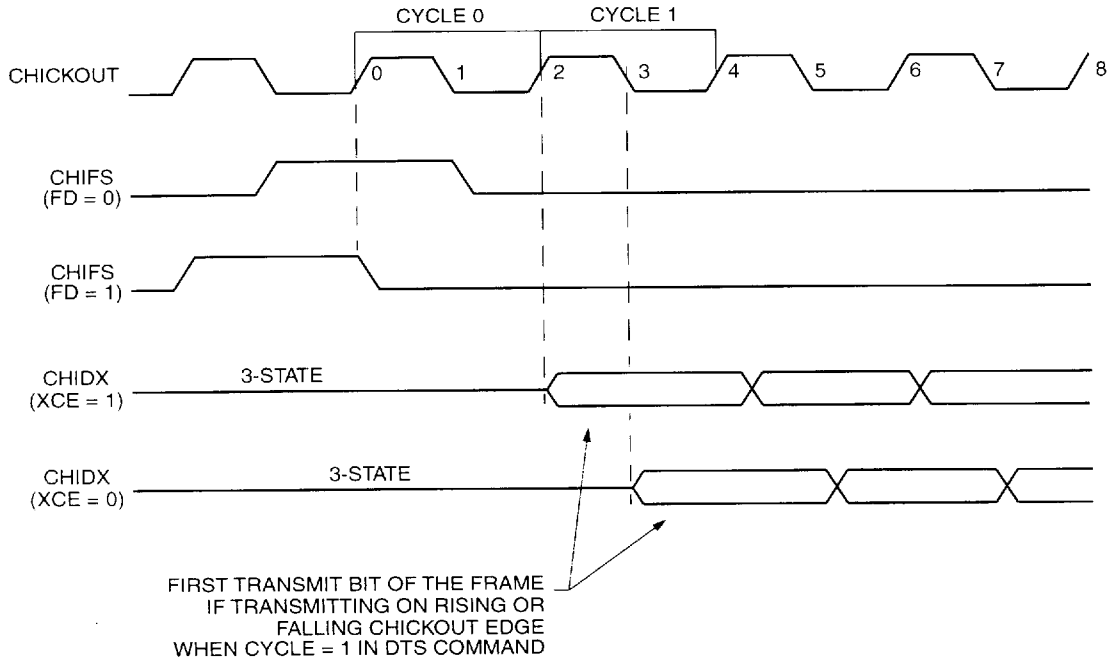
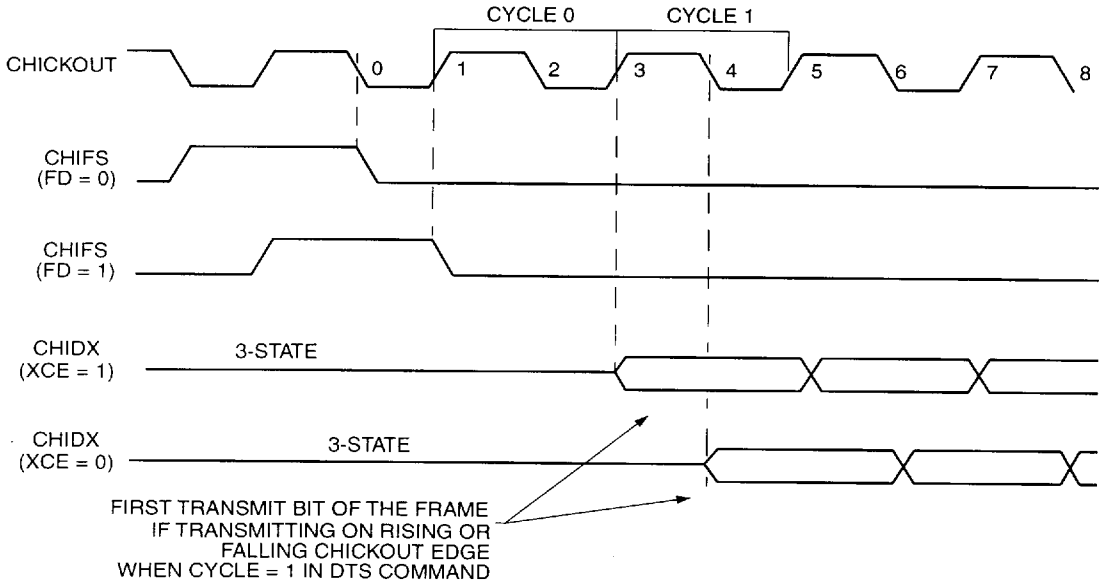


Figure 11. Transmit Timing (FE = 1)—CHI Master Mode

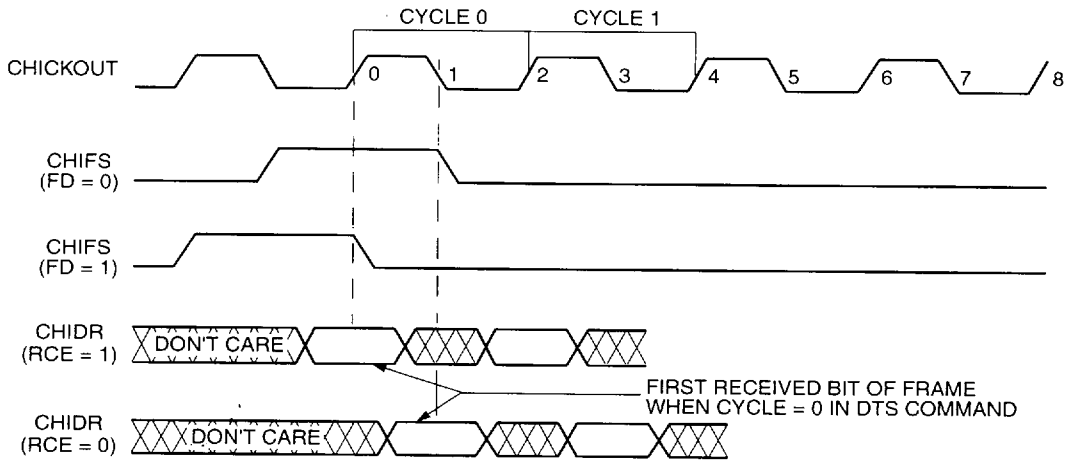
Concentration Highway Interface (CHI) (continued)

CHI Master Mode (continued)



5-3779(F).a

Figure 12. Transmit Timing (FE = 0)—CHI Master Mode



5-3780(F).a

Figure 13. Receive Timing (FE = 1)—CHI Master Mode

Concentration Highway Interface (CHI) (continued)

CHI Master Mode (continued)

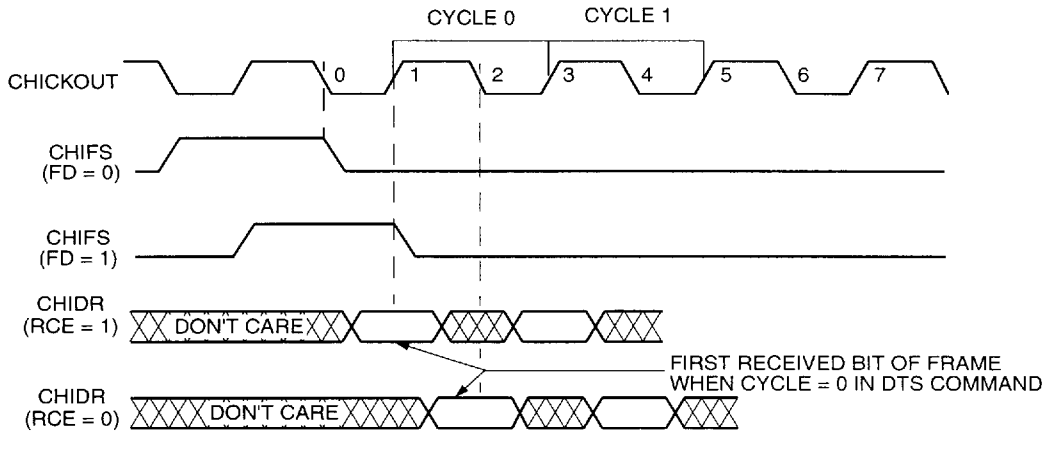


Figure 14. Receive Timing (FE = 0)—CHI Master Mode

ISA Interface Description

The ISA-MWAC connects directly to the *PC/AT* industry-standard architecture (ISA) system bus. It is designed to be a 16-bit I/O slave to the ISA bus but can also operate as an 8-bit slave. Standard and IOCHRDY-controlled ISA I/O access cycles are supported. Zero wait-state access cycles are not supported by the T7903.

To facilitate easy system configuration, the ISA-MWAC supports *Microsoft's* Plug and Play ISA Specification (PNP ver. 1.0a, 5/5/94). This provides jumperless, software allocation of interrupt and I/O space resources. One of seven possible interrupt output pins can be enabled (IRQ3, 5, 7, 10, 11, 12, or 15) and the I/O space base address can be selected in the range of 0x200 to 0x3e0. After device powerup or reset, the T7903 is inactive. Plug and Play software residing on the host initializes all cards on the ISA bus, individually isolates each card to determine necessary resources, and then allocates the resources accordingly. For host platforms that do not support Plug and Play, the host must initialize the T7903 and allocate resources upon powerup and after system reset (if the Plug and Play feature is enabled). See the Plug and Play Support section of this document for more information.

The ISA interface can also connect to general-purpose 16-bit or 8-bit microprocessors. If desired, the Plug and Play feature can be disabled entirely. In this case, the I/O base address defaults to 0x0000 and the interrupt request lead defaults to pin 120 (IRQ15). (See Appendix G for more information.)

ISA I/O Port Overview

The T7903 contains eight 16-bit registers, referred to as I/O ports (IP0—IP7) that provide status and control of the chip. The I/O ports also provide a path for the host to get to local DRAM. The host communicates with the ports via I/O reads and writes, with the ports taking up 16 consecutive addresses (bytes) in the PC's I/O space. The base address of this space, along with other information, is provided by software to the ISA-MWAC through three autoconfiguration ports as defined in the Plug and Play specification. For more details, see the Plug and Play section of this document. Table 8 shows the T7903's 8 I/O ports IP0—IP7. Tables 9 through 16 give a full description of the bits in IP0—IP7.

The T7903 uses A0 and $\overline{\text{SBHE}}$ to determine the type of access that is pending, as described below:

A0	$\overline{\text{SBHE}}$	Access Type
0	0	16-bit
0	1	8-bit access to low-order register byte (even address)
1	0	8-bit access to high-order register byte (odd address)
1	1	not allowed

ISA Interface Description (continued)

ISA I/O Port Overview (continued)

For all register accesses (8- or 16-bit), the T7903 responds with $\overline{IOCS16}$ = 0, indicating that 16-bit accesses are supported by the device. For 16-bit accesses, data is driven on all 16 data lines (SD[15:0]). For 8-bit accesses to the low-order (even addressed) byte of a T7903 register, the device expects data on the low-order data lines (SD[7:0]) for writes, and drives only the low-order lines for reads (SD[15:8] are 3-stated). For 8-bit accesses to the high-order (odd addressed) byte of a T7903 register, the device expects data on the low-order data lines (SD[7:0]) for writes, and drives the identical 8 bits of data on both the low-order and high-order halves of the data bus for reads. Note that the above is valid for non-Plug and Play accesses only. For 8-bit accesses to Plug and Play ports, the T7903 responds with $\overline{IOCS16}$ = 1 and drives only the low-order data bus during reads.

Accessing DRAM Through the I/O Ports

The T7903 must be connected to external DRAM (or an optional SRAM circuit described in Appendix H). The minimum amount of DRAM is dependent upon the application. The maximum amount is 1 Mbyte. This DRAM holds the ISA-MWAC command queue, interrupt queue and the data buffers and buffer descriptors for data going to and coming from the serial interfaces. The host gains access to these structures through the I/O mapped ports. To read or write a location in DRAM, the host must:

- Load the lower 16 bits of the DRAM address into IP5 (DRAM address pointer—lower 16 bits)
- Load the upper 4 bits of DRAM address into the four least significant bits of IP6 (DRAM address—upper 4 bits/control)
- Read or write IP7 (DRAM data port) to complete the access.

In systems using 16-bit host access, DRAM data is accessed 16 bits at a time from IP7. In 8-bit systems, DRAM data is accessed 8 bits at a time, from the low-order (even addressed) byte of IP7. The high-order byte of IP7 is not used in 8-bit systems.

Table 8. ISA-MWAC ISA I/O Ports

Address	IP#	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base + 0	IP0	Status and Control															
Base + 2	IP1	Pipe Active Bits															
Base + 4	IP2	Programmable I/O Control and Access															
Base + 6	IP3	—								Interrupt Status							
Base + 8	IP4	—															
Base + 0xA	IP5	DRAM Address Pointer Port—Lower 16 Bits															
Base + 0xC	IP6	—	NAI	SA										DRAM Address Pointer Port—Upper 4 Bits			
Base + 0xE	IP7	DRAM Data Port															

ISA Interface Description (continued)

ISA I/O Port Overview (continued)

Accessing DRAM Through the I/O Ports (continued)

Note that when NAI = 0 in IP6 (no automatic increment of DRAM address control bit, bit 14), the ISA-MWAC will automatically increment the DRAM address pointer after every read or write to IP7. If a 16-bit access is performed to IP7 (even address), the DRAM address pointer will be incremented by two. If an 8-bit access is made to the lower byte (even address) of IP7, the pointer will be incremented by one. If a 16-bit even access is followed by an 8-bit high-byte (odd) access, the 16-bit access will be performed on the 2 bytes located at the address pointed to by the DRAM address pointer, and the subsequent 8-bit access will be performed on the high-order byte of the previously accessed word. This operation is necessary to allow software designed for 16-bit I/O accesses to be compatible with 8-bit platforms. An 8-bit access to the low-order byte of IP7 (even byte) followed by an 8-bit access to the high-order byte (odd byte) is not allowed.

When NAI = 1, repeated accesses to IP7 will not increment the entire DRAM address pointer (the host must manually change the pointer). See the NAI bit description in Table 15 for more information.

When the host accesses DRAM through the T7903, the chip may request that the cycle be extended by deasserting IOCHRDY (driving it low). This may occur when the host attempts to access the local DRAM while the T7903 is servicing one of its long pipes. These long pipes are 128-byte deep FIFOs that are used to interface the data in DRAM with the serial interfaces. For data being received from the outside world on a serial interface, the data collects in the pipe up to some programmed fill level (usually 64 bytes). When the fill level is reached, the T7903 will move the block of data to a receive buffer in DRAM. If, during this process, the host begins an access to the DRAM data port (IP7), the cycle will be extended. A similar situation can occur for data to be transmitted on a serial interface. The minimum cycle extension that the ISA-MWAC can request is 1 wait-state (125 ns). The maximum is 5.53 µs, which is comprised of 64 DRAM accesses (each 2 RCLK cycles long plus 2 cycles of overhead), and a DRAM refresh cycle (4 RCLK cycles). Note that this maximum time is for a programmed fill level of 64 bytes (FL = 1 in IP0, bit 13). This allows 64 bytes to accumulate (either in DRAM for transmit data or in a long pipe for receive data) before processing occurs. For FL = 0, processing occurs when 32 bytes accumulate, and thus the maximum cycle extension would be 2.85 µs.

ISA wait-states may also be required when the DRAM address pointer (IP5 or 6) is written before reading or after writing the DRAM data port (IP7). But, because of internal buffering between the ISA and DRAM interfaces (8 bytes for reads and 4 bytes for writes), wait-state requirements are kept to a minimum. In the case of writing the DRAM pointer and then reading IP7, the T7903 will do a 4-byte fast page mode read to DRAM (starting at the address pointed to by the DRAM address pointer), even if only a single byte is requested. This will cause IOCHRDY to assert while the 4 bytes are fetched. The host then has standard access to these 4 bytes without additional wait-states. Meanwhile, four more bytes are simultaneously fetched from DRAM. This process continues until the host changes IP5 or IP6. Thus, large blocks of data can be read from DRAM with only the first access incurring any additional wait-states. In the case of writes to DRAM, bytes from the host will collect in an internal 4-byte buffer. Once 4 bytes have been collected, DRAM will be automatically updated with these bytes via a fast page mode write. DRAM will also be updated when less than four bytes are buffered if the DRAM address pointer is written. Wait-states may be necessary if the host accesses IP7 while the ISA-MWAC is writing DRAM. Note that reads to IP5 and IP6 always provide the T7903's internal value for the DRAM address pointer. The value read indicates the next DRAM address to be buffered, not the next address accessible by the host.

The Staging Area: Accessing the Command Queue Pointer

After configuring the control bits in the I/O port registers, setting up the interrupt queue (see the Interrupts section for more details) and creating the command queue in DRAM (see the Commands section), the host must instruct the T7903 to begin command execution. This is done by loading the command queue's address (in DRAM) into the command queue pointer. The command queue pointer, however, is not part of the I/O port registers, but resides in another functional block called the staging area. The staging area is a block of internal memory mapped into the first 128 bytes of local DRAM space. It serves as an interface between internal chip blocks and also contains the command queue pointer. Its operation is generally transparent to the host except for the command queue pointer function. The command queue pointer is located at address 0x40 of the staging area and is accessed through indirect addressing by performing the following four operations:

- Load IP5 (DRAM address pointer port—lower 16 bits) with 0x0040 (the address of the command queue pointer in the staging area).

ISA Interface Description (continued)

ISA I/O Port Overview (continued)

The Staging Area: Accessing the Command Queue Pointer (continued)

- Load IP6 (DRAM address pointer port—upper 4 bits/ control) with 0x6000. This disables automatic incrementing of the address pointer (NAI = 1) and enables staging area access (SA = 1).
- Write the low-order 16 bits of the command queue's address into IP7 (DRAM data port).
- Write the high-order 4 bits of the command queue's address into the low-order 4 bits of IP7 (DRAM data port).

The T7903 will immediately begin executing commands from the command queue.

Important: When loading the command queue pointer in the staging area, all 32 bits must be written in consecutive accesses to IP7 (even though the address in DRAM requires a maximum of only 20 bits). This means that two 16-bit writes or four 8-bit writes must be made to IP7 before command execution will begin.

Note that the command queue pointer in the staging area will be reset to all zeros after powerup, a software or a hardware reset. Setting the P bit in IP0 (IP0, bit 15) causes the T7903 to begin execution of the commands in the command queue at the address pointed to by the command queue pointer. Therefore, an alternate method of starting command execution after powerup or reset is to place the command queue at location 0x00000 in DRAM and set the P bit. The T7903 will begin executing commands immediately.

ISA I/O Port Bit Descriptions

Tables 9 through 16 describe the function of the bits in the T7903 I/O ports.

IP0: Status Control Register

Table 9. IP0: Status Control Register Description (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P	LPM	FL	—	ID1	ID0	ICPIOM	BO	NP2	NP1	NP0	CHI	—	—	HALT	RESET

Field	Bit	Name/Description
P	15	**Pointer to the Command Queue is Valid.** This bit is set by the host CPU to initiate execution of the command queue starting at the DRAM address currently pointed to by the command queue pointer. It is also set by the ISA-MWAC when the command queue pointer is written by the host. It is cleared by the ISA-MWAC when a WAIT command is executed from the command list. Default: P = 0.
LPM	14	**Low-Power Mode.** When LPM = 1, the oscillator clock is gated and the analog block is powered down. To initiate a complete powerdown, first software reset the device (RESET = 1, IP0, bit 0), then program LPHRCL = 1 (IP4, bit 15), and finally set LPM = 1. To power the chip back up, program LPM = 0 first, then LPHRCL = 0 and again software reset the chip. **Note that when the chip is in low-power mode, LPM is the only register bit that can be accessed. The host must program LPM = 0 first, and then LPHRCL = 0 for proper operation.** Default: LPM = 0.
FL	13	**FIFO Level.** If FL = 1, the ISA-MWAC processes data when 64 bytes have accumulated in a long pipe (if possible). If FL = 0, processing occurs at 32 bytes. Default: FL = 0.
—	12	**Reserved.** Program to 0.
ID1	11	**ID Bit 1.** This bit reports the current value of device pin PNPID1/PIO5/$\overline{CS1}$ when read (Read Only).
ID0	10	**ID Bit 0.** This bit reports the current value of device pin PNPID0/PIO4/$\overline{CS0}$ when read (Read Only).
ICPIOM	9	**Interrupt on Change of PIO Mask.** When ICPIOM = 1, changes on PIO pins will be reported to the host via interrupt. This only reports PIO changes when the associated ENPIO bit in IP2 is programmed to 0 (the PIO is an input). When ICPIOM = 0, this interrupt is disabled. Default: ICPIOM = 0.

ISA Interface Description (continued)

ISA I/O Port Bit Descriptions (continued)

IP0: Status Control Register (continued)

Table 9. IP0: Status Control Register Description (Read/Write) (continued)

Field	Bit	Name/Description
BO	8	**Byte Order.** BO determines the ordering of bytes within the data words stored in local DRAM. When BO = 1, the order is little endian (the bits are stored in order from bit 0 in the LSB position to bit 15 in the MSB position). When BO = 0, the order is big endian. This means that bits 0 through 7 are stored in bits 8 through 15 of the 16-bit data word and bits 8 through 15 are stored in bits 0 through 7 of the data word. Note that this refers only to the data in receive and transmit buffers. The commands and descriptors are always stored little endian. Default: BO = 1.
NP2	7	**Permit Activation of NP2.** When NP2 = 1, network port 2 can activate. When NP2 = 0, network port 2 is disabled. Default: NP2 = 0.
NP1	6	**Permit Activation of NP1.** When NP1 = 1, network port 1 can activate. When NP1 = 0, network port 1 is disabled. Default: NP1 = 0.
NP0	5	**Permit Activation of NP0.** When NP0 = 1, network port 0 can activate. When NP0 = 0, network port 0 is disabled. Default: NP0 = 0.
CHI	4	**Permit Activation of CHI.** When CHI = 1, the CHI can activate. When CHI = 0, the CHI is disabled. Default: CHI = 0.
—	3	**Reserved.** Program to 0.
—	2	**Reserved.** Program to 0.
HALT	1	**Halt for Analysis.** Programming HALT = 1 halts the ISA-MWAC from accessing the data associated with all long pipes in the DRAM, but allows the ISA-MWAC to continue executing commands. Any command that controls a data pipe (SDP and DTS commands) is delayed in its execution until the HALT bit is cleared. Issuing commands with HALT = 1 is not recommended, since overruns and underruns may occur. Default: HALT = 0.
RESET	0	**Reset.** This bit is set by the host CPU to reset the ISA-MWAC. This bit is cleared internally when the ISA-MWAC has completed its internal initialization process approximately 500 RCLK periods (20.3 µs) after RESET. This bit is also set on hardware reset and clears itself in the same way. Setting this bit initiates an internal initialization procedure that releases all time slots, clears all pipes, and resets the I/O ports to their defaults. It does not reset the Plug and Play registers or the DRAM refresh circuitry.

ISA Interface Description (continued)

ISA I/O Port Bit Descriptions (continued)

IP1: Pipe Activity Register

Table 10. IP1: Pipe Activity Register Description (Read Only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

Field	Bit	Name/Description
PA15—0	15—0	**Pipe Active Bits.** The ISA-MWAC sets these bits to indicate that the associated long pipes are currently active. The following two conditions must be true for a Pipe Active bit to be set: 1) An SDP command has been issued for the pipe with PTR = 1 and a valid descriptor pointer, and 2) An end of list condition has not been encountered.

IP2: Programmable I/O Control and Access Register

Table 11. IP2: Register Description (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENPIO 7	ENPIO 6	ENPIO 5	ENPIO 4	PIO 7	PIO 6	PIO 5	PIO 4	ENPIO 3	ENPIO 2	ENPIO 1	ENPIO 0	PIO 3	PIO 2	PIO 1	PIO 0

Field	Bit	Name/Description
ENPIO7	15	**PIO Enable for PIO7.**
ENPIO6	14	**PIO Enable for PIO6.**
ENPIO5	13	**PIO Enable for PIO5.**
ENPIO4	12	**PIO Enable for PIO4.**
PIO7	11	**Parallel Input/Output 7.**
PIO6	10	**Parallel Input/Output 6.**
PIO5	9	**Parallel Input/Output 5.**
PIO4	8	**Parallel Input/Output 4.**
ENPIO3	7	**PIO Enable for PIO3.**
ENPIO2	6	**PIO Enable for PIO2.**
ENPIO1	5	**PIO Enable for PIO1.**
ENPIO0	4	**PIO Enable for PIO0.**
PIO3	3	**Parallel Input/Output 3.**
PIO2	2	**Parallel Input/Output 2.**
PIO1	1	**Parallel Input/Output 1.**
PIO0	0	**Parallel Input/Output 0.**

If an enable bit is set to 1 (ENPIO0—7; bits 4—7 and 12—15), then the PIO pin associated with that enable is configured as an output and is driven by the associated PIO bit (PIO0—7; bits 0—3 and 8—11). If the enable bit is cleared to 0, the PIO pin associated with that enable is in a high-impedance state. When IP2 is read, the PIO bits come from the PIO pins whether the pin is configured as an input or an output. This means that if signals to the PIOs change while they are being read, the system data bus may glitch. If ICPIOM = 1 (IP0, bit 9), changes on PIO pins will be reported to the host via interrupt. This only reports PIO changes when the associated enable bit is programmed to 0. The default state of IP2 is 0x0F0F.

ISA Interface Description (continued)

ISA I/O Port Bit Descriptions (continued)

IP3: Interrupt Register

Table 12. IP3: Interrupt Register Description (Read Only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—													ICPIO	—	IRI

Field	Bit	Name/Description
—	15—3	**Reserved.** Program to 0.
ICPIO	2	**Interrupt on Change of PIO.** If ICPIOM = 1 (this interrupt is enabled), ICPIO is set to 1 by the T7903, if at least one of the PIO pins is configured as an input and one of these input PIOs has changed its binary state. When ICPIO is set by the T7903, the IRQ pin will be driven high. IP2 must be read to determine which pin(s) changed. When IP3 is read, the IRQ pin is deasserted (driven low) and ICPIO is cleared. Default: ICPIO = 0.
—	1	**Reserved.** Program to 0.
IRI	0	**Interrupt Request Indicator.** When an interrupt occurs (except for ICPIO), IRI is set to 1 by the ISA-MWAC and the IRQ pin is driven high. When IP3 is read, the IRQ pin is deasserted (driven low) and IRI is cleared. Default: IRI = 0.

IP4: ROM Clock Control and Reserved Function Register

Table 13. IP4: ROM Clock Control and Reserved Function Register Description (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPHRCL	—														

Field	Bit	Name/Description
LPHRCL	15	**Low-Power Halt ROM Clock Low.** When LPHRCL = 1, the internal ROM clock is forced low, resulting in minimum ROM power consumption. For more detailed information, refer to the LPM bit description in the IP0 register description. Default: LPHRCL = 0.
—	14—0	**Reserved.** Program to 0.

IP5: DRAM Address Pointer Port—Lower 16 Bits

Table 14. IP5: DRAM Address Pointer Port—Lower 16 Bits (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM Address Pointer Port—Lower 16 Bits															

Field	Bit	Name/Description
—	15—0	**DRAM Address Pointer Port—Lower 16 Bits.** The locations in local DRAM are addressed through IP5 and the lower 4 bits of IP6. IP5 defaults to 0xFFFF.

ISA Interface Description (continued)

ISA I/O Port Bit Descriptions (continued)

IP6: DRAM Address Pointer Port—Upper 4 Bits/Control

Table 15. IP6: DRAM Address Pointer Port—Upper 4 Bits/Control (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	NAI	SA	—									DRAM Address Pointer Port—Upper 4 Bits			

Field	Bit	Name/Description
—	15	**Reserved.** Program to 0.
NAI	14	**No Automatic Increment of DRAM Address Control.** When NAI = 0, the ISA-MWAC will automatically increment the DRAM address pointer after every read or write to IP7 (DRAM data port). The pointer will wrap around to all zeros after 0xFFFFF. When NAI = 1, repeated reads or repeated writes to IP7 will cause the DRAM address pointer to automatically increment through the least significant 2 bits (4 bytes). In the case of a read access followed by a write access, the write will be performed on the same location as the preceding read. In this way, read-modify-write operations can be performed without rewriting the DRAM address pointer. The NAI bit defaults to 0.
SA	13	**Access to On-Chip Staging Area.** When SA = 1, access to the chip's internal staging area is enabled. Internal to the ISA-MWAC is a 32-word (32 bits per word) staging area mapped into the first 128 bytes of DRAM address space. One of the words in the staging area is the command queue pointer (CQP). The remaining 31 words are reserved. The command queue pointer is located at address 0x40 of the staging area and is accessed through indirect addressing as follows: ■ Load IP5 (DRAM address pointer port—lower 16 bits) with 0x0040 (the address of the command queue pointer in the staging area). ■ Load IP6 (DRAM address pointer port—upper 4 bits/control) with 0x6000. This disables automatic incrementing of the address pointer (NAI = 1) and enables staging area access (SA = 1). ■ Write the low-order bits of the command queue's address into IP7 (DRAM data port). ■ Write the high-order bits of the command queue's address into IP7. The T7903 will immediately begin executing commands from the command queue. **Important: When loading the command queue pointer in the staging area, all 32 bits must be written in consecutive accesses to IP7 (even though the address in DRAM requires a maximum of only 20 bits). This means that two 16-bit writes or four 8-bit writes must be made to IP7 before command execution will begin.** When SA = 0, access to the staging area is disabled (the first 128 bytes of DRAM are accessed instead of the staging area). The SA bit defaults to 1. **Note**: The command queue pointer in the staging area will be reset to all zeros after powerup, a software or a hardware reset. Setting the P bit in IP0 (IP0, bit 15) causes the T7903 to begin execution of the command list at the address pointed to by the command queue pointer. Therefore, an alternate method of starting command execution after powerup or reset is to place the command queue at location 0x00000 in DRAM and set the P bit. T7903 will begin executing commands immediately.
—	12—4	**Reserved.** Program to 0.
—	3—0	**DRAM Address Pointer Port—Upper 4 Bits.** The locations in local DRAM are indirectly addressed through IP5 and the lower 4 bits of IP6. These bits default to 1.

ISA Interface Description (continued)

ISA I/O Port Bit Descriptions (continued)

IP7: DRAM Data Port

Table 16. IP7: DRAM Data Port (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAM Data Port															

Field	Bit	Name/Description
—	15—0	**DRAM Data Port.** DRAM data is accessed through this port.

Plug and Play Support

If pin 69, ENPNP is strapped to V_{DD}, the T7903 will support *Microsoft's* Plug and Play ISA Specification (Plug and Play version 1.0a, 5/5/94) allowing software control of I/O space base address and interrupt level selection. The T7903 requires 16 consecutive bytes of I/O space when in normal I/O mode and 32 consecutive bytes when in extended I/O chip select mode (see the Programmable I/O Pins (PIOs) section for more information). This I/O block must be located in the range from 0x200 to 0x3e0. The chip also requires the use of one of the following ISA interrupt pins: IRQ3, 5, 7, 10, 11, 12, or 15.

The remainder of this section will focus on the details of Plug and Play as necessary for initialization of the T7903, with emphasis placed on non-Plug and Play environments. Consult the Plug and Play specification (Plug and Play version 1.0, 6/2/93) for more details. See Appendix G for details on disabling Plug and Play support entirely.

Plug and Play Overview

The Plug and Play specification defines the software and hardware required to allow compatible cards to be inserted and initialized for use without any user intervention. It provides a means for software allocation of I/O space, memory space, DMA channels, and interrupt levels (note that the ISA-MWAC does not require DMA or memory resources).

The Plug and Play specification outlines five major steps to autoconfigure a card.

1. Put all Plug and Play ISA cards into configuration mode.
2. Isolate one Plug and Play ISA card at a time.
3. Assign each card a unique number (card select number—CSN) and read its resource requirements.
4. After all cards' resource requirements are determined, use each card's CSN to assign conflict-free resources to that card.
5. Activate all PNP cards and take them out of configuration mode.

Each Plug and Play compatible device has three dedicated 8-bit I/O ports, called autoconfiguration ports. Through these ports, the host can access internal registers to perform the steps listed above and configure the device for operation.

Important: The Plug and Play ports are 8-bit ports. Access to these ports is over the lower 8 bits of the T7903 data bus (SD0—SD7).

Autoconfiguration Ports and the Configuration Space

The autoconfiguration ports are shown in Table 17. Through these ports, the T7903's configuration space can be accessed. This space holds the following:

- Serial identification information: vendor ID and serial/unique number.
- Resource requirements: Plug and Play version, identification information, I/O space requirements, and interrupt requirements.
- Plug and Play control and configuration registers.

Table 17. Plug and Play Autoconfiguration Ports

I/O Address	I/O Port Name	Access Allowed
0x279	Address Port	Write only
0xA79	Write_data Port	Write only
0x203—0x3FF*	Read_data Port	Read only

* The Read_data port is relocatable. Default address upon powerup or hardware reset of the T7903 is 0x203. After activation of the ISA interface, the Read_data port is no longer accessible. However, the address port is always accessible and care should be taken to avoid selecting a T7903 I/O space that overlaps address 0x279.

ISA Interface Description (continued)

Plug and Play Support (continued)

Autoconfiguration Ports and the Configuration Space (continued)

The Plug and Play configuration space contains various control and configuration registers that are accessed indirectly using the autoconfiguration ports. To do this, first the address of the register must be written to the address port. Then, to read the register's data, the host must read the Read_data port. To write data to the register, the host must write to the Write_data port. The control registers supported by the T7903 are shown in Table 18 and the configuration registers are shown in Table 19.

Table 18. Plug and Play Control Registers

Name	Comment	Address Port Value	Access Allowed
Set RD_DATA Port	Used to relocate the Read_data port from its default of 0x203. These 8 bits become bits 9—2 of the RD_Data port I/O address (bits 1 and 0 are always ones).	0x00	Write only
Serial Isolation	—	0x01	Read only
Config Control	—	0x02	Write only
Wake (CSN)	—	0x03	Write only
Resource Data	—	0x04	Read only
Status	Bit 0 always reads back a 1.	0x05	Read only
Card Select Number	—	0x06	Read/Write
Logical Device Number	Bit 0 always reads back a 0.	0x07	Read only
Activate	—	0x30	Read/Write
I/O Range Check	—	0x31	Read/Write

Table 19. Plug and Play Configuration Registers

Name	Comment	Address Port Value	Access Allowed
I/O Port Base Address Bits[15:08] Descriptor 0	—	0x60	Read/Write
I/O Port Base Address Bits[07:00] Descriptor 0	—	0x61	Read/Write
Interrupt Request Level Select 0	Program to 0x03, 0x05, 0x07, 0x0A, 0x0B, 0x0C, or 0x0F (IRQ3, 5, 7, 10, 11, 12, or 15).	0x70	Read/Write
Interrupt Request Type Select 0	Always reads back 0x02 (edge triggered, high active).	0x71	Read only
DMA Channel Select 0	Always reads back 0x04 (no DMA support).	0x74	Read only
DMA Channel Select 1		0x75	Read only

ISA Interface Description (continued)

Plug and Play Support (continued)

Plug and Play States

There are four states used by the Plug and Play hardware:

- Wait for Key
- Sleep
- Isolation
- Config

After powerup or reset, all cards enter the Wait for Key state. Each card has the ability to be programmed with a unique identifier, called the card select number (CSN), but after reset all CSNs are cleared to 0. All cards' ISA interfaces are inactive and do not respond to any accesses. The host then writes a pattern called the Initiation Key to all cards that moves them to the Sleep state. In the Sleep state, the autoconfiguration ports for each card are enabled. The host then issues a Wake [CSN = 0] command to the cards to cause them to enter the Isolation state, preparing them for the isolation sequence. After the first isolation sequence is performed, only one card remains in the Isolation state; all others have dropped back to the Sleep state. A nonzero CSN is then given to the isolated card, moving it to the Config state. The card's resource needs are read and the card is returned to the Sleep state. The isolation sequence is repeated until all cards are given unique CSNs and have provided their resource needs to the Plug and Play software. At this point, all cards are individually brought back to the Config state (using the Wake [CSN] command), programmed with the necessary resource allocations and then activated for normal operation. After each card is activated, they are put back into the Wait for Key state.

Initiation Key

Upon powerup or hardware reset, the T7903 (and all other Plug and Play compatible devices in the system) are placed in the Wait for Key state and their CSNs are reset to 0. The host must write a predefined pattern, called the Initiation Key, to the address port (address 0x279; see Table 17) to move the device to the Sleep state. The pattern in hexadecimal notation is:

6A, B5, DA, ED, F6, FB, 7D, BE,
DF, 6F, 37, 1B, 0D, 86, C3, 61,
B0, 58, 2C, 16, 8B, 45, A2, D1,
E8, 74, 3A, 9D, CE, E7, 73, 39

This key must be written to the ISA-MWAC after powerup or hardware reset (not software reset) in both Plug and Play and non-Plug and Play systems, if Plug and Play is enabled.

Isolation Protocol

All Plug and Play compatible cards in a system have their three autoconfiguration ports mapped to the same addresses, but each card must be polled individually to determine its resource requirements. For this reason, an isolation protocol is required. The protocol uses a 72-bit number unique to each card (called the serial identifier) for individual card isolation. The isolation protocol accesses the serial identifier through the Read_data port via 72 pairs of I/O reads to the serial isolation register (control register 0x01—see the Isolation Protocol section of the Plug and Play Specification for more details).

The isolation protocol is not necessary when using the T7903 in non-Plug and Play systems. A transition from the Isolation state to the Config state can be forced by writing a nonzero CSN. See the Initialization in Systems not Supporting Plug and Play section of this document.

The Config State: Determining and Allocating Resource Requirements

Once in the Config state, a Plug and Play compatible device can be polled to find its resource requirements. They are accessed by reading the resource data register located at 0x04. The following listing gives the output of the T7903 in response to 48 eight-bit reads of the resource data register. The first 9 bytes make up the serial identifier used in the isolation protocol. The remaining 39 bytes describe resource information and are comprised of the Plug and Play version, card ID, logical device ID, I/O port requirements, and interrupt requirements. Note that this list shows the data that is available from the resource data register if the isolation protocol was not used previous to the resource data register access. If the isolation protocol was used prior to accessing the resource requirements, the serial identifier would not be available from the resource data register (it would have been read out during the isolation protocol execution) and only the 39 bytes of resource information would be read out.

ISA Interface Description (continued)

Plug and Play Support (continued)

The Config State: Determining and Allocating Resource Requirements (continued)

```
/* Plug and Play Serial Identifier (9 bytes) */
0xa731      /* 16 bits of vendor ASCII EISA ID "LMG" */
0x0X0Y      /* 16 bits of vendor product and revision numbers */
            /* X is equal to silicon version number (i.e., X = 5 means version FC5) */
            /* Y is equal to 3 for T7903 */
0x000X      /* 16 bits of serial/unique number */
            /* X = 0x0 for PNPID[1:0] = 00 */
            /* X = 0x1 for PNPID[1:0] = 01 */
            /* X = 0x2 for PNPID[1:0] = 10 */
            /* X = 0x3 for PNPID[1:0] = 11 */
0x0000      /* 16 bits of serial/unique number */
0xXX        /* 8 bit checksum */
            /* X = 0x9a for PNPID[1:0] = 00 */
            /* X = 0x86 for PNPID[1:0] = 01 */
            /* X = 0x69 for PNPID[1:0] = 10 */
            /* X = 0xa8 for PNPID[1:0] = 11 */

/* Plug and Play Resource Information (39 bytes) */

0x0a        /* Small resource data type tag: PNP Version Number */
0x10        /* 8 bits of PNP ver 1.0 */
0x0X        /* X is equal to silicon version number (i.e., X = 5 means version FC5) */

0x82        /* Large resource data type tag: ANSI Card ID */
0x000e      /* 16 bits of string length: 14 bytes of ID */
0x4e445349  /* 32 bits of string descriptor "ISDN" */
0x41534920  /* 32 bits of string descriptor "ISA" */
0x41574d2d  /* 32 bits of string descriptor "-MWA" */
0x3543      /* 16 bits of string descriptor "C5" */

0x15        /* Small resource data type tag: Logical Device ID */
0x0000      /* 16 bits of logical device ID bits [15:0] */
0x0000      /* 16 bits of logical device ID bits [31:16] */
0x00        /* 8 bits of vendor specific commands and BOOT FLAG */

0x47        /* Small resource data type tag: I/O Port Resource Requirements */
0x00        /* 8 bits of 10-bit SA decode indication */
0x0200      /* 16 bits of min base address */
0x03e0      /* 16 bits of max base address */
0xXX        /* 8 bits of base addr inc.
            /* XX = 0x10 for normal mode: 16 bit aligned */
            /* XX = 0x20 for extended mode: 32 bit aligned */
0xXX        /* 8 bits of no. of ports */
            /* XX = 0x10 for normal mode (PNPID0 or PNPID1 = 0): 16 ports */
            /* XX = 0x20 for extended mode (PNPID0 = PNPID1 = 1): 32 ports */

0x22        /* Small resource data type tag: IRQ Requirements */
0x9cA8      /* 16 bits of IRQ selection; IRQ15, 12, 11, 10, 7, 5, and 3*/

0x79        /* 8 bits of END TAG */
0x00        /* Checksum */
```

ISA Interface Description (continued)

Plug and Play Support (continued)

The Config State: Determining and Allocating Resource Requirements (continued)

After all boards in a Plug and Play system have been isolated and their resource requirements read, they are individually brought back to the Config state for resource allocation and ISA interface activation. After activation, the cards are returned to the Wait for Key state.

Initialization in Systems Not Supporting Plug and Play

It is often useful to use the T7903's Plug and Play interface in non-Plug and Play systems. One reason for doing this is that the programmable I/O address decoder in the chip alleviates the need for an external decoder. If ENPNP (pin 69) is strapped to V_{DD} during powerup or hardware reset, the T7903's Plug and Play mode will be enabled and the ISA interface will be inactive (Wait for Key state). A base address for its I/O space must be assigned, an interrupt pin must be designated (IRQ3, 5, 7, 10, 11, 12, or 15), and the ISA interface must be activated. When the T7903 is used in systems that do not support Plug and Play initialization, the software driver must perform these tasks. The following listing shows the required I/O writes necessary to bring the device up with a base I/O address of 0x280 and an interrupt request on IRQ15. The format for the I/O writes in this example is: out (port address, data).

```
/* Current State = Wait For Key State */
/* Reset Initiation and send Initiation Key for transition to Sleep state */
            out (0x279, 0x00) /* RESET INITIATION KEY */
            out (0x279, 0x00) /* RESET INITIATION KEY */
            out (0x279, 0x6a) /* PNP INITIATION KEY */
            out (0x279, 0xb5) /* PNP INITIATION KEY */
            out (0x279, 0xda) /* PNP INITIATION KEY */
            out (0x279, 0xed) /* PNP INITIATION KEY */
            out (0x279, 0xf6) /* PNP INITIATION KEY */
            out (0x279, 0xfb) /* PNP INITIATION KEY */
            out (0x279, 0x7d) /* PNP INITIATION KEY */
            out (0x279, 0xbe) /* PNP INITIATION KEY */
            out (0x279, 0xdf) /* PNP INITIATION KEY */
            out (0x279, 0x6f) /* PNP INITIATION KEY */
            out (0x279, 0x37) /* PNP INITIATION KEY */
            out (0x279, 0x1b) /* PNP INITIATION KEY */
            out (0x279, 0x0d) /* PNP INITIATION KEY */
            out (0x279, 0x86) /* PNP INITIATION KEY */
            out (0x279, 0xc3) /* PNP INITIATION KEY */
            out (0x279, 0x61) /* PNP INITIATION KEY */
            out (0x279, 0xb0) /* PNP INITIATION KEY */
            out (0x279, 0x58) /* PNP INITIATION KEY */
            out (0x279, 0x2c) /* PNP INITIATION KEY */
            out (0x279, 0x16) /* PNP INITIATION KEY */
            out (0x279, 0x8b) /* PNP INITIATION KEY */
            out (0x279, 0x45) /* PNP INITIATION KEY */
            out (0x279, 0xa2) /* PNP INITIATION KEY */
            out (0x279, 0xd1) /* PNP INITIATION KEY */
            out (0x279, 0xe8) /* PNP INITIATION KEY */
            out (0x279, 0x74) /* PNP INITIATION KEY */
            out (0x279, 0x3a) /* PNP INITIATION KEY */
            out (0x279, 0x9d) /* PNP INITIATION KEY */
            out (0x279, 0xce) /* PNP INITIATION KEY */
            out (0x279, 0xe7) /* PNP INITIATION KEY */
            out (0x279, 0x73) /* PNP INITIATION KEY */
            out (0x279, 0x39) /* PNP INITIATION KEY */
```

ISA Interface Description (continued)

Plug and Play Support (continued)

Initialization in Systems Not Supporting Plug and Play (continued)

```
/* Current State = Sleep State */
            out (0x279, 0x02) /* Load Address Port with Config. Control reg. addr.*/
            out (0xa79, 0x05) /* Initiate Reset and Reset CSN Commands */
/* Send Wake[CSN = 0] to transition to Isolation State */
            out (0x279, 0x03) /* Load Address Port with Wake[CSN] reg. addr. */
            out (0xa79, 0x00) /* Write Wake[CSN] with 0x00 */
/* Current State = Isolation State */
/* No Isolation Protocol performed: assume only one T7903 board in system */
/* SET CSN = 0x01 to transition to Config. State */
            out (0x279, 0x06) /* Load Address Port with CSN reg. addr. */
            out (0xa79, 0x01) /* Write CSN = 0x01 */
/* Current State = Config State */
/* Set interrupt request to IRQ15 */
            out (0x279, 0x70) /* Load Address Port with IRQ sel. reg. addr. */
            out (0xa79, 0x0f) /* Write IRQ sel. = 0x0f for IRQ15 */
/* Set base I/O address = 0x280 */
            out (0x279, 0x60) /* Load Address Port with Upper I/O base reg. addr. */
            out (0xa79, 0x02) /* Write Upper Part I/O Base = 0x02 */
            out (0x279, 0x61) /* Load Address Port with Lower I/O base reg. addr. */
            out (0xa79, 0x80) /* Write Lower Part I/O Base = 0x80 */
/* Activate ISA interface */
/* Transition to Wait for Key State to Deactivate Plug and Play */
            out (0x279, 0x30) /* Load Address Port with Activate reg. addr. */
            out (0xa79, 0x01) /* Activate = 0x01 */
            out (0x279, 0x02) /* Load Address Port with Config. reg. addr. */
            out (0xa79, 0x02) /* go to Wait for Key State; Plug and Play disabled */
```

Internal Data Routing

The internal block diagram of the ISA-MWAC is shown in Figure 15. This shows the four serial interfaces, the ISA interface, and the DRAM interface, as well as the internal memory (data pipe memory) that routes data between them.

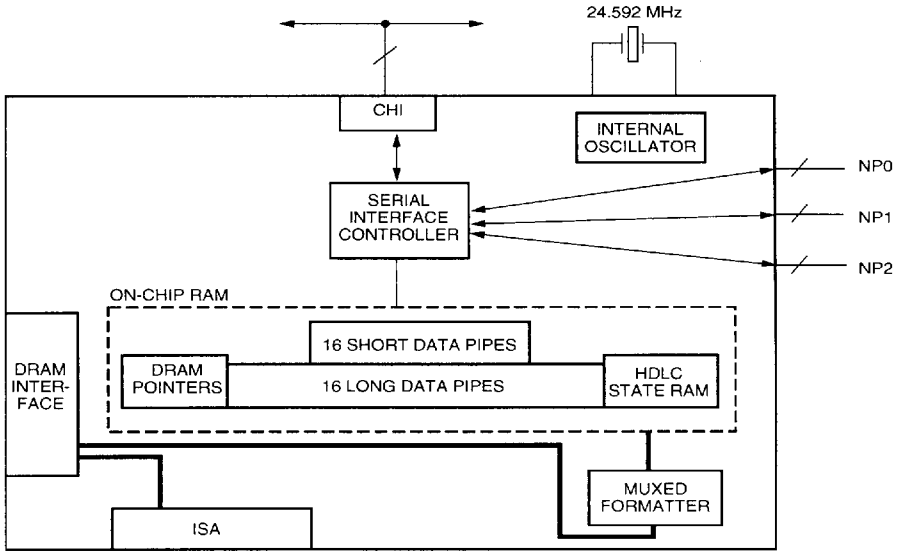


Figure 15. Internal Block Diagram

More About Data Pipes and Time Slots

The ISA-MWAC has 32 data pipes. All data transfers take place through these data pipes. Sixteen long data pipes have a direct memory access channel to local DRAM and are 128 bytes deep. Long pipes are numbered 0—15. Long pipes are normally used to pass data between a serial interface and DRAM and can optionally be configured for HDLC formatting. Long pipes can be used for serial to serial transfer if desired, but HDLC formatting cannot be performed.

Sixteen short data pipes are used for data transfer between any two serial interfaces (CHI, NP0, NP1, and NP2) and can have time slots assigned to both ends. Each short data pipe stores up to 32 bits of data. Short pipes are numbered 16—31.

The Setup Data Pipe command is used to initialize the mode, direction, pipe number, transmit/receive descriptor pointer, and other parameters of the data pipes.

Data Pipe Modes

Data can enter a pipe in one of three ways:

- DRAM: Data can come from a data structure in local DRAM.
- Serial: Data can come from a time slot on one of the serial interfaces (CHI, NP0, NP1, and NP2) as defined by a time-slot descriptor (TSD) associated with the data pipe. (See the DTS (0x7): Define Time-Slot Command section.)
- Fixed: Fixed data patterns can be set by the Set Short Pipe Data (SSP) command. (See the SSP (0x8): Set Short Pipe Data Command section.)

Similarly, data can leave a pipe in one of three ways:

- DRAM: Data can go to a data structure in local DRAM.
- Serial: Data can go to a time slot on one of the serial interfaces (CHI, NP0, NP1, and NP2) as defined by a TSD associated with the data pipe.
- Fixed: A change in fixed data can be reported in the interrupt queue in DRAM.

Any data pipe that is connected to DRAM or is fixed data on one end must be serial on the other end.

The data pipe modes are selected by the MODE field of the SDP command for each pipe. Two other parameters are selected by the MODE field. HDLC mode should be used if HDLC formatting is required on a pipe. HDLC—D-channel mode must be selected if a pipe is used as the transmit pipe for the D channel of a BRI TE network port interface.

Internal Data Routing (continued)

More About Data Pipes and Time Slots (continued)

Data Pipe Modes (continued)

Noncontiguous Mode. In the noncontiguous mode, multiple time slots from a serial interface can be assigned to the same pipe (see the Noncontiguous Mode section in the DTS (0x7): Define Time-Slot Command section of this document). For example, two-channel data from the same file can be put on two different time slots of the CHI for stereo applications.

Linked Lists and Anchor Pipes

To enable a serial interface to send or receive data, DTS commands must be used to form a circular linked list internal to the T7903. The linked list describes the polling order of data pipes that pass time-slot data to and from the interface and allows the T7903 to properly queue up all time slots. A separate linked list must be maintained for each serial interface used, and for each direction (transmit and receive). Therefore, a maximum of eight linked lists may be needed (one for each direction on the CHI, NP0, NP1, and NP2 interfaces). To form the linked lists, first use SDP commands to set up the data pipes for all required data paths through the chip. Then, for each time slot, use a DTS command to define the time slot's length and position in the serial bit stream, the pipe that the time slot connects to (PIPE field), the pipe that preceded this pipe in the linked list (Previous In/Out PIPE field), and the next pipe in the list (Next PIPE field).

It is important to note that the serial interface that a data pipe connects to (and that time slots are defined for) is not specifically named in the SDP and DTS commands. Where does this information come from? It is inferred by the use of anchor pipes. An anchor pipe is a dedicated pipe that, when used as the first pipe of a linked list, automatically assigns the pipes/time slots in that list to the associated serial interface. The T7903's dedicated NP0, NP1, and NP2 anchor pipes and their associated time slots are as follows:

NP0: receive time-slot list starts with pipe 0.
NP0: transmit time-slot list starts with pipe 1.
NP1: receive time-slot list starts with pipe 5.
NP1: transmit time-slot list starts with pipe 4.
NP2: receive time-slot list starts with pipe 3.
NP2: transmit time-slot list starts with pipe 2.

For example, whenever the NP0 port is used, pipe 0 must be used as the first (anchor) pipe of the linked list of pipes for the receive direction, and pipe 1 must be used as the first (anchor) pipe of the linked list of pipes for the transmit direction. Similarly, the NP1 port uses pipes 5 and 4 and NP2 uses pipes 3 and 2. Pipes 0 through 5 are reserved for this purpose. When the network ports are used in BRI mode, the anchor pipes shown above must be used for the D channels. It should be noted that when the network ports are used as BRI TEs, the transmit time-slot list anchor pipes (pipe 1, 2, and 4) must be assigned a special mode, HDLC D-channel mode, in the SDP commands for proper operation on a passive bus.

The CHI also has a dedicated anchor pipe that's used as the first pipe in its linked lists. Both the transmit and receive CHI linked lists must start with pipe 16 (CHI anchor pipe). One difference between the CHI anchor pipe and those used on the network ports is that pipe 16 does not actually transfer any data. No SDP command should be issued for pipe 16. It is used simply to tell the T7903 that the linked list that it anchors is for the CHI. Note that when pipe 16 is used to anchor a CHI transmit or receive linked list, CHI anchor mode must be selected in the MODE field of the time-slot descriptor portion of the DTS command.

When setting up the linked lists for the serial interfaces on the ISA-MWAC, four important rules must be followed. These define the sequence of DTS commands in the command queue as well as the values of the Previous In/Out PIPE and Next PIPE fields in the DTS commands.

Rule 1: Time slots on the CHI must be defined, via DTS commands, in the order they occur on the CHI.

Rule 2: Time slots on BRI-configured network ports must be defined, via DTS commands, starting with the D channel. Subsequent time slots must be defined in the order that they occur (i.e., B1, B2, S/Q). For example, to define D, B1, and B2 time slots for the receive direction on NP0, DTS commands must be placed in the command queue in the following order: D-channel receive DTS command using Pipe 0 (NP0 receive anchor pipe), B1 channel receive DTS command (using either a long or short pipe, depending on the data's destination), and B2 channel receive DTS command (again using a long or short pipe).

Rule 3: As each DTS command is executed by the T7903, the circular linked list must be maintained. For example, when creating the initial list of DTS commands for a serial interface, set the Next PIPE field in each DTS command to the anchor pipe for the list. Doing this ensures that connectivity to the beginning of the list is always maintained as the list grows. As each DTS command is executed by the T7903, the list always points back to the beginning.

Internal Data Routing (continued)

Linked Lists and Anchor Pipes (continued)

Rule 4: Always set up the SDP and DTS commands for the serial interface anchor pipes **before** executing CDM and NP commands, and **before** turning on the CHI and NP bits in IP0. For example, if the CHI is to be used, DTS commands setting up CHI anchor pipe 16 must be executed by the T7903 before any CDM command is executed (no SDP commands are used for pipe 16).

If the network ports are to be used, the network port anchor pipes (D-channel pipes) must be set up via SDP and DTS commands before any NP commands are executed. The recommended ordering of commands is shown below (note that the PAUSE command is used after SDP and DTS commands).

IIQ cmd
SDP cmds
DTS cmds
CGM cmd
PAUSE cmd
NP0 and CDM cmds
WAIT cmd

Then, execute the command list and, finally, turn on the CHI and NP bits in IP0, if these interfaces are to be used.

When inserting a new time slot between time slots that are already set up, the previous PIPE field must point to the previous time slot's pipe, and the next PIPE field must point to the next time slot's pipe. By doing this, time slots are serviced by the chip in the order that they occur on the serial interface. An example of this would be bringing up a B1 channel call on NP0 after having established a B2 channel call. In the transmit direction, a new DTS command must be executed for the B1 time slot, with the previous PIPE field pointing to pipe 1 (the NP0 D channel transmit anchor pipe) and the next PIPE field pointing to the B2 time slot's transmit pipe. A similar DTS command must be used for the receive direction, with the previous PIPE field pointing to pipe 0 (the NP0 D channel receive anchor pipe) and the next PIPE field pointing to the B2 time slot's receive pipe.

See the Commands section and Appendix C for more information.

Fixed I/O Channels

ISDN S and Q channels are supported on the basic rate interfaces. They can be connected to short data pipes, the other ends of which are in fixed I/O mode. Commands set a value for S and Q, which is output repeatedly until changed. If an incoming S or Q channel changes, the change is reported on the interrupt queue. Note that when receiving fixed data, the FXDT interrupt reports only the least significant 20 bits (see the Interrupts section of this document).

Delay Equalization in Support of BONDING

See the Bandwidth On Demand Interoperability Group's BONDING specification (version 1.0 Sept. 1, 1992) for details on the BONDING frame structure and protocol.

In brief, BONDING defines a method for communicating over multiple independent 56/64 kbits/s channels by:

1. Defining a frame structure which is transmitted over each channel.
2. Synchronizing and aligning the phase of each channel (via the frame structure) to recreate the original data stream.

Although the T7903 does not implement the BONDING algorithms, it does support two host assisted methods of equalizing the delays between multiple B channels or synchronous serial channels. These methods are:

1. Low-latency delay equalization of up to 15 ms by allowing the host to adjust the T7903's internal FIFO pointers.
2. Long delay equalization (greater than 15 ms) using the T7903's local (external) memory and software-controlled pointers.

These methods provide equalized data at the CHI.

Low-Latency Delay Equalization of Up to 15 ms

To perform low-latency delay equalization, software running on the receiving host must examine the BONDING frames coming from the far end and determine the delay between the channels. Once the individual delays between the earliest channel and each of the others has been determined, the delays can be equalized by adjusting the internal pointers used by the T7903's long pipes. A long pipe can be thought of as a 128-byte deep elastic storage buffer with a write pointer that is accessible by the host CPU via the CDP command.The following is an example of how delay equalization could be accomplished for multiple channels coming from the network ports and going to the CHI.

1. Set up calls on all ISDN B channels (or synchronous serial channels) that are to be equalized.

Internal Data Routing (continued)

Delay Equalization in Support of BONDING (continued)

Low-Latency Delay Equalization of Up to 15 ms (continued)

2. Using long pipes, connect the receive direction time slots from each of these channels to the CHI in contiguous time slots. These long pipes will carry the B channel data from the network ports to the CHI and provide the adjustable pointers necessary for delay equalization.
3. The contiguous time slots being transmitted out of the CHI must then be wrapped back to the CHI receiver and directed to memory as a single time slot. To do this, use a long pipe to connect the CHI receiver to DRAM and define a time slot wide enough to hold all of the contiguous octets from the network ports. The CHI should then be looped back to allow the BONDING frames from the network ports to be wrapped from CHI transmit to CHI receive and then to DRAM (through the CHI to DRAM long pipe). This loopback is enabled by execution of a CDM (CHI data mode) command with bit 7, RHI = 1. The size of the receive buffer in DRAM is dependent on the number of channels being equalized and the maximum delay expected.
4. The software must then search through the BONDING information in DRAM to determine the delays between the earliest channel and each of the other channels.
5. The T7903 supports phase delay equalization from one bit (15.6 µs on a 64 kbits/s ISDN B channel) to about 960 bits (15 ms on an ISDN B channel). This is accomplished by issuing a Continue Data Pipe (CDP) command with bit 15, PA, set to 1, and bits 4—0, PIPE, set to the number of the long pipe that connects to the channel needing equalization. When PA = 1, the T7903 interprets the Inc_value field of the CDP command as an offset to the long pipe's current write pointer position. In other words, the pipe's current write pointer (the pointer used to load the pipe's memory with data from a serial interface) is increased by the amount Inc_value. Inc_value must be the number of bits of delay equalization required. Therefore, the software must determine the delay between the channels (4 above) in bits and use this as the Inc_value field of a CDP command (with PA = 1).
6. Once all channels are equalized, the pipe from the looped back CHI is no longer necessary. The CHI loopback can also be removed.

Delay Equalization Greater than 15 ms

When channel delay is greater than 15 ms, the host can use the T7903's local DRAM to buffer the received data.

After the host determines the channel delay, the same buffers can be transmitted to the CHI using transmit buffer pointers (the TBA field of the transmit descriptor) offset by the appropriate amount to equalize delays.

Device Configuration

Device Synchronization

The ISA-MWAC is capable of synchronizing its serial interfaces in various ways. This flexibility allows the device to fit well into many applications at either the network or customer end of the wide area network. This section outlines the various ways that the T7903 can synchronize its serial interfaces.

Internal Phase-Locked Loop

The 24.592 MHz free-running crystal oscillator is counted down to 192 kHz with an occasional extra 24.592 MHz cycle added to the 192 kHz cycle. This allows the ISA-MWAC to meet the ITU-T I.430 requirements for phase jitter, for both TE and NT interfaces. This method is used to phase-lock the basic rate bit clocks.

Network Ports in BRI Mode

The network ports will synchronize to their received signals when configured as BRI TEs and will be the source of timing when they are NTs. When a port is configured as a TE and the CHI is in master mode, the CHI will synchronize to the activated TE port. Any interfaces configured as BRI NTs will also synchronize to the activated TE. If more than one network port is a TE, each will recover timing from their own received signal and the master mode CHI (and all NT ports) will synchronize to the first TE to activate. If no TE ports are active before the NT or CHI (master mode) are activated, then the first one to activate (NT or CHI) is free-running. Then, the next to activate (NT or CHI) synchronizes to the first. If the TE interface then becomes active, the NT and CHI are frequency-locked to the TE interface, but no specific phase relationship is maintained. The resulting phase misalignment does not affect operation.

Device Configuration (continued)

Device Synchronization (continued)

Network Ports in BRI Mode (continued)

Recommendation: For data transfers between a TE interface and either the CHI or an NT interface, activate the TE first. In this way, all interfaces are synchronized to the TE and, thus, the network.

If the CHI is used in slave mode, any NT-configured ports will be synchronous with the CHI. The CHI input CHIFS must be an 8 kHz signal.

Note: In CHI slave mode, the CHI synchronizes to the CHIFS input. If a network interface is then configured as a TE, data transmission between the CHI and the network can be unreliable.

Network Ports in Synchronous Mode

The network ports will synchronize to their received signals when configured as synchronous serial slaves and will be the source of timing when they are masters. When a port is configured as a slave and the CHI is in master mode, the CHI will synchronize to the activated slave port. Any interfaces configured as synchronous serial masters will also synchronize to the activated slave. If more than one network port is a slave, each will recover timing from their own received signal and the master mode CHI and all synchronous serial master ports will synchronize to the first slave to activate. If no slave ports are active before the master network port or CHI (master mode) are activated, then the first one to activate (master network port or CHI) is free-running. Then, the next to activate (master network port or CHI) synchronizes to the first. If the slave interface then becomes active, the master port and CHI are frequency-locked to the slave port.

TECK Operation

Device pin TECK can be configured as either an input or an output, as determined by STECK (bit 25 of the CGM command). When STECK = 1, TECK is a 4 kHz output that is synchronous with the first TE or synchronous slave-configured network port to activate. If no network ports of that type are activated, TECK is a free-running 4 kHz signal.

When STECK = 0, TECK is an input. The CHI (master mode only) and NT-configured network ports can synchronize to TECK, depending on the value of SSYNC (bit 24 of the CGM command). If SSYNC = 1, the CHI and NT ports will synchronize to an 8 kHz signal applied to TECK. If SSYNC = 0, TECK will be ignored (synchronization of the CHI and network ports is as described above).

Local DRAM

The T7903 requires local DRAM (or an optional SRAM circuit) organized into 8-bit words. The minimum amount of DRAM depends upon the command and interrupt queue sizes and data buffer requirements. The maximum size addressable is 1 Mbyte. The T7903 performs all necessary refresh of this local DRAM. DRAM devices must support the following features:

- 60 ns to 80 ns access time
- Fast page mode
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh

Appendix H describes how to use SRAM in place of DRAM.

Optional DRAM Arbitration

The private DRAM is normally accessed via I/O reads and writes. However, local DRAM arbitration is supported through the use of two pins, DRAMREQ and DRAMACK. These can be used in an arbitration scheme to prevent the ISA-MWAC from accessing DRAM, thereby allowing an external processor or host microprocessor to use the DRAM as a memory-mapped or shared-memory resource. The host (or arbitration logic) should assert DRAMREQ and wait for the T7903 to assert DRAMACK before beginning a DRAM access. During the host access, DRAMREQ must remain asserted.

For implementations in which there is an external arbitrator for the DRAM, care must be taken to not lock out the ISA-MWAC from the DRAM for long periods of time. See Appendix E Questions and Answers (Miscellaneous section) for more information. Also note that the ISA-MWAC only supports Plug and Play for its IRQs and I/O space. If the DRAMREQ and DRAMACK signals are used to map DRAM into system memory space or to support ISA's DRQ and DACK signals, support for Plug and Play must be provided external to the ISA-MWAC.

Note: If normal I/O mapped DRAM access is used, DRAMREQ must be tied low.

Device Configuration (continued)

Programmable I/O Pins (PIOs)

The T7903 has eight programmable I/O pins, called PIOs. These PIOs can be independently programmed, via register IP2, to be input or output pins. When programmed as inputs, they can be set up to interrupt the host processor when the data applied to them changes. Register IP0, bit 9 (ICPIOM), is used to enable this interrupt. IP3, bit 2 (ICPIO), is set by the T7903 to indicate that this interrupt has occurred. Reading IP3 clears the interrupt lead and the ICPIO bit. Note that no interrupt words are written to the interrupt queue for the ICPIO interrupt. An IIQ command is not required to enable this interrupt.

If Plug and Play support is enabled, two of the PIOs, PIO4 and PIO5, are polled during Plug and Play initialization. The polled state of these pins is returned to the host as part of the Plug and Play identifier. Since the state of these pins occupies 2 bits of the identifier, four unique IDs can be formed by the various strapping selections (high or low). This allows the Plug and Play software to uniquely identify up to four identical T7903 boards in the same system.

Extended I/O Chip Select Mode

PI04 and PI05 also have another function when Plug and Play support is enabled. If both PI04 and PI05 are pulled high during Plug and Play initialization, their PI0 function is automatically disabled. Instead, if the pins are programmed as outputs (see register IP2 description), they turn into active-low chip select outputs $\overline{CS0}$ and $\overline{CS1}$. This feature is called extended I/O chip select mode. The T7903 will ask the Plug and Play software for 32 consecutive bytes of I/O space instead of 16 bytes. The additional 16 bytes are not used by the T7903. Instead, accesses to this extended block are decoded by the T7903 (along with AEN). Any access to the first 8 bytes of extended space will cause $\overline{CS0}$ to assert low, and any access to the second block of 8 bytes causes $\overline{CS1}$ to assert low. See Figure 16. This is useful in Plug and Play systems that need additional address decoding for external board logic. **PIO4 and PIO5 must be programmed as outputs when using this mode.**

Note that $\overline{IOR}$ and $\overline{IOW}$ are not decoded as part of the chip select logic. This means that ISA memory accesses that fall within the 32-byte I/O space allocated to the T7903 will activate the chip select outputs. Therefore, the $\overline{CS0}$ and $\overline{CS1}$ outputs may need to be qualified externally with $\overline{IOR}$ and $\overline{IOW}$ in some applications.

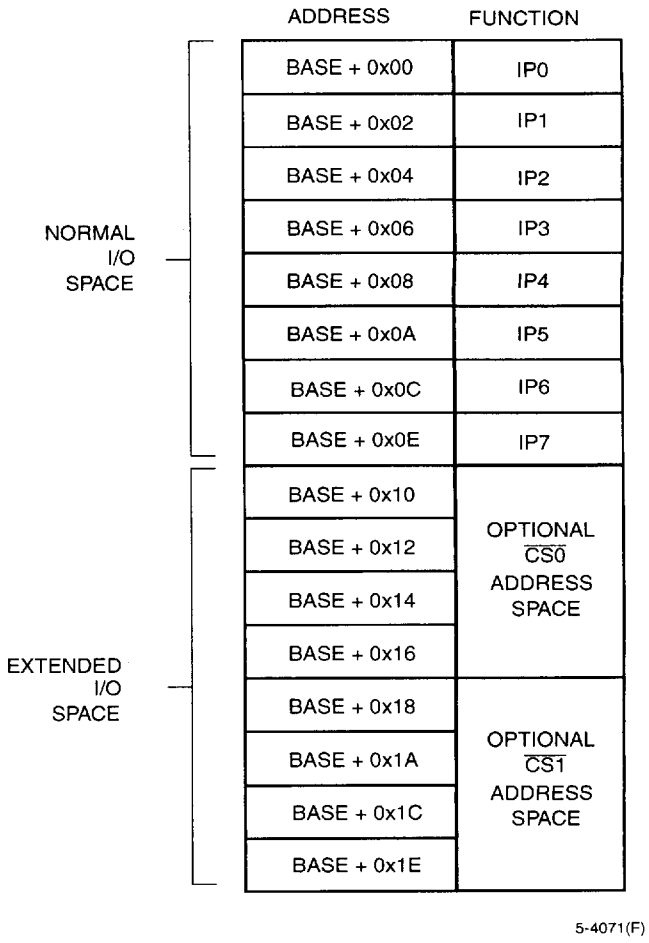


Figure 16. Extended I/O Chip Select I/O Space

Commands

Control of the ISA-MWAC is primarily accomplished by a string of commands in local DRAM. The host places these commands in consecutive bytes in DRAM with the WAIT command as the last command in the list. This is called the command queue. Execution of the command queue is started by writing the command queue pointer (see The Staging Area: Accessing the Command Queue Pointer section of this document).

Execution stops when the WAIT command is executed. Execution can be restarted by overwriting the WAIT command with a new command and setting the P bit in IP0 (pointer to command queue valid—IP0, bit 15). New commands can be executed by overwriting the old queue and rewriting the command queue pointer. Remember that arbitrarily long sequences of frames can be transmitted and received without intervening commands or interrupts.

Command Set Summary

Each command is at least one word (32 bits) in length. The first word contains the command opcode and various status and control bits. The second word usually contains a pointer (if needed). Table 20 lists all of the commands and their assigned opcodes.

Bits 31—28 contain the opcode of each command. If I = 1 (bit 27 of each command), a CMDI interrupt is issued when the T7903 reads the first word of the command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word, and other command bits are reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes (to determine if a certain instruction has or has not been executed). Reserved bits must be programmed to 0 except where noted.

Table 20. Command Descriptions

Opcode	Command	Command Description
0x0	WAIT	Wait.
0x1	PAUSE	Pause.
0x2	JMP	Jump to new command queue.
0x3	IIQ	Initialize interrupt queue base pointer.
0x4	REX	Report execution (via interrupt).
0x5	SDP	Set up data pipe.
0x6	CDP	Continue data pipe (reread TD/RD pointer).
0x7	DTS	Define time slot.
0x8	SSP	Set short pipe data.
0x9	CGM	CHI global mode.
0xA	NP2	Network port 2.
0xB	NP0	Network port 0.
0xC	—	Reserved.
0xD	—	Reserved.
0xE	CDM	CHI data mode.
0xF	NP1	Network port 1.

Always set up the SDP and DTS commands for the serial interface anchor pipes **before** executing CDM and NP commands, and **before** turning on the CHI and NP bits in IP0. For example, if the CHI is to be used, DTS commands setting up CHI anchor pipe 16 must be executed by the T7903 before any CDM command is executed (no SDP commands are used for pipe 16). If the network port is to be used, the network port anchor pipes (D-channel pipes) must be set up via SDP and DTS commands before any NP0 commands are executed. This is shown below (note that the PAUSE command is used after SDP and DTS commands).

Commands (continued)

Command Set Summary (continued)

IIQ cmd
SDP cmds
DTS cmds
CGM cmd
PAUSE cmd
NP and CDM cmds
WAIT cmd

Then, execute the command list and, finally, turn on the CHI and NP bits in IP0, if these interfaces are to be used.

See the WAIT and PAUSE command descriptions for more information on the required order of commands in the command queue.

WAIT (0x0): Wait Command

The WAIT command should be placed at the end of the command queue to indicate to the T7903 that the end of the command list has been reached. Execution of this command clears the P bit in IP0. The command queue can be extended by overwriting the WAIT command and setting the P bit in IP0 or by writing the command queue pointer with the address of a new command queue. New commands can also be executed by overwriting the previous list with the new list and then rewriting the command queue pointer to point to the beginning.

Table 21. WAIT (0x0): Wait Command Description

31	30	29	28	27	26—16	15—0
0	0	0	0	I	—	Value

Field	Bit	Name/Description
Opcode	31—28	**Opcode.** Opcode = 0x0.
I	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word and the Value field (bits 15—0) is reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	26—16	**Reserved.** Program to zero.
Value	15—0	**Value.** When I = 1, the user-programmable Value field is reported in bits 15—0 of the Interrupt Information field of the interrupt word.

PAUSE (0x1): Pause Command

The PAUSE command pauses execution of the command queue, and serves the long data pipes before resuming execution of the command queue. This pause allows the ISA-MWAC to synchronize the setting up of and enabling of an interface. There are four commands used to set up the serial interfaces and to define time slots for them: SDP, SSP, CGM, and DTS commands. Since the SDP and SSP commands may be delayed in their internal execution, the PAUSE command should be used after a group of SDP, SSP, DTS, and CGM commands to allow the desired configuration to take effect within the ISA-MWAC. After the PAUSE command, set up the serial interfaces (if used) via the NP0, NP1, NP2, and CDM commands. The WAIT command should be the last command in the list. The sequence of commands is slightly different if new time slots/pipes need to be assigned after an interface is enabled. First issue the new SDP and SSP commands, then a PAUSE, and finally, the new DTS commands.

Commands (continued)

PAUSE (0x1): Pause Command (continued)

Table 22. PAUSE (0x1): Pause Command Description

31	30	29	28	27	26—16	15—0
0	0	0	1	I	—	Value

Field	Bit	Name/Description
Opcode	31—28	**Opcode.** Opcode = 0x1.
I	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word and the Value field (bits 15— 0) is reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	26—16	**Reserved.** Program to zero.
Value	15—0	**Value.** When I = 1, the user programmable Value field is reported in bits 15—0 of the Interrupt Information field of the interrupt word.

JMP (0x2): Jump Command

Upon execution of the Jump command, the T7903 reads the Pointer to New Command and starts executing commands from that point in DRAM.

Table 23. JMP (0x2): Jump Command Description

31	30	29	28	27	26—20	19—16	15—0
0	0	1	0	I	—		Value
—							Pointer to New Command

Field	Word	Bit	Name/Description
Opcode	1	31—28	**Opcode.** Opcode = 0x2.
I	1	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads the first word of this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word and the Value field (bits 15—0) is reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	1	26—16	**Reserved.** Program to zero.
Value	1	15—0	**Value.** When I = 1, the user-programmable Value field is reported in bits 15—0 of the Interrupt Information field of the interrupt word.
—	2	31—20	**Reserved.** Program to zero.
Pointer to New Command	2	19—0	**Pointer to New Command.** This is the 20-bit starting address of the new command queue in DRAM.

Commands (continued)

IIQ (0x3): Initialize Interrupt Queue Command

The IIQ command sets up a new interrupt queue base pointer. To disable interrupts (except PIO interrupts), program the Pointer to New Interrupt Queue to 0x00000 (NULL pointer).

Table 24. IIQ (0x3): Initialize Interrupt Queue Command Description

31	30	29	28	27	26—20	19—0
0	0	1	1	I	—	
—						Pointer to New Interrupt Queue

Field	Word	Bit	Name/Description
Opcode	1	31—28	**Opcode.** Opcode = 0x3.
I	1	27	**Interrupt on Command Execution.** If I = 1 and an interrupt queue has been previously set up (via an IIQ command), a CMDI interrupt is issued when the T7903 reads the first word of this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. If an interrupt queue has not previously been set up, an interrupt will not be generated when this command is read. When I = 0, no CMDI interrupt is issued.
—	1	26—0	**Reserved.** Program to zero.
—	2	31—20	**Reserved.** Program to zero.
Pointer to New Interrupt Queue	2	19—0	**Pointer to New Interrupt Queue.** This is the starting address in local DRAM of the new interrupt queue.

REX (0x4): Report Execution Command

If I = 1, a CMDI interrupt is issued upon execution of the REX command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word and the Value field (bits 15—0) is reported in bits 15—0 of the Interrupt Information field of the interrupt word. When I = 0, this command can be used as a NOP.

Table 25. REX (0x4): Report Execution Command Description

31	30	29	28	27	26—16	15—0
0	1	0	0	I	—	Value

Field	Bit	Name/Description
Opcode	31—28	**Opcode.** Opcode = 0x4.
I	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word and the Value field (bits 15—0) is reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	26—16	**Reserved.** Program to zero.
Value	15—0	**Value.** When I = 1, the user-programmable Value field is reported in bits 15—0 of the Interrupt Information field of the interrupt word.

Commands (continued)

SDP (0x5): Setup Data Pipe Command

The parameters of each data pipe used are set by using this command. Execution of this command initializes a long or short pipe.

Table 26. SDP (0x5): Setup Data Pipe Command Description

31	30	29	28	27	26—20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	I	—	IRM3—0				MODE			DIR	BOB	PTR	—	ABT	CLR	—		PIPE				
—						Pointer to TD or RD																			

Field	Word	Bit	Name/Description
Opcode	1	31—28	**Opcode.** Opcode = 0x5.
I	1	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads the first word of this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. Bits 15—0 are reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	1	26—20	**Reserved.** Program to zero.
IRM3—IRM2	1	19, 18	**Interrupt Report and Mask Bits 3 and 2.** (See the Interrupts section of this document for a more detailed description of these interrupts.) The FXDT, UNDR, DBYT, RBYT, and COLL interrupts can be enabled or masked on a pipe-by-pipe basis by using the IRM3 and IRM2 bits as shown below. See MODE field description (bits 15—13) for more information.

Interrupt	Applicable MODE	IRM3	IRM2	Description
FXDT	0x6; receive only (DIR = 0)	0	0	Disable FXDT interrupt
		0	1	Report second time in a row value is received
		1	0	Report any changes
		1	1	Report every value received
UNDR	0x0, 0x2, 0x3;	0	0	Disable UNDR interrupt
	transmit only (DIR = 1)	0	1	Enable UNDR interrupt
DBYT	0x4; transmit only (DIR = 1)	0	x	Disable DBYT interrupt
		1	x	Enable DBYT interrupt
RBYT	0x4; receive only (DIR = 0)	0	x	Disable RBYT interrupt
		1	x	Enable RBYT interrupt
COLL	0x3; transmit only (DIR = 1)	0	x	Disable COLL interrupt
		1	x	Enable COLL interrupt

IRM1	1	17	**Interrupt Report and Mask Bit 1—EOL Interrupt Enable.** Setting IRM1 = 1 enables the EOL interrupt for the pipe.
IRM0	1	16	**Interrupt Report and Mask Bit 0—IBEG and IEND Interrupt Enable.** In the HDLC mode, the ISA-MWAC monitors the receive data stream between a closing HDLC flag and an opening flag. Any transitions between flags and idle are reported via the IBEG and IEND interrupts when IRM0 = 1.

Commands (continued)

SDP (0x5): Setup Data Pipe Command (continued)

Table 26. SDP (0x5): Setup Data Pipe Command Description (continued)

Field	Word	Bit	Name/Description
MODE	1	15—13	**Mode.** The mode bits control the type of data that flows through the pipe.
			Bit 15 / Bit 14 / Bit 13 / Hex / Description
			0 / 0 / 0 / 0x0 / Transparent to/from DRAM (long pipes only)
			0 / 0 / 1 / 0x1 / Not used
			0 / 1 / 0 / 0x2 / HDLC (long pipes only)
			0 / 1 / 1 / 0x3 / HDLC D channel (priority control for TE D channel transmit pipes to NP0, 1, and 2 interfaces—pipes 1, 2, and 4 only)
			1 / 0 / 0 / 0x4 / Serial in to serial out (long and short pipes)
			1 / 0 / 1 / 0x5 / Not used
			1 / 1 / 0 / 0x6 / Fixed data (short pipes only)
			1 / 1 / 1 / 0x7 / Not used
DIR	1	12	**Direction.** This bit indicates the direction of data flow in the pipe. Programming DIR = 1 indicates that data flow is from DRAM or fixed data to a serial interface. Programming DIR = 0 indicates that data flow is from a serial interface to DRAM, from a serial interface for FXDT interrupt generation, or is serial to serial.
BOB	1	11	**Bit Order Within Byte.** If BOB = 1, MSB is transmitted first; if BOB = 0, LSB is transmitted first. This bit affects long pipes only; short pipes always transmit LSB first.
PTR	1	10	**Pointer.** Setting PTR = 1 indicates to the T7903 that word 2 of this command points to a new TD/RD descriptor which should be used following the current frame. To halt a pipe, set the PTR bit with a NULL pointer.
—	1	9	**Reserved.** Program to zero.
ABT	1	8	**Abort.** This bit applies only to HDLC/HDLC D mode transmit data (MODE = 2 or 3; DIR = 1; long pipes only). This bit is ignored for receive data pipes (DIR = 0). If ABT = 1, an HDLC abort pattern is inserted in the data FIFO. If it is set in the middle of a frame, the frame is aborted and the ABORT bit in the TD status is set to 1. If the HDLC abort pattern is placed in interframe data (FLAGS or IDLES), it simply is transmitted.
CLR	1	7	**Clear.** When CLR = 1, the pipe is cleared. Any frame or interframe data in the pipe is lost. **A pipe must be cleared whenever it is set up for the first time (long and short pipes).**
—	1	6, 5	**Reserved.** Program to zero.
PIPE	1	4—0	**Pipe Identification Number.** Use 0—15 for long pipes; 16—31 for short pipes.
—	2	31—20	**Reserved.** Program to zero.
Pointer to TD or RD	2	19—0	**Pointer to Transmit Descriptor or Receive Descriptor.** This word points to the location of the associated pipe's transmit or receive descriptor (in local DRAM). This is used for long pipes in modes 0, 2, and 3 only. The transmit and receive descriptors must be aligned on 16-byte boundaries (the least significant 4 bits of the TD/RD pointer must be 0).

Commands (continued)

CDP (0x6): Continue Data Pipe Command

The CDP command has two functions. When PA = 0, the normal CDP function is enabled. This command causes the ISA-MWAC to reread (if needed) its pointer to the next TD/RD (NDA in the descriptor). If the ISA-MWAC has encountered an end-of-list condition (null pointer in the next descriptor address or EOL bit set to 1 in TD/RD), it rereads the NDA pointer and continues. If the ISA-MWAC has not encountered an end-of-list condition, it ignores the CDP command and continues processing the TD/RD lists with no interruption. The CDP may be placed on the command queue whenever the TD/RD queue for a specific pipe is extended. CDP is only valid for long pipes (pipes 0—15).

If PA = 1, then the CDP command is used to adjust the pointer into the indicated long pipe's internal FIFO by adding the Inc_value to the current pointer. This can be used to equalize delays between data channels (see the Delay Equalization in Support of BONDING section).

Table 27. CDP (0x6): Continue Data Pipe Command Description

31	30	29	28	27	26—16	15	14—5	4	3	2	1	0
0	1	1	0	I	—	PA	Inc_value	PIPE				

Field	Bit	Name/Description
Opcode	31—28	**Opcode.** Opcode = 0x6.
I	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. Bits 15—0 are reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	26—16	**Reserved.** Program to zero.
PA	15	**Pointer Adjust.** This bit selects either normal mode or pointer adjust mode for the CDP command. When PA = 0, the T7903 ignores the Inc_value and the CDP command operates normally. When PA = 1, the normal CDP function is bypassed and the T7903 uses the 10-bit Inc_value as an offset to its internal input FIFO pointer for the designated pipe. Modifying this pointer adjusts the incoming phase of data coming into the long pipe.
Inc_value	14—5	**Increment Value.** When PA = 1, Inc_value is used as an offset to the input pointer of the associated pipe's FIFO. See the Delay Equalization in Support of BONDING section. When PA = 0, Inc_value is ignored.
PIPE	4—0	**Pipe.** Pipe number.

Commands (continued)

DTS (0x7): Define Time-Slot Command

Any data pipe connecting to any of the serial interfaces (CHI, NP0, NP1, or NP2) must have a time slot assigned to it, defined by the DTS command. The first word of the command defines general features of the time slot such as whether it is an input or an output time slot, its pipe, and its connectivity (see the Internal Data Routing section for more information on connectivity). The second and third words of the DTS command hold the time-slot descriptors and more pipe connectivity information. The second word is used by the T7903 if the time slot is an input to a pipe (VI = 1), and the third word is used if the time slot is an output to a pipe (VO = 1). The time-slot descriptor gives specific information such as starting cycle, length, and mode. These descriptors are detailed in Table 29 (for network port time slots) and Table 31 (for CHI time slots). **Caution: TC, bit 20 of the DTS command, must be set to 1.**

Table 28. DTS (0x7): Define Time-Slot Command Description

31	30	29	28	27	26—21	20	19	18	17	16	15	14	13	12	11	10	9—5	4	3	2	1	0
0	1	1	1	I	—	TC	—		VI	VO	I/D	Prev. In PIPE					Prev. Out PIPE	PIPE				
Input TSD																	Aux. In PIPE	Next In PIPE				
Output TSD																	Aux. Out PIPE	Next Out PIPE				

Field	Word	Bit	Name/Description
Opcode	1	31—28	**Opcode.** Opcode = 0x7.
I	1	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads the first word of this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. Bits 15—0 are reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	1	26—21	**Reserved.** Program to zero.
TC	1	20	**TC—Reserved.** This bit **must** be set to 1.
—	1	19, 18	**Reserved.** Program to zero.
VI*	1	17	**Valid Input Time-Slot Descriptor.** Setting VI = 1 indicates that this DTS command describes the input time slot to a data pipe (data received at a serial interface).
VO*	1	16	**Valid Output Time-Slot Descriptor.** Setting VO = 1 indicates that this DTS command describes the output time slot of a data pipe (data output at a serial interface).
I/D	1	15	**Insert/Delete.** When I/D = 0, the T7903 will delete this time slot from linked list. When deleting a time slot, only the first 4 bytes of the DTS command are used by the ISA-MWAC (the Next Pipe, Aux Pipe, and TSD fields are ignored). The ISA-MWAC automatically maintains linked list connectivity between the remaining pipes when deleting time slots. When I/D = 1, the T7903 will add/modify this time slot to the linked list.
Prev. In PIPE	1	14—10	**Previous In Pipe.** This field is only used if VI = 1 (the time slot is an input to a serial interface). This field identifies the pipe preceding this pipe in the input list.
Prev. Out PIPE	1	9—5	**Previous Out Pipe.** This field is only used if VO = 0 (the time slot is an output at a serial interface). This field identifies the pipe preceding this pipe in the output list.
PIPE	1	4—0	**Pipe.** Pipe number for these descriptors.

* For programming simplicity, a serial-to-serial data pipe can have its input and output time slots defined by using one DTS command (both VI and VO set to 1) or by using the two DTS commands. Serial-to-DRAM or DRAM-to-serial data pipes can have only one direction defined per DTS command.

Commands (continued)

DTS (0x7): Define Time-Slot Command (continued)

Table 28. DTS (0x7): Define Time-Slot Command Description (continued)

Field	Word	Bit	Name/Description
Input TSD	2	31—10	**Input Time-Slot Descriptor.** This field is only used if VI = 1 (the time slot is an input to a serial interface). The Input TSD describes the time slot's mode, length, and location in the serial stream. **See Time-Slot Descriptor: Network Port Time Slots section below.**
Aux. In PIPE	2	9—5	**Auxiliary Input Pipe Identifier.** This field is only used if VI = 1 (the time slot is an input to a serial interface).Valid only for noncontiguous time-slot mode (see noncontiguous mode description below).
Next In PIPE	2	4—0	**Next Input TSD/Data Pipe.** This field is only used if VI = 1 (the time slot is an input to a serial interface). This field identifies the next pipe in the input list.
Output TSD	3	31—10	**Output Time-Slot Descriptor.** This field is only used if VO = 1 (the time slot is an output at a serial interface). The Output TSD describes the time slot's mode, length, and location in the serial stream. **See Time-Slot Descriptor: Network Port Time Slots section below.**
Aux. Out PIPE	3	9—5	**Auxiliary Output Pipe Identifier.** This field is only used if VO = 1 (the time slot is an output at a serial interface). Valid only for noncontiguous time-slot mode (see noncontiguous mode description below).
Next Out PIPE	3	4—0	**Next Output TSD/Data Pipe.** This field is only used if VO = 1 (the time slot is an output at a serial interface). This field identifies the next pipe in the output list.

Time-Slot Descriptors (TSD): Network Port Time Slots

Table 29 describes the Input and Output Time-Slot Descriptor fields for the NP0, NP1, and NP2 interfaces.

Table 29. Network Port (NP0, NP1, or NP2) Input/Output Time-Slot Descriptor (TSD)

Field	Bit	Name/Description
LEN	31—24	**Length.** Number of bits in the time slot.
CYCLE	23—14	**Cycle.** Bit count at start of the time slot.
DI	13	**Data Invert.** When DI = 1, all data is inverted. When DI = 0, data is not inverted.
—	12	**Reserved.** Program to 0.
TSMODE	11—10	**Time-Slot Mode.** TSMODE = 00: Normal operation (single time slot per pipe). TSMODE = 01: Reserved. TSMODE = 10: Reserved. TSMODE = 11: Noncontiguous mode (multiple time slots per pipe).

The BRI interfaces are viewed as 19-bit long serial interfaces. The B1, B2, D, S, and Q channels have predetermined cycle and length values which must be used in the input and output TSD fields. These are shown in Table 30. Synchronous serial mode channels are also shown.

Commands (continued)

DTS (0x7): Define Time-Slot Command (continued)

Time-Slot Descriptors (TSD): Network Port Time Slots (continued)

Table 30. Predetermined Cycle and Length Values for the Network Port Interfaces

Channel	CYCLE	LEN
B1	0	8
B2	8	8
S/Q	16	1
D	17	2
B1 and B2 Channels Concatenated (128 kbits/s channel)	0	16
Synchronous—56 kbits/s	0	7
Synchronous—64 kbits/s	0	8
Synchronous—128 kbits/s	0	16

Time-Slot Descriptors (TSD): CHI Time Slots

Table 31 describes the Input TSD and Output TSD fields when using the CHI.

Table 31. CHI Input/Output Time-Slot Descriptor (TSD)

Field	Bit	Name/Description
LEN	31—24	**Length.** Number of bits in the time slot. This field is ignored for the CHI anchor mode.
CYCLE	23—14	**Cycle.** CHICKIN/CHICKOUT count at start of the time slot. This field is ignored for the CHI anchor mode.
DI	13	**Data Invert.** When DI = 1, all data is inverted. When DI = 0, data is not inverted. This field is ignored for the CHI anchor mode.
TSMODE	12—10	**Time-Slot Mode.** TSMODE = 000: Single channel (normal operation). TSMODE = 001: Reserved. TSMODE = 010: Reserved. TSMODE = 011: Noncontiguous mode. TSMODE = 100: Reserved. TSMODE = 101: Reserved. TSMODE = 110: Reserved. TSMODE = 111: Anchor mode. This mode is used only when defining the CHI anchor pipe. In this case, LENGTH, CYCLE, and DI are ignored.

Commands (continued)

DTS (0x7): Define Time-Slot Command (continued)

Linked List Management

Time-slot descriptors (TSD) form eight circular linked lists internal to the ISA-MWAC, one in each direction for the concentration highway and the three network port interfaces. When a new time slot is deleted, added, or modified, the DTS command must always have a valid pointer to the preceding time slot so the linked list can be maintained.

Note: Time slots **must** be assigned in the order they occur on the CHI. Time slots on BRI-configured network ports must be defined starting with the D channel. Subsequent time slots must be defined in the order that they occur (i.e., B1, B2, S/Q).

The time-slot descriptor must also always have a valid pointer to the next time-slot descriptor (or to itself if it is the only time slot defined for that serial interface). This is done with the Next In PIPE and Next Out PIPE fields. For data pipes that are not serial-to-serial, one time-slot descriptor is used. The user must indicate which time-slot descriptors are valid by setting bit 17, the valid input time-slot descriptor bit (VI), and/or bit 16, the valid output time-slot descriptor bit (VO). Whenever a time slot is defined, it **must** be assigned to a data pipe.

The input/output time-slot descriptors are ignored when time slots are deleted, although the VI/VO bits need to be set indicating if the time slot to be deleted is an outgoing (VO = 1) or incoming (VI = 1) time slot.

See the Linked Lists and Anchor Pipes section for more information.

Anchor Pipes

Whenever the concentration highway is used, short pipe #16 (CHI anchor pipe) **must** be used to start both transmit and receive linked lists for the CHI interface and, thus, cannot be assigned to a time slot. The time-slot mode must be set to 7, CHI anchor mode. The first CHI TSD must use the CHI anchor mode to establish an anchor pipe from which all other time slots are linked.

Whenever the network port interfaces are used in the BRI mode, the D channel **must** be set up first with the following requirements:

The NP0 receive time-slot list starts with pipe 0.
The NP0 transmit time-slot list starts with pipe 1.
The NP1 receive time-slot list starts with pipe 5.
The NP1 transmit time-slot list starts with pipe 4.
The NP2 receive time-slot list starts with pipe 3.
The NP2 transmit time-slot list starts with pipe 2.

It is not recommended that the D channel be passed directly between the TE and NT interfaces. See the Linked Lists and Anchor Pipes section for more information.

Noncontiguous Mode

If multiple time slots need to be assigned to the same pipe (noncontiguous mode), the following procedure should be used to set up the data pipe and define the time slots.

1. Set up appropriate data pipes via SDP commands.
2. Define the first time slot as if it were the only time slot assigned to that pipe (mode = 0).
3. Define the following time slot as if it were the only time slot assigned to another pipe (this pipe is a sacrificial long or short pipe). Set the mode to noncontiguous mode (TSMODE = 11), and place the pipe you want to associate with this time slot in the auxiliary input/output pipe identifier.

Note: Attributes from the original SDP command apply to all time-slot segments.

Commands (continued)

SSP (0x8): Set Short Pipe Data Command

When a short pipe is sending fixed data to a serial interface, the SSP command is used to set or change the data being sent. This is useful for the Q channel on a TE interface and the S channel on an NT interface. If bit 4 is not set (indicating a long pipe has been selected—pipes 16—31), the command is ignored. PIPE must be an outgoing pipe (DIR = 1 in SDP command). When fixed data is assigned an outgoing time slot, the number of bits used from the data field is the number of bits programmed in the LEN field of the DTS command. The only two exceptions are the BRI S and Q time slots. The BRI S channel uses the least significant 20 bits. The BRI Q channel uses the least significant 5 bits.

Note: Data should be adjusted low order first.

Table 32. SSP (0x8): Set Short Pipe Data Command Description

31	30	29	28	27	26—5	4	3	2	1	0
1	0	0	0	I	—	PIPE				
Data										

Field	Word	Bit	Name/Description
Opcode	1	31—28	**Opcode.** Opcode = 0x8.
I	1	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads the first word of this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. Bits 15—0 are reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	1	26—5	**Reserved.** Program to zero.
PIPE	1	4—0	**Pipe.** Pipe number for these descriptors. Short pipes only.
Data	2	31—0	**Data.** This is the fixed data to be transmitted out the short pipe.

Commands (continued)

CGM (0x9): CHI Global Mode Command

The CGM command establishes CHI master or slave mode and determines the CHICKOUT clock rate in master mode. It also defines CHIFS frame sync clocking, and certain global drive and report conditions. The BPF (bits per frame) field in the CGM command results in BPF + 1 CHICKOUT cycles per frame when CHI master mode is used.

Table 33. CGM (0x9): CHI Global Mode Command Description

31	30	29	28	27	26	25	24	23—16	15	14	13	12	11	10—0
1	0	0	1	I	FSI	STECK	SSYNC	CHICM	IRM1—0		OD	FE	FD	BPF

Field	Bit	Name/Description
Opcode	31—28	**Opcode.** Opcode = 0x9.
I	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads the first word of this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. Bits 15—0 are reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
FSI	26	**Frame Strobe Invert.** FSI is valid for CHI master mode only (CHICM ≥ 3). When FSI = 0, the beginning of the CHI frame is indicated by a high-going pulse on CHIFS. When FSI = 1, the beginning of the CHI frame is indicated by a low-going pulse on CHIFS (normal mode of *MVIP* frame strobe).
STECK	25	**Select TECK as Input or Output.** This bit configures the TECK pin as an input or output. When STECK = 0, TECK is an input (it must be 8 kHz). If SSYNC (bit 24) is set to 1, the CHI (master only) and network ports (NT and serial master only) will synchronize to the signal on TECK. If STECK = 0 but SSYNC = 0, TECK will be an input but will not be used by the chip for synchronization (TECK is ignored by the chip). When STECK = 1, TECK is a 4 kHz output that is synchronized to the first TE-configured port or synchronous serial slave port to activate. SSYNC is ignored. If no TE or synchronous slave ports are active, TECK will free-run.
SSYNC	24	**Select Synchronization to CHI or TECK.** This bit is only used if STECK = 0 (it is ignored when STECK = 1). When SSYNC = 1, the chip will synchronize to an 8 kHz signal supplied to the TECK input pin. When SSYNC = 0, the chip will synchronize to the CHI (if the CHI is in slave mode) or the first TE or synchronous slave port to become active.
CHICM	23—16	**CHI Clock Mode.** The CHICM field selects CHI master or slave mode and sets CHIFS rate. CHICM = 0: CHI slave mode (CHICKIN is the clock input and CHIFS is the frame strobe input). CHIFS must be 8 kHz. CHICM = 1: CHI slave mode (CHICKIN is the clock input and CHIFS is the frame strobe input). CHIFS can range from 8 kHz to 50 kHz. CHICM ≥ 3: CHI master mode (CHICKOUT is the clock output and CHIFS is the frame strobe output). CHICK rate is 12.288 MHz divided by CHICM. CHIFS is 8 kHz.

Commands (continued)

CGM (0x9): CHI Global Mode Command (continued)

Table 33. CGM (0x9): CHI Global Mode Command Description (continued)

Field	Bit	Name/Description
IRM1	15	**Interrupt Report and Mask Bit 1.** If IRM0 = 1 and IRM1 = 1, an immediate CHIL interrupt is generated. This is used to give an immediate report of the CHI status.
IRM0	14	**Interrupt Report and Mask Bit 2.** If IRM0 = 1, the CHIL interrupt is enabled.
OD	13	**Open-Drain Enable.** The OD bit selects the type of output drive on the CHI transmitter pin CHIDX. When OD = 0, an active pull-up is enabled on CHIDX. When OD = 1, CHIDX uses an open-drain driver (no active pull-up).
FE	12	**Frame Edge.** This bit selects the CHICKIN/CHICKOUT edge used to sample CHIFS. When FE = 0, CHIFS is sampled on the falling edge of CHICKIN (slave mode) or CHICKOUT (master mode). When FE = 1, CHIFS is sampled on the rising edge of CHICKIN (slave mode) or CHICKOUT (master mode).
FD	11	**Frame Drive.** This bit selects the CHICKOUT edge used to drive CHIFS (CHI master mode). This bit is ignored for CHI slave mode. When FD = 0, CHIFS is driven on the falling edge of CHICKOUT. When FD = 1, CHIFS is driven on the rising edge of CHICKOUT.
BPF	10—0	**Bits Per Frame.** When the CHI is in master mode (CHICM ≥ 3), CHICKOUT outputs BPF + 1 pulses per 125 µs frame. If BPF is programmed to 0, CHICKOUT will output clock pulses continuously. If BPF is not 0, it must be programmed to a value that is at least one greater than the total number of bits being output in the time slots on CHI. If BPF + 1 defines fewer cycles than can actually occur in 125 µs (given the CHICKOUT rate defined by CHICM), then CHICKOUT outputs BPF + 1 cycles and then remains low until the next frame. BPF does not force a frame to be longer than 125 µs. When the CHI is in slave mode (CHICM = 0 or 1), the BPF field is ignored.

NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands

These commands configure the network ports. The control bits are defined as follows.

Table 34. NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands Description

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17—0
Opcode				I	—			Control Bits				—		Control Bits

Field	Bit	Name/Description
Opcode	31—28	**Opcode.** Opcode = 0xB for NP0, 0xF for NP1, and 0xA for NP2.
I	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads the first word of this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. Bits 15—0 are reported in bits 15—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	26—24	**Reserved.** Program to 0.

Commands (continued)

NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands (continued)

Table 34. NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands Description (continued)

Field	Bit	Name/Description
NPMODE	23	**Network Port Mode.** This bit selects the network port mode. If NPMODE = 1, synchronous serial mode is selected. **LEVEL (bit 22) must be programmed to 1 when NPMODE = 1.** When NPMODE = 0, BRI mode is selected. **TLEVEL and RLEVEL (bits 20 and 22) must be programmed to 0 when NPMODE = 0.**
RLEVEL	22	**Receive Levels.** This bit determines the type of signals used by the network port receiver. If RLEVEL = 1, digital levels are used. This is required for synchronous serial mode (NPMODE = 1). If RLEVEL = 0, analog levels are used, as required for BRI mode (NPMODE = 0). **RLEVEL and TLEVEL (bits 22 and 20) must be programmed to the same value.**
EZOBS	21	**Enhanced Zero-to-One Backswing Suppression.** When in BRI mode (NPMODE = 0), this bit enables enhanced backswing suppression on the transmit pins of the network port. If EZOBS = 1, enhanced backswing suppression is enabled for binary 0 to binary 1 transitions. If EZOBS = 0, this feature is disabled. This pin is ignored when synchronous serial mode is enabled (NPMODE = 1). **Recommendation:** It is recommended that EZOBS be programmed to 0 when the port is used in BRI mode.
TLEVEL	20	**Transmit Levels.** This bit determines the type of signals used by the network port transmitter. If TLEVEL = 1, digital levels are used. This is required for synchronous serial mode (NPMODE = 1). If TLEVEL = 0, analog levels are used, as required for BRI mode (NPMODE = 0). **TLEVEL and RLEVEL (bits 20 and 22) must be programmed to the same value.**
—	19, 18	**Reserved.** Program to 0.
FBIT/ SCKM1	17	**Frame Bit.** When in BRI mode (NPMODE = 0), this bit selects the type of BRI framing bit that is accepted as good by the T7903. When FBIT = 1, the chip will accept a frame beginning with an F bit that is not a bipolar violation after an errored frame. When FBIT = 0, this type of frame will not be considered good. **Recommendation:** It is recommended that FBIT be programmed to 1 when the port is used in BRI mode. **Synchronous Clock Mode Bit 1.** When in synchronous serial mode (NPMODE = 1), SCKM0 and SCKM1 are used to select the synchronous serial clock mode (see the Synchronous Serial Modes section). **SCKM1 / SCKM0 / Clock Modes** 0 / 0 / Slave mode, standard timing. 0 / 1 / Slave mode, terminal timing. 1 / 0 / Reserved. 1 / 1 / Master mode. STx should be connected to RTx.
NBF/ SCKM0	16	**Number of Bad Frames to Lose Framing.** When in BRI mode (NPMODE = 0), this bit selects the number of bad frames required to lose framing. If NBF = 0, three bad frames must be received to lose framing. If NBF = 1, two bad frames must be received to lose framing. Note that three good frames are always required to regain framing. **Recommendation:** It is recommended that NBF be programmed to 0 when the port is used in BRI mode. **Synchronous Clock Mode Bit 1.** See bit description for SCKM1 above.
IRM1	15	**Interrupt Report and Mask for Network Port—Bit 1.** This bit functions only for BRI mode (NPMODE = 0). When IRM1 = 1, an immediate report of the BRI status is forced (regardless of the value of IRM0) upon execution of this command. See the SBRI: Status of BRI Changed Interrupt section in the Interrupt Description section. When IRM1 = 0, the SBRI interrupt is not forced.

Commands (continued)

NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands (continued)

Table 34. NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands Description (continued)

Field	Bit	Name/Description
IRM0	14	**Interrupt Report and Mask for Network Port—Bit 0.** This bit functions only for BRI mode (NPMODE = 0). When IRM0 = 1, the SBRI interrupt is enabled. When IRM0 = 0, the SBRI interrupt is disabled.
ISNT	13	**ISDN NT Interface.** This bit is used to select either TE or NT mode for a BRI network port (NPMODE = 0). If ISNT = 1, the network port is configured as an NT. If ISNT = 0, the network port is a TE. **Caution: When NPMODE = 1 (synchronous serial mode is selected), ISNT must be programmed to 0.**
FT/SRM1	12	**Fixed Timing.** When in BRI mode (NPMODE = 0) and the network port is configured as an NT (ISNT = 1), this bit selects the type of timing used by the BRI receiver. When FT = 1 (fixed timing), the incoming data is sampled at a fixed delay (synchronous) from the transmitter. If FT = 0, the incoming data is sampled by an adaptive timing mechanism. **Caution: When in BRI mode (NPMODE = 0) and the network port is configured as a TE (ISNT = 0), FT must be programmed to 0 for proper operation.** **Synchronous Rate Mode Bit 1.** When in synchronous serial mode (NPMODE = 1), SRM1 and SRM0 select the data rate. **SRM1 / SRM0 / Selection** 0 / 0 / 56 kbits/s 0 / 1 / 64 kbits/s 1 / 0 / 128 kbits/s 1 / 1 / Reserved
EZ/ SRM0	11	**Echo Channel All Zeros.** When in BRI mode (NPMODE = 0) and the network port is configured as an NT (ISNT = 1), this bit defines the echo channel operation. When EZ = 1, the echo channel sends all zeros. When EZ = 0, the echo channel echoes the received D-channel bits. When in BRI mode and the network port is configured as a TE, EZ should be programmed to 0 for normal operation. When operating in D-channel local loopback, program EZ to 1, if force activating the network port (FACT = 1, bit 1). **Synchronous Rate Mode Bit 0.** When in synchronous serial mode (NPMODE = 1), SRM1 and SRM0 select the data rate (see FT/SRM1 bit).
IFA	10	**Inhibit Final Activation.** When in BRI mode (NPMODE = 0), this bit provides a means to keep the network port from fully activating. When the port is an NT (ISNT = 1), IFA = 1 will keep the A bit in the transmitted ISDN frames set to 0 (INFO 2). When the port is a TE, IFA = 1 will prevent data from being transmitted in the B1, B2, and D channels (2B+D operational data will not pass through the device for transmission out the network port). When in synchronous serial mode (NPMODE = 1), this bit should be cleared to 0.

Commands (continued)

NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands (continued)

Table 34. NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands Description (continued)

Field	Bit	Name/Description
ACT	9	**Activate Interface.** When in BRI mode (NPMODE = 0), this bit is used in conjunction with the NP0, NP1, and NP2 bits in IP0. If the NPx bit in IP0 is programmed to 1, then the network port will respond to a request to activate but does not initiate activation of its interface until ACT is set to 1. The ACT bit is ignored until the NPx bit is set. If NPx = 1 and ACT = 1, then the network port will initiate activation (transmit INFO 1 if its a TE or INFO 2 if its an NT). When in synchronous serial mode (NPMODE = 1), this bit should be cleared to 0.
MFE	8	**Multiframe (S and Q Channels) Enable.** When in BRI mode (NPMODE = 0), this bit enables/disables multiframing. When the port is an NT (ISNT = 1) and MFE = 1, S channel transmission is enabled. When the port is a TE (ISNT = 0) and MFE = 1, Q channel transmission is enabled (note that the TE must also detect multiframing before it activates Q). When MFE = 0, multiframing is disabled. When in synchronous serial mode (NPMODE = 1), this bit should be cleared to 0.
RLB_D	7	**Remote Loopback for D.** See Loopbacks section.
RLB_B1	6	**Remote Loopback for B1.** See Loopbacks section.
RLB_B2	5	**Remote Loopback for B2.** See Loopbacks section.
LLB_D	4	**Local Loopback for D.** See Loopbacks section.
LLB_B1	3	**Local Loopback for B1.** See Loopbacks section.
LLB_B2	2	**Local Loopback for B2.** See Loopbacks section.
FACT	1	**Force Activation.** When in BRI mode (NPMODE = 0), this bit allows the network port to fully activate without regard to received INFO states. When FACT = 1 and NPx = 1 (in IP0), the port will transmit INFO 3 if it is a TE or INFO 4 if it is an NT. This allows local loopback and other tests of the interface without requiring framing from the other end of the line. **Caution: When NPMODE = 1 (synchronous serial mode is selected), FACT must be programmed to 1.**
ABVI	0	**Additional Bipolar Violation Illegal.** When in BRI mode (NPMODE = 0), this bit allows additional bipolar violations (BPVs) to be recognized as illegal. When ABVI = 0 (strict ITU-T mode), extra BPVs are allowed; they do not cause loss of frame synchronization. When ABVI = 1, extra BPVs are treated the same as missing BPVs for loss and recovery of frame synchronization. In either case, extra BPVs are reported in SBRI interrupts, if enabled (BRI only). **Recommendation:** It is recommended that ABVI be programmed to 1 when the port is used in BRI mode. When in synchronous serial mode (NPMODE = 1), this bit is ignored.

Loopbacks—General information: When using remote loopback on B1, B2, or synchronous channels, data pipes connecting to these channels must be deleted (see DTS command) before the loopback will take effect. This is not necessary for D-channel remote loopback.

Loopbacks—BRI mode: A BRI network port can be configured in several kinds of loopback modes. The programmer can configure either the D, B1, or B2 channel (or any combination) in remote loopback (RLB) or local loopback (LLB) mode by programming the corresponding bit (bits 2—7) to a 1. B-channel remote loopback puts data received at the network port's B channels back on the port's transmitter with one frame of delay, while D-channel remote loopback has only a half-frame delay. The data on the receiver can be buffered in a receive pipe (transparent loopback). Local loopback mode internally routes data destined for the network port transmitter into the receive data pipe, ignoring what is on the receiver (nontransparent local loopback).

Note: Enabling LLB or RLB mode does not cause the network port interface to initiate activation with the network.

Commands (continued)

NP0 (0xB), NP1 (0xF), and NP2 (0xA): Network Port Commands (continued)

Loopbacks—Synchronous Serial Mode: The bits necessary to enable loopbacks for a synchronous serial port are determined by the data rate of the interface, as shown below.

- Remote loopback at 56 or 64 kbits/s data rate: RLB_D = 0, RLB_B1 = 1, and RLB_B2 = 0.
- Remote loopback at 128 kbits/s data rate: RLB_D = 0, RLB_B1 = 1, and RLB_B2 = 1.
- Local loopback at 56 or 64 kbits/s data rate: LLB_D = 0, LLB_B1 = 1, and LLB_B2 = 0.
- Local loopback at 128 kbits/s data rate: LLB_D = 0, LLB_B1 = 1, and LLB_B2 = 1.

Operation Notes

At reset, the network ports come up in BRI mode. When programming a port for synchronous serial mode, the internal transition out of BRI mode can cause unpredictable data transmission or reception during the first time slot. To prevent this, set up the network port's anchor pipes before issuing the NP command to force activate (FACT = 1) the port.

After enabling a BRI-configured network port and subsequently disabling it, line state changes on the receiver can generate an SBRI interrupt even though the interface is disabled (the corresponding NP bit in IP0 is cleared to 0). To prevent this occurrence, first issue an NP command to deactivate the port and to disable its interrupts, and then clear the NP bit in IP0.

CDM (0xE): CHI Data Mode Command

This command sets up important CHI clock and frame strobe parameters. For more information on double clocking modes and *MVIP* compatibility, see Appendix D.

Table 35. CDM (0xE): CHI Data Mode Description

31	30	29	28	27	26—8	7—0
1	1	1	0	I	—	Control Bits

Field	Bit	Name/Description
Opcode	31—28	**Opcode.** Opcode = 0xE.
I	27	**Interrupt on Command Execution.** If I = 1, a CMDI interrupt is issued when the T7903 reads the first word of this command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. Bits 7—0 are reported in bits 7—0 of the Interrupt Information field of the interrupt word. This can be used for diagnostic purposes. When I = 0, no CMDI interrupt is issued.
—	26—8	**Reserved.** Program to 0.
RPIN	7	**Receive Pin.** This bit determines the pin used to receive data on the CHI. When RPIN = 0, data is received on CHIDR. This is normal operation. When RPIN = 1, data is received on CHIDX. This is used for CHI local loopbacks.
RCE	6	**Receive Clock Edge.** This bit determines the clock edge used to receive data on the CHI. When RCE = 0, data is received on the falling edge of CHICKIN/CHICKOUT. When RCE = 1, data is received on the rising edge of CHICKIN/CHICKOUT.
CMSR	5	**Clock Mode Select—Receiver.** This bit selects single- or double-clock mode for the receiver. When CMSR = 0, the CHI receiver operates in single-clock mode. One data bit is received per CHICKIN/CHICKOUT period. When CMSR = 1, the CHI receiver operates in double-clock mode. One data bit is received every two CHICKIN/CHICKOUT periods. This is used for *MVIP* and GCI compatible buses. See Appendix D.
—	4	**Reserved.** Program to 0.

Commands (continued)

CDM (0xE): CHI Data Mode Command (continued)

Table 35. CDM (0xE): Set CHI Data Mode Description (continued)

Field	Bit	Name/Description
CMST	3	**Clock Mode Select—Transmitter.** This bit selects single- or double-clock mode for the transmitter. When CMST = 0, the CHI transmitter operates in single-clock mode. One data bit is transmitted per CHICKIN/CHICKOUT period. When CMST = 1, the CHI transmitter operates in double-clock mode. One data bit is transmitted every two CHICKIN/CHICKOUT periods. This is used for *MVIP* and GCI compatible buses (see Appendix D).
XCE	2	**Transmit Clock Edge.** This bit determines the clock edge used to transmit data on the CHI. When XCE = 0, data is transmitted on the falling edge of CHICKIN/CHICKOUT. When XCE = 1, data is transmitted on the rising edge of CHICKIN/CHICKOUT.
XEN	1	**Transmit Highway Enable.** This bit is used to enable the CHI transmitter. When XEN = 0, the ISA-MWAC 3-states CHIDX. Reset forces XEN to 0. When XEN = 1, the CHI transmitter is enabled.
REN	0	**Receive Highway Enable.** This bit is used to enable the CHI receiver. When REN = 0, the CHI receiver is disabled. When REN = 1, the receiver is enabled.

Interrupts

The ISA-MWAC writes interrupt words into an interrupt queue in DRAM to provide information and status for a variety of events. Each interrupt word contains the channel number, interrupt code, and interrupt information field. Table 36 shows the bit assignments for the interrupt word. The ISA-MWAC sets the IIND bits to 10, writes the channel number, the interrupt code, and the interrupt field, and then generates an interrupt.

Interrupt Setup

The Initialize Interrupt Queue (IIQ) command contains a 20-bit pointer to the beginning of the interrupt queue in local DRAM. Interrupts are globally enabled by an IIQ command with a valid pointer. Interrupts are globally disabled by an IIQ command with a null pointer. Each interrupt queue segment consists of sixty-four 32-bit words (256 bytes): the first word (four bytes) contains a pointer to the next interrupt queue segment, and the remaining 63 words represent interrupts. Every interrupt can also be masked by clearing the appropriate interrupt control bits associated with the command or transmit and receive descriptors.

When an interrupt condition occurs, one or more words are written to the interrupt queue and the selected IRQ signal is raised. Reading register IP3 clears the interrupt signal. A recommended housekeeping procedure is for the host to write 0x00000000 to the location of the current interrupt word for interrupt queue maintenance after it services the interrupt. When the interrupt queue is full, the ISA-MWAC reads the pointer to the next interrupt queue and continues recording interrupts. This gives the host flexibility in making the interrupt queue arbitrarily long (in 63-word segments). The host must always provide a valid pointer in each interrupt queue. The ISA-MWAC never reads the contents of the interrupt queue. It only reads the pointer to the next interrupt queue segment. Therefore, the host must ensure that the queue does not overflow if it is circular.

When interrupts are globally disabled (no IIQ command executed or IIQ null pointer was executed) but individual interrupts are enabled, interrupt conditions will cause interrupt words to be stored in an internal 32-word queue. Execution of an IIQ command with a valid pointer will cause the stored interrupt words to be dumped to the newly initialized queue. If more than 32 words were generated before the IIQ command, a LINT interrupt is flagged. The LINT interrupt word will be the first word written to the new queue. Note that the following interrupts will be lost if no IIQ command has been executed: EOL, CMDI, IBEG, IEND, MINT, RBRDY, and UNDR.

Interrupts (continued)

Interrupt Setup (continued)

Operational Note: Because the ISA-MWAC uses 4-byte write buffering, host initiated writes to DRAM can be delayed. In the case of writing zeros to the interrupt queue for maintenance, this delay could cause new interrupt words to be corrupted. Therefore, it is recommended that the DRAM address pointer be touched (written) immediately after writing to a location in the interrupt queue.

Table 36. Bit Assignments for Interrupt Word

31	30	29	28	27	26	25	24	23	22	21	20	19—0
IIND		Channel						Int Code				Interrupt Information

Field	Bit	Name/Description
IIND	31, 30	**Interrupt Indicators.** These bits are set to 10 by ISA-MWAC when the interrupt word is written to the interrupt queue (indicating that the word is a new addition to the queue). The IIND bits serve no other function. As a housekeeping procedure, it is recommended that the entire interrupt word be cleared to all zeros by the host processor after the interrupt is serviced.
Channel	29—24	**Channel.** These bits describe the source of the interrupt (the ISA-MWAC channel number on which the interrupt occurred). The sources and their associated channel numbers are as follows: ■ Channels 0 to 31 are the data pipes. ■ Channel 32 is the NP0 status. ■ Channel 33 is the NP1 status. ■ Channel 34 is the NP2 status. ■ Channel 35 is not used. ■ Channel 36 is the CHI status. ■ Channel 37 is not used. ■ Channel 38 is the command and interrupt status (CMDI and LINT interrupts).
Int Code	23—20	**Interrupt Code.** This field identifies the interrupt that caused the report. **Int Code / Interrupt / Description** 0x1 RBRDY Receive buffer ready for processing 0x2 MINT Marked interrupt in RD/TD 0x3 IBEG Flag-to-idle transition detected (HDLC mode only) 0x4 IEND Idle-to-flag transition detected (HDLC mode only) 0x5 EOL End of list 0x6 CMDI Command has been read 0x7 Not used 0x8 TFC Transmission of frame complete 0x9 SBRI Status of BRI changed 0xA FXDT Fixed data change 0xB CHIL CHI lost frame sync—channel 36 (CHI) only 0xB COLL Unrecoverable D-channel collision—channels 1, 2, or 4 (D-channel transmit pipes) only 0xC DBYT Dropped byte frame slip 0xD RBYT Repeated byte frame slip 0xE LINT Lost interrupt 0xF UNDR DMA underrun
Interrupt Information	19—0	**Interrupt Information.** Used to report a longer piece of data such as the Value field for CMDI interrupts or S-channel data.

Interrupts (continued)

Interrupt Description

RBRDY (0x1): Receive Buffer Ready Interrupt

This interrupt applies to receive buffer operations. It indicates that the ISA-MWAC has closed a receive buffer due to an end-of-frame condition. For HDLC mode data, an EOF condition is caused by the receipt of a closing flag or an abort pattern. For transparent mode data, an EOF condition occurs when a buffer is full. This interrupt is masked by clearing the RBRDYEN bit in the receive descriptor (see the Memory Structure section of this document).

The channel numbers are from channel 0—15 (the long pipes); the Interrupt Information field contains the bits of the receive descriptor address in DRAM (20 bits).

MINT (0x2): Marker Interrupt

This interrupt is issued as soon as the TD/RD is read. This allows interrupts, which are not HDLC frame synchronous, to facilitate list management. The MINT interrupt is maskable by clearing the MIEN bit to 0 in the TD/RD.

The channel numbers are from channel 0—15; the Interrupt Information field contains the TD/RD address.

IBEG (0x3): Idles Began (Flag-to-Idle Transition Detected) Interrupt

The IBEG interrupt is issued when a flag-to-idle transition has been detected by the receiver (HDLC mode only). It is masked by IRM0 (bit 16) of an SDP command. This interrupt could be used to start the T3 idle timer for LAPB.

The channel numbers are from channel 0—15; it has no Interrupt Information field.

IEND (0x4): Idles Ended (Idle-to-Flag Transition Detected) Interrupt

The IEND interrupt is issued when an idle-to-flag transition has been detected by the receiver (HDLC mode only). It is masked by IRM0 (bit 16) of an SDP command. This interrupt could be used to stop the T3 idle timer for LAPB.

The channel numbers are from channel 0—15; it has no Interrupt Information field.

EOL (0x5): End-of-List Interrupt

This interrupt indicates that the ISA-MWAC has encountered either:

- A null pointer to the next transmit or receive descriptor (next descriptor address—NDA).
- A transmit/receive descriptor with EOL = 1 (bit 29).

In the case of a null NDA pointer, the current buffer is transmitted/filled and then the EOL interrupt is issued. In the case of EOL = 1, the EOL interrupt is issued but the current buffer is not transmitted/filled.

The transmitter repeats the last byte(s) and rereads NDA upon execution of the subsequent CDP or SDP command. The EOL interrupt is maskable by IRM1 (bit 17) of the SDP command.

The channel numbers are from channel 0—15. If an SDP command is issued with a valid pointer and PTR = 1, then the ensuing EOL interrupt has an Interrupt Information field set to the 20-bit address of the start of the current descriptor. If an SDP is issued with a null pointer and PTR = 1, the ensuing interrupt has an Interrupt Information field of 0.

CMDI (0x6): Command Read Interrupt

This interrupt indicates that the first word of a command has been read by the ISA-MWAC. It can be masked by clearing the I bit in the command. The command's opcode is reported in bits 19—16 of the Interrupt Information field of the interrupt word. Other command bits are reported in bits 15—0 of the Interrupt Information field.

The channel number is channel 38.

TFC (0x8): Transmission of Frame Completed Interrupt

This interrupt is issued when a frame has been transferred from on-chip RAM to the serial shift register for transmission. It can be masked by clearing the TFCEN bit (bit 15) to 0 in the transmit descriptor (TD). The TFCEN bit is only valid when the EOF bit is set in the corresponding TD.

The channel numbers are from channel 0—15; it has no Interrupt Information field.

Interrupts (continued)

Interrupt Description (continued)

SBRI (0x9): Status of BRI Changed Interrupt

This interrupt is used to report state changes and status information for BRI-configured network ports. When enabled (IRM0 = 1; bit 14 of NP0, NP1, and NP2 commands), the SBRI interrupt can occur for four reasons:

- The BRI interface was just enabled (NP bit in register IP0 was set to 1).
- The BRI interface activation (INFO) state changed (asi bits 2—0).
- There was a bipolar violation error, multiframing error, frame synchronization error, or the T7903 failed to service the network port in time (these are described below).
- The interrupt was forced in order to generate a status report, by setting IRM1 = 1 (bit 15 in the NP0, NP1, or NP2 commands).

Table 37 describes the bits in the Interrupt Information field. These bits are most useful when forcing status reports of the BRI interface. In this way, SBRI interrupts can be disabled until a status report is desired. The asi bits (bits 2—0) are a subset of Tables 5 and 6 in ITU-T I.430 and provide activation state information. The asi bit descriptions are shown in Table 38 for a TE port and Table 39 for an NT.

SBRI operational notes:

1. After a TE-configured port has reached state F3 (asi[2:0] = 011), transitions to asi[2:0] = 000 should be considered identical to F3. These transitions are caused by the software driver clearing the NP0, NP1, or NP2 bits in IP0.
2. Transitions from asi = 0 to asi = 3 should be ignored. This occurs spontaneously after the NPx bit is set to 1 in IP0.
3. A forced SBRI interrupt may cause a state change not to report. This is most common when an NP command forces the interrupt and sets ACT = 1 at the same time. The asi bits may change from 011 to 100 between the time when the interrupt is reported and the time when the request is cleared.

Table 37. Interrupt Information Field Bits for SBRI Interrupt

Name	Interrupt Information Field Bit	SBRI Interrupt Generated?	Name/Description
mferr	12	yes	**Multiframing Error.** When mferr = 1, a TE-configured port has received an error in the bits sent from the NT that provide multiframing synchronization.
nperr	11	yes	**Network Port Failure to Service Error.** When the chip is operated in excess of recommended conditions (CHI slave with CHICKIN rate greater than 4.096 MHz while all ports are in full operation), the internal serial controller may not be able to service the network ports properly. Data may be lost or incorrectly transmitted. When nperr = 1, this condition has occurred.
vta	10	no	**Voltage Threshold Adjustment for Receiver.** The BRI receivers use an adaptive threshold mechanism. This bit reports the current state of the threshold. When vta = 0, the high threshold is in use. When vta = 1, the low threshold is in use.
bpverr	9	yes	**Bipolar Violation (BPV) Error.** When bpverr = 1, an illegal BPV was detected.
fserr	8	yes	**Frame Synchronization Error.** When fserr = 1, at least two consecutive bad frames were received.
mfm	7	no	**Multiframe Mode.** For a TE-configured port, mfm = 1 when multiframing is enabled (MFE = 1 in the NP0, NP1, and NP2 commands) and the port is synchronized to multiframes sent from the network. For an NT port, mfm = 1 when multiframing is enabled (mfe = 1).
fse	6	no	**Frame Sync Established.** When fse = 1, the port is fully synchronized.
rif4	5	no	**Receiving INFO 4 from the Network.** This is valid for TE ports only.
rif0	4	no	**Receiving INFO 0.** This is valid for both TE and NT ports.
act	3	no	**Activate Bit.** This bit reflects the state of the ACT bit in the NP0, NP1, and NP2 commands (bit 9).
asi	2—0	upon change	**Activation State Indication.** These bits provide information regarding the current activation state of the interface. See Tables 38 and 39 for details.

Interrupts (continued)

Interrupt Description (continued)

SBRI (0x9): Status of BRI Changed Interrupt (continued)

Table 38. asi Field for a TE Port

asi Bits b[2—0]	State	State Description
000	—	Interface Inactive (NPx bit set to 0 in IP0).
001	—	Not used.
010	F8	TE has lost framing.
011	F3	TE and network are inactive (neither is seeking activation).
100	F4	TE is transmitting INFO 1 and is receiving INFO 0.
101	F5	TE has sent INFO 1 to request activation and is now identifying a signal from the network. TE sends INFO 0 while identifying.
110	F6	Network is sending INFO 2 and TE is responding with INFO 3 (TE does not send operational data).
111	F7	TE and network are fully activated (data can be transmitted by TE).

Table 39. asi Field for an NT Port

asi Bits b[2—0]	State	State Description
000	G1	NT and TE are inactive (neither is seeking activation).
001—101	—	Not used.
110	G2	NT is sending INFO 2 and is waiting for INFO 3 from TE.
111	G3	NT and TE are fully activated.

The channel number is channel 32 for NP0, 33 for NP1, and 34 for NP2.

FXDT (0xA): Fixed Data Change Interrupt

The function of the FXDT interrupt is defined by IRM3 and IRM2 bits of the SDP command (bits 19 and 18) as follows:

IRM[3:2] = 00: disable FXDT interrupt,

IRM[3:2] = 01: report the second time in a row a value (of size defined by the fixed data time slot) is received,

IRM[3:2] = 10: report any change between the fixed data time slot just received and the previous one,

IRM[3:2] = 11: report every value received in the fixed data time slot (changed or not).

This interrupt applies to fixed data mode (MODE = 0x6 in SDP command) only. The changed data is reported into the 20-bit Interrupt Information field. The first bit received is the low-order bit. The channel numbers are from channel 0—31, but they are usually from channel 16—31.

CHIL (0xB): CHI Lost Frame Sync Interrupt

This interrupt reports the CHI status as defined in Table 40.

Table 40. CHIL Interrupt Information Field Bits

Interrupt Information Field Bit	CHIL Interrupt Generated?	Description
3	yes	When this bit is 1, the CHI receiver could not keep up. This may occur when the chip is operated in excess of recommended conditions (CHI slave with CHICKIN rate greater than 4.096 MHz while all ports are in full 2B+D operation).
2	yes	When this bit is a 1, the CHI expects external CHIFS and has not detected it for 250 µs (CHICM = 0 in CGM command only).
1	no	When this bit is set to 1, the CHI transmitter is active.
0	no	When this bit is set to 1, the CHI receiver is active.

Interrupts (continued)

Interrupt Description (continued)

CHIL (0xB): CHI Lost Frame Sync Interrupt (continued)

The CHIL interrupt is masked by the IRM0 bit in the CGM command (bit 14). Bit 15 of the CGM command (IRM1) forces an immediate report of the CHI status. The channel number is channel 36 (CHI).

COLL (0xB): Unrecoverable Collision

This interrupt is issued when a collision of a D-channel packet results in a packet or frame fragment that cannot be retransmitted. Legal LAP-D packets cannot collide late enough to cause this interrupt. The D channel must be restarted with an SDP command with the clear pipe bit set. If a single packet is presented to the ISA-MWAC each time for TE D-channel transmission, that packet should be queued again. If multiple packets are in the pipe, the queue should be restarted after the last marked frame. It is masked by bit 19 (IRM3) of an SDP command.

This interrupt applies to HDLC D mode (MODE = 0x3 in SDP command) only. The channel number is channel 1, 2, or 4 (pipes associated with TE D-channel transmit).

DBYT (0xC): Dropped Byte Frame Slip Interrupt

This interrupt can occur when the network ports and the CHI are not properly synchronized. When the network ports have one clock and the CHI has an independent clock (CHI is a slave), sometimes there is not room in a data pipe for new data. This interrupt reports that condition. It is masked by bit 19 of an SDP command.

This interrupt applies to the serial in to serial out mode (MODE = 0x4 in SDP command) only. The channel numbers are from channel 0 to channel 31; it has no Interrupt field.

RBYT (0xD): Repeat Byte Frame Slip Interrupt

This interrupt can occur when the network ports and the CHI are not properly synchronized. When the network ports have one clock and the CHI has an independent clock (CHI slave mode), sometimes there is no data in a pipe when it is needed. This interrupt reports that condition. It is masked by bit 19 of an SDP command.

This interrupt applies to the serial in to serial out mode (MODE = 0x4 in SDP command) only. The channel numbers are from channel 0 to channel 31; it has no Interrupt field.

LINT (0xE): Lost Interrupt Interrupt

If reportable interrupt conditions cannot be written to DRAM fast enough, a lost interrupt is reported. This interrupt can occur when individual interrupts are enabled but an interrupt queue in local DRAM has not been initialized via an IIQ command with a valid (non-null) pointer. Interrupt conditions will cause interrupt words to collect in an internal buffer. If more than 32 interrupts are generated before initializing the queue, a LINT interrupt will be generated. It will be the first interrupt word written when a valid queue is initialized. Although this interrupt cannot be masked, it cannot occur if all other interrupts are masked off. This interrupt reports the following lost interrupts: XCMP, SBRI, FXDT, CHIL, DBYT, and RBYT.

The channel number is channel 38; it has no Interrupt field.

UNDR (0xF): DMA Underrun Interrupt

This interrupt indicates that the ISA-MWAC could not keep up with the serial port. This interrupt is not reported if the last byte sent was a flag or an idle (HDLC and HDLC D modes). It is masked by bit 18 of an SDP command (IRM2). In HDLC mode, an underrun causes the current frame to be aborted, and the status bit in the transmit descriptor (TD) is set indicating an underrun. All TDs up to and including the TD with EOF = 1 are marked with a UNDR status.

When an HDLC frame is distributed over several transmit descriptors (TDs) and an EOL condition is encountered (EOL = 1 in the descriptor or a null pointer), but EOF = 0 in the last TD, an EOL interrupt will be issued if enabled. However, the frame will not be aborted and an underrun will not be reported in the TD or via the UNDR interrupt. The last data bits in the final buffer will be repeatedly transmitted until the pipe is acted upon. The best way to work around this issue is to always queue up an entire frame. In other words, if a frame is distributed over multiple TDs, always set EOF = 1 in the last TD before issuing an SDP command to start transmission.

The channel numbers are from channel 0 to channel 15; it has no Interrupt field.

Memory Structure

Figure 17 shows the memory structure used by the T7903. The value loaded into the command queue pointer (CQP) is the address of the command queue in local DRAM. The command queue must be aligned on a 4-byte boundary (the least significant 2 bits of the address must be 0). The IIQ command points to the location of the interrupt queue which must also be aligned on a 4-byte boundary. SDP commands point to transmit and receive descriptors that in turn point to transmit and receive data buffers. The descriptors also point to other descriptors (via their Next Descriptor Address fields), forming a linked chain of descriptors and data buffers. The transmit and receive descriptors must be aligned on 16-byte boundaries (the least significant 4 bits must be 0). The receive buffers must be aligned on a 4-byte boundary. Their length must be a multiple of 4 bytes. There are no address restrictions on transmit buffers.

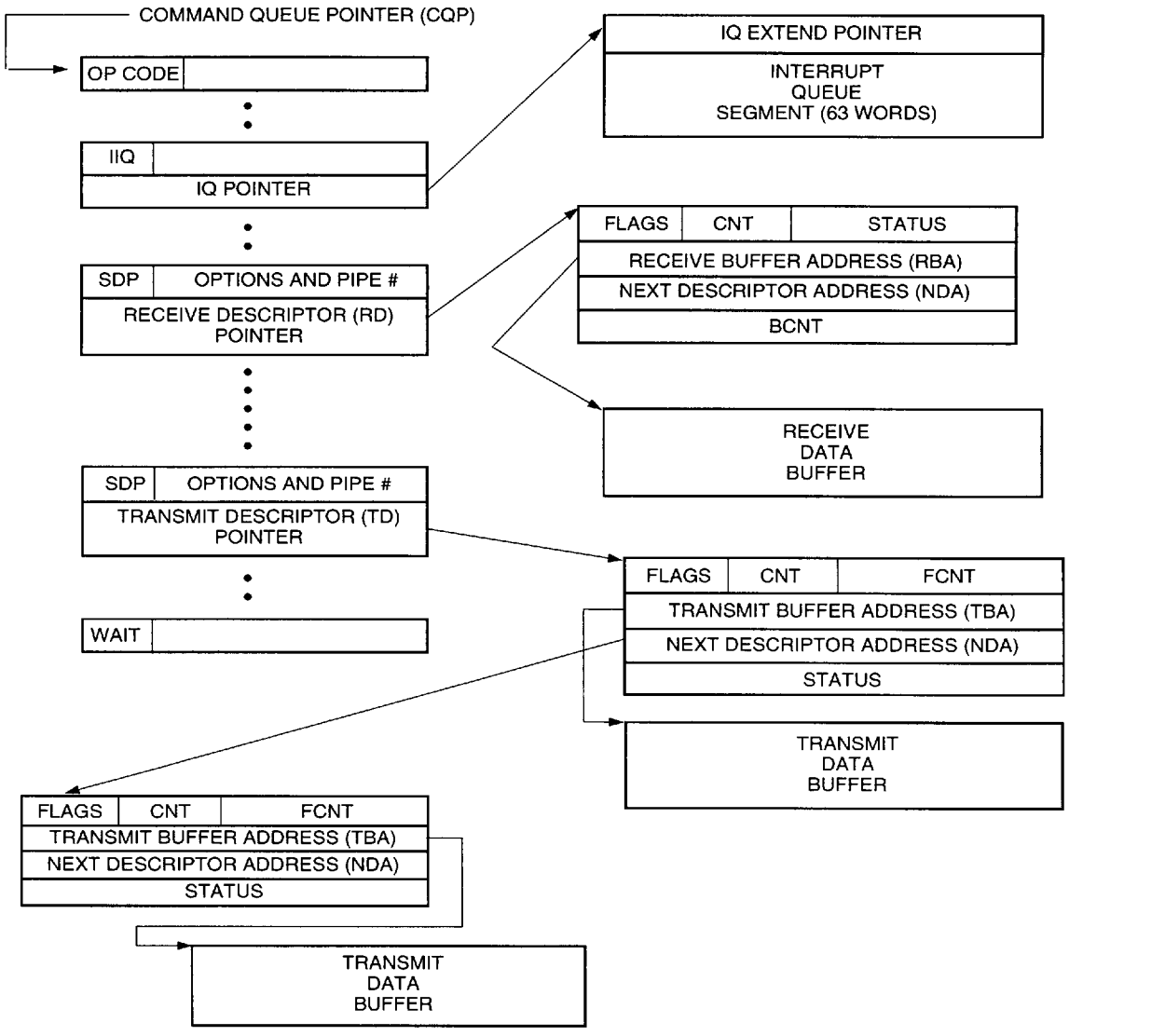


Figure 17. T7903 DRAM Memory Structures

Memory Structure (continued)

For each transmit channel, there is a linked chain of transmit descriptors (TD). Each TD has a buffer pointer and a byte count. An HDLC frame (or transparent data) can be made of one or more TDs and buffers. The Next Descriptor Address field points to the next descriptor in the transmit chain. After a buffer is read, the ISA-MWAC writes the status information into the descriptor.

For each receive channel, there is a linked list of receive descriptors (RD). Each RD has a buffer pointer and a buffer size field. An HDLC frame (or transparent data) can require one or more RDs and buffers. The Next Descriptor Address field points to the next descriptor in the receive chain. When a complete frame is received, the ISA-MWAC sets the actual byte count and status information in the descriptor. The command and interrupt queues have been described previously.

Transmit Descriptor (TD)

A transmit descriptor (TD) contains a pointer to the next TD (NDA), a pointer to the transmit buffer (TBA), the length of the transmit buffer (BCNT), the fill flag count (FCNT), and the control bits. The ISA-MWAC stores BCNT in on-chip memory and decrements it by one whenever a byte is transmitted.

If the EOF bit is set, the ISA-MWAC reads the FCNT field after transmitting BCNT data bytes and sends at least FCNT + 1 flags or idles (HDLC mode). Otherwise, the ISA-MWAC opens the next TD and continues to send data in a continuous frame. In this manner, data for a frame can be spread across several transmit descriptors. The ISA-MWAC then reads the next descriptor address (NDA) and writes the status word for the current descriptor. The functions described above are repeated until either the host issues a Setup Data Pipe (SDP) command to break the chain or the end-of-list is encountered (null NDA or EOL = 1). If a null NDA pointer is encountered, the ISA-MWAC transmits the data in the last buffer and then repeatedly sends the FLAG or IDLE pattern (depending on IDL bit in the TD) for HDLC mode or repeats the last byte(s) for transparent mode. If EOL was encountered in the last descriptor, no access to the last buffer is made (the previous descriptor's data buffer is the last transmitted).

After the ISA-MWAC completes reading the data from the transmit buffer, it writes the status in the fourth word of the transmit descriptor. All bits of the status are written in the same transaction, and TBC is **always** set to 1 when the ISA-MWAC completes use of the TD and its associated buffer. The status bits should be initialized to 0 by the host. Table 41 describes the transmit descriptor in detail. The status field for all transmit modes is shown in Table 42.

Table 41. Transmit Descriptor

31	30	29	28—20	19—16	15	14	13	12—8	7—0
EOF	DCRC	EOL	BCNT		TFCEN	MIEN	IDL	FCNT/PCLASS	
—			TBA						
—			NDA						
—									Status

Field	Word	Bit	Name/Description
EOF	1	31	**End of Frame.** For HDLC and HDLC D modes, this bit must be set by the host if the HDLC frame is completed by data in the associated buffer. The ISA-MWAC appends the CRC at the end of the frame if required (i.e., DCRC = 0). If BCNT = 0 (zero bytes in the associated buffer) and EOF = 0, then one flag or one idle code (sixteen 1s) is transmitted (depending on the previous transmit descriptor's IDL bit setting). **Caution: For transparent mode buffers, EOF must be set to 1.**
DCRC	1	30	**Do Not Append CRC (HDLC Only).** The CRC is not appended to the current frame if this bit is set to 1. This bit is ignored for transparent data.

Memory Structure (continued)

Transmit Descriptor (TD) (continued)

Table 41. Transmit Descriptor (continued)

Field	Word	Bit	Name/Description
EOL	1	29	**End of List.** When EOL = 1, the associated buffer is not used. Alternately, if EOL = 0 and NDA is null (the host sets all zeros), the data in the associated buffer is transmitted, but the next descriptor is not accessed. In either case, an EOL interrupt is issued if IRM1 = 1 in the SDP command. If an underrun condition occurs after an EOL = 1 condition is encountered by the T7903, the underrun condition will be reported via the UNDR interrupt (if enabled) when the EOL bit is cleared to 0.
BCNT	1	28—16	**Byte Count.** BCNT is the number of the data bytes in the buffer linked to the associated descriptor. If BCNT is initially 0 and the EOF bit is set, the ISA-MWAC transmits flags or idles based on the IDL and FCNT bits.
TFCEN	1	15	**Transmission of Frame Complete Interrupt Enable.** The TFCEN bit is only valid when the EOF bit is set. The host must set both the EOF and TFCEN bits to generate a TFC interrupt when the end of the frame has been transferred from the internal RAM to the serial shift register for transmission. See TFC interrupt in the Interrupt Description section.
MIEN	1	14	**Marker Interrupt Enable.** When MIEN = 1, a MINT interrupt is generated as soon as the transmit descriptor is read. When MIEN = 0, the MINT interrupt is disabled.
IDL	1	13	**Transmit Idle Characters.** When MODE = 0x2 in the SDP command (HDLC mode), IDL determines if flags or idles are transmitted between frames. If IDL = 0, FCNT + 1 HDLC flags are sent between frames. If additional packets are not queued for transmission, continuous flags are transmitted. If IDL = 1 and multiple packets are queued for transmission, FCNT + 1 idle patterns (8-bit sequences of 1s) are sent between frames. The exception to this is when FCNT = 0, in which case no idles are sent (the frames are transmitted back to back). If additional packets are not queued for transmission, continuous idles will be transmitted only if FCNT is **not** 0 (if FCNT = 0, continuous flags will be sent even though IDL = 1). Note that IDL is valid only if EOF = 1. When MODE = 0x3 in the SDP command (HDLC D mode—TE D-channel transmit), IDL must be set to 1 in the initial transmit descriptor of a frame. If the frame spans multiple buffers, then IDL must be programmed to 0 in subsequent transmit descriptors. The PCLASS field determines the D-channel priority class for the transmit direction of a TE port (HDLC D-channel mode only). This priority class determines the number of 1s that must be transmitted on the D-channel (and received on the echo channel from the network) before transmission of an HDLC frame can begin. IDL is independent of EOF.
FCNT/ PCLASS	1	12—0	**Flag Count.** When MODE = 0x2 in the SDP command (HDLC mode), FCNT is the number of flags or idle patterns (depending on IDL) that the ISA-MWAC inserts after the closing flag of the current frame. If FCNT = 0, the closing flag is shared with the opening flag of the next frame. If FCNT is not 0, FCNT + 1 idles or flags are transmitted. Valid only if EOF = 1. **Priority Class.** When MODE = 0x3 in the SDP command (HDLC D-channel mode—TE D-channel transmit), PCLASS is read in the first transmit descriptor of each frame to determine the number of 1s (priority class) transmitted before the opening flag. The number of 1s is 8 or 9 if PCLASS = 0 (priority class 1). The number of 1s is 10 or 11 if PCLASS = 1 (priority class 2). PCLASS is independent of EOF.

Memory Structure (continued)

Transmit Descriptor (TD) (continued)

Table 41. Transmit Descriptor (continued)

Field	Word	Bit	Name/Description
—	2	31—20	**Reserved.** Program to zero.
TBA	2	19—0	**Transmit Buffer Address.** This is the 20-bit starting address of the data buffer associated with the descriptor. Transmit buffers can begin on byte boundaries.
—	3	31—20	**Reserved.** Program to zero.
NDA	3	19—0	**Next Descriptor Address.** This is the 20-bit starting address of the next transmit descriptor in the linked chain. The ISA-MWAC can be configured to interrupt the host when it encounters an NDA field that is null (see EOL interrupt in the Interrupt Description section). The ISA-MWAC then sends flags or idles without regard to FCNT until it finds a good pointer after executing an SDP command or the P bit in IP0 is set. The ISA-MWAC then follows the new pointer and begins to transmit data again.
—	4	31—8	**Reserved.** Program to zero.
Status	4	7—0	**Status.** See Table 42.

Table 42. Transmit Descriptor Word 4—Status Field for All Modes

7	6	5	4	3	2	1	0
—				UNDR	ABT	—	TBC

Field	Bit	Name/Description
—	7—4	**Reserved.**
UNDR	3	**Underrun**. The serial transmitter ran out of data. For HDLC mode, the frame is aborted. For transparent mode, the last time slot's data is repeated. See UNDR interrupt in the Interrupt Description section.
ABT	2	**Abort**. The ISA-MWAC sets this bit if the frame is aborted while the ISA-MWAC is transmitting data bytes in the current descriptor. (HDLC and HDLC D modes only.) See SDP command in the Commands section and UNDR interrupt in the Interrupt Description section.
—	1	**Reserved.**
TBC	0	**Transmission of Buffer Complete**. The ISA-MWAC sets this bit when it has completed all accesses to the TD and its transmit buffer.

Receive Descriptor (RD)

A receive descriptor contains the size of the associated receive data buffer (BFSIZE), number of received bytes in the buffer (RBCNT), and status of the received frame. The ISA-MWAC writes the number of received bytes in RBCNT when it fills the buffer (RBCNT = BCNT) or it receives a closing flag. The ISA-MWAC also writes the status and updates the EOF and CBF bits. When a complete HDLC frame has been received, the associated buffer is ready for processing by the host. Subsequent received data will be stored in the next receive buffer.

When the ISA-MWAC receives an HDLC frame longer than the allocated buffer, it clears the EOF bit and sets the CBF bit, writes the RBCNT, and proceeds to the next descriptor. The ISA-MWAC continues to write the received data in the buffer assigned by the new receive descriptor. The status of the received frame is written to the RD whenever an EOF condition is detected.

It is the responsibility of the host to program the first word of the RD to all zeros when it is put on the receive queue for use by the ISA-MWAC.

Memory Structure (continued)

Receive Descriptor (RD) (continued)

Table 43. Receive Descriptor

31	30	29	28—20	19—16	15	14	13	12—8	7—0
EOF	CBF	—	RBCNT		—				Status
—			RBA						
—			NDA						
—					RBRDYEN	MIEN	EOL	BFSIZE	

Field	Word	Bit	Name/Description
EOF	1	31	**End of Frame.** The ISA-MWAC sets EOF = 1 to indicate that the current frame has ended in the buffer area for the associated descriptor. If EOF = 0 and CBF = 1, the current frame continues in the next buffer area. When EOF = 1 and CBF = 1, the end of a frame has been encountered and the current buffer is full (the buffer and entire frame are ready for host processing). The EOF bit is always set to 1 when CBF =.1 in the transparent mode.
CBF	1	30	**Completed Buffer.** The ISA-MWAC sets the CBF bit to 1 to indicate that the buffer of the associated descriptor has been filled. This does not necessarily mean the end of the frame has been received. The ISA-MWAC **always** sets CBF = 1 when it has completed all accesses to the RD and its receive buffer. Therefore, the host can process the buffer if CBF = 1.
—	1	29	**Reserved.** Program to zero.
RBCNT	1	28—16	**Received Byte Count.** This field is written by the ISA-MWAC when a buffer is full or a closing flag is received. RBCNT reflects the total number of data bytes stored in the data buffer associated with the current descriptor. If CBF = 1 and EOF = 0, RBCNT = BFSIZE. For HDLC modes of operation, the CRC is always included in the buffer and is reflected in the RBCNT field (the CRC is two bytes in length). Note that only the first RBCNT bytes in the buffer are valid and all others should be ignored.
—	1	15—8	**Reserved.** Program to zero.
Status	1	7—0	**Status.** See Table 44.
—	2	31—20	**Reserved.** Program to zero.
RBA	2	19—0	**Receive Buffer Address.** This is the 20-bit starting address of the data buffer associated with the descriptor. It **must** be 4-byte (32-bit) aligned.
—	3	31—20	**Reserved.** Program to zero.
NDA	3	19—0	**Next Descriptor Address.** This is the 20-bit starting address of the next transmit descriptor in the linked chain. The ISA-MWAC can be configured to interrupt the host when it encounters an NDA field that is null (see EOL interrupt in the Interrupt Description section). Note that data may be lost if a receiver runs out of buffers (see Overrun Condition Detected in Table 44).
—	4	31—16	**Reserved.** Program to zero.

Memory Structure (continued)

Receive Descriptor (RD) (continued)

Table 43. Receive Descriptor (continued)

Field	Word	Bit	Name/Description
RBRDY-EN	4	15	**Receive Buffer Ready Interrupt Enable.** When RBRDYEN is set to 1 by the host, the ISA-MWAC will issue an RBRDY interrupt when the buffer is filled (HDLC or transparent mode) or an HDLC frame ends in the buffer. See RBRDY interrupt in the Interrupt Description section.
MIEN	4	14	**Marker Interrupt Enable.** When MIEN = 1, the ISA-MWAC will issue a MINT interrupt as soon as the RD is read. This allows interrupts that are not frame synchronous, for list management. See MINT interrupt in the Interrupt Description section.
EOL	4	13	**End of List.** This bit is programmed by the host. When EOL = 1, the associated buffer is not used. Alternately, if EOL = 0 and NDA is null (all zeros), the associated buffer is filled, but no other descriptors are accessed. In either case, an EOL interrupt is issued if IRM1 = 1 in the SDP command.
BFSIZE	4	12—0	**Buffer Size**. BFSIZE is the number of bytes the host allocates for the receive buffer. Note that BFSIZE must be greater than or equal to four and be a multiple of four. Frames (data delimited by an opening and closing flag) with less than three octets are not stored to DRAM (they are discarded).

The ISA-MWAC writes the status in the receive descriptor when it detects an EOF condition. The Status field bit assignments are shown in Table 44.

Table 44. Receive Descriptor Word 4—Status Field for All Modes

7	6	5	4	3	2	1	0
CRCS	BBC	ABT	—	OVRN	—		

Field	Bit	Name/Description
CRCS	7	**CRC Status.** If CRCS = 0, the CRC was correct for the received frame. If CRCS = 1, the CRC was bad for the received frame (HDLC mode; valid only when EOF = 1).
BBC	6	**Bad Byte Count.** BBC = 1 indicates that a frame has been received that is not a multiple of 8 bits. The frame could still have good or bad CRC status (HDLC mode; valid only when EOF = 1).
ABT	5	**Abort.** ABT = 1 if the receive frame was aborted (HDLC mode; valid only when EOF = 1).
—	4	**Reserved.**
OVRN	3	**Overrun Condition Detected.** The OVRN bit is set to 1 for an overrun condition. Data is lost from the buffer. Note that this condition cannot be reported until there are receive descriptors in the receive descriptor list. Subsequent buffers are filled normally.
—	2—0	**Reserved.**

Data Modes

When transferring data between local DRAM and the serial interfaces, the ISA-MWAC's long data pipes can be configured for either HDLC formatting or transparent mode.

HDLC Mode

Table 45 shows the HDLC frame format. The Information field is optional. Its length ranges from 0 to 8190 bytes.

Table 45. HDLC Frame Format

Opening Flag	Header Bytes	Information Field	CRC	Closing Flag
01111110	Up to 7 Bytes	Optional	2 bytes	01111110

The transmitter produces HDLC frames bounded by flags from the data contained in one or more transmit buffers. The ITU-T 16-bit CRC is generated by the ISA-MWAC and appended to the user-supplied data. The polynomial used in calculating the CRC is $X^{16} + X^{12} + X^5 + 1$. The zero bit stuffing for data transparency is performed on the data between the last bit of the opening flag and the first bit of the closing flag.

The receiver recognizes the start of a frame by searching the incoming data stream for a nonflag octet following a flag. It then removes the zeros that were inserted for data transparency, writes this data into one or more receive buffers, and performs the CRC detection checks until a closing flag is detected. The 2 bytes of CRC are stored in the receive buffer immediately following the data.

Zero Bit Insertion/Deletion (Bit Stuffing/Unstuffing)

The ISA-MWAC performs the bit stuffing and unstuffing for the information field on the data setup in the TDs to maintain data transparency. A zero bit is inserted (bit stuffing) into the transmitted bit stream after five ones. The receiver deletes a zero immediately following five ones. The purpose of bit stuffing all data internal to the frame is to permit the use of a flag character (01111110) to delineate a frame and abort (01111111) and idle (11111111) characters. Whenever the receiver encounters more than five consecutive 1s, it is interpreted as part of one of these special characters.

Flags, Aborts, and Idles

The flag has the binary representation of 01111110 (0x7e) and is used for frame delineation. The flags are also used as fill characters between frames. If the receive unit receives one flag between two frames, the ISA-MWAC recognizes it as the closing flag of one frame and also the opening flag of the next frame. The transmit unit always transmits at least one flag between successive frames, and an additional number of flags may be transmitted by programming the FCNT field in the transmit descriptor. This is described in detail in the Memory Structure section.

The receive unit also recognizes two or more successive flags which share the zero bit in between them (011111101111110). The transmit unit does not share the zero bit between flags (i.e., 0111111001111110 is transmitted).

The abort character has the binary representation of 01111111 (0x7f). The transmit unit sends the abort if the ABT bit in the SDP command is set. The receiver interprets seven consecutive 1s as an abort.

The idle character has the binary representation of 11111111 (0xff). A number of idle characters equal to FCNT can be transmitted between frames as an alternative to the flags. The opening flag and closing flag are still sent to delimit the frame. When receiving data, an idle condition is detected after receiving 15 consecutive ones.

Short Frames

Frames less than 24 bits long, including CRC, are dropped and not reported. No common protocols use frames less than 32 bits including CRC.

Transparent Mode

In the transparent mode, the ISA-MWAC transmits the data without any bit manipulation. For the receive channels, the ISA-MWAC continues to write the received data into system memory as specified in the receive descriptor. The receiver continues to fill the buffers until a null pointer is encountered or the host (via a command) stops the receiver from buffering data.

Crystal Oscillator

The T7903 requires a 24.592 MHz clock source. To supply this, a 24.592 MHz crystal can be connected between the RCLK and XTALO pins. External 33 pF 5% capacitors must be connected from RCLK and XTALO to Vss. Crystal specifications are given in Table 46. If a crystal is not used, a 24.592 MHz (100 ppm tolerance or less) signal must be provided to the RCLK pin and XTALO should be left unconnected.

Table 46. Device Crystal Specifications

Parameter	Value
Frequency	24.592 MHz
Oscillation Mode	Fundamental, Parallel Resonant
Load Capacitance	21 pF
Effective Series Resistance	25 Ω Maximum
Shunt Capacitance	7 pF Maximum
Frequency Tolerance and Stability*	55 ppm
Saronix Vendor Information and Part Number Saronix 151 Laura Lane Palo Alto, CA 94303 (415) 855-6806 Part Number: SRX5577	
***CTS*† Vendor Information and Part Number** CTS 400 Reimann Ave. Sandwich, IL 60548 (815) 786-8411 Part Number R1B22A21 @ 24.592 MHz	

* This specification includes frequency tolerance at 25 °C, temperature stability over the range from 0 °C to 70 °C, and aging.
† *CTS* is a registered trademark of Chicago Telephone Supply.

An internal 12.288 MHz (average) signal is produced from the 24.592 MHz signal by occasionally doubling a period. The 12.288 MHz signal is used to produce the CHI master mode clock output (CHICKOUT) as well as the ISDN basic rate timing. Because synchronization with the network is achieved by doubling a period and never dropping a period, the CHI clock never has a very short period.

JTAG Test Access Port

The test access port is a four-wire interface that complies with the *IEEE** 1149.1A-1993 standard. This standard provides a means of selecting a value to drive each digital output and sensing each digital input through a serial interface. This procedure can be used for testing connections between points on the printed-circuit board.

Instruction Register

The instruction register (IR) is 4 bits in length (minimum length with no parity bit). The instructions are defined in Table 47.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 47. Instruction Register Description

Instruction	Hex	Binary (type)
EXTEST	0	0000 (mandatory)
IDCODE	1	0001 (optional)
SAMPLE/PRELOAD	2	0010 (mandatory)
HIGHZ	3	0011 (optional)
BYPASS*	4	0100 (mandatory)
BYPASS*	5	0101 (mandatory)
BYPASS*	6	0110 (mandatory)
BYPASS*	7	0111 (mandatory)
CLAMP	8	1000 (optional)
BYPASS *	9—F	1001—1111 (mandatory)

* LSB shifted in JTDI first.

JTAG Test Access Port (continued)

Instruction Register (continued)

The following instructions are optional and not supported in this device: INTEST, RUNBIST, and USERCODE. A fixed binary 0001 pattern (the 1 into the LSB) is loaded into the IR in the capture-IR controller state. The IDCODE instruction (binary 0001) is loaded into the IR during the test-logic-reset controller state and also at powerup.

The following is an explanation of each instruction and its effect on the device pins.

EXTEST

This instruction places the boundary-scan register (BSR) in the scan chain. EXTEST forces the outputs and bidirectional pins to the value in the holding register. The holding register can be preloaded by using the SAMPLE/PRELOAD instruction prior to the EXTEST instruction; otherwise, the state of the outputs and bidirectional pins is unknown.

IDCODE

This instruction places the device identification register in the scan chain. The device ID value is 0x5630e03b.

SAMPLE/PRELOAD

This instruction places the BSR in the scan chain. SAMPLE/PRELOAD samples the state of the pins and pin enables (for 3-statable pins). The sampled values are shifted out, and another pattern is shifted in on JTDI (PRELOAD). The new values are not forced on the pins, but are held in the holding register.

HIGHZ

This instruction places the BYPASS register in the scan chain. It also forces all the 3-statable outputs to a high-impedance state and all bidirectional pins to an input state.

BYPASS

This instruction places the BYPASS register in the scan chain.

CLAMP

The CLAMP instruction places the BYPASS register in the scan chain, and then uses the values in the holding register to force the outputs and bidirectional pins into a known state (assuming the SAMPLE/PRELOAD instruction has been issued).

Boundary-Scan Register

The boundary-scan register (BSR) is 121 bits in length. Table 27 gives descriptions of each cell in the boundary-scan chain beginning at the LSB. No cell can apply its value to on-chip logic.

Note: All enables are cleared to 0 at powerup reset. JTDO and XTALO are not 3-statable by OE.

Table 48. Boundary-Scan Register

Name	Boundary-Scan Register Bit	Description
PIO[0:7]	0—7	Bidirectional
EN_PIO0	8	PIO0 is an input when EN_PIO0 = 0
EN_PIO1	9	PIO1 is an input when EN_PIO1 = 0
EN_PIO2	10	PIO2 is an input when EN_PIO2 = 0
EN_PIO3	11	PIO3 is an input when EN_PIO3 = 0
EN_PIO4	12	PIO4 is an input when EN_PIO4 = 0
EN_PIO5	13	PIO5 is an input when EN_PIO5 = 0
EN_PIO6	14	PIO6 is an input when EN_PIO6 = 0
EN_PIO7	15	PIO7 is an input when EN_PIO7 = 0
DRAMREQ	16	Input
DRAMACK	17	3-statable Output

JTAG Test Access Port (continued)

Boundary-Scan Register (continued)

Table 48. Boundary-Scan Register (continued)

Name	Boundary-Scan Register Bit	Description
CASN	18	3-statable output
RASN	19	3-statable output
WEN	20	3-statable output
DA[0:9]	21—30	3-statable output
EN_DC	31	CASN, RASN, WEN, DA[0:9] are HIZ when EN_DC = 0
DD[0:7]	32—39	Bidirectional
EN_DD	40	DD[0:7] input when EN_DD = 0
IOCHRDY	41	Open collector output
IOCS16N	42	Open collector output
RESET	43	Input
IRQ10	44	3-statable output
EN_IRQ10	45	IRQ10 HIZ when EN_IRQ10 = 0
IRQ11	46	3-statable output
EN_IRQ11	47	IRQ11 HIZ when EN_IRQ11 = 0
IRQ12	48	3-statable output
EN_IRQ12	49	IRQ12 HIZ when EN_IRQ12 = 0
IRQ15	50	3-statable output
EN_IRQ15	51	IRQ15 HIZ when EN_IRQ15 = 0
IOWN	52	Input
IORN	53	Input
AEN	54	Input
SBHEN	55	Input
SA[0:11]	56—67	Input
SD[0:15]	68—83	Bidirectional
EN_DATA_L	84	SD[0:7] are inputs when EN_DATA_L = 0
EN_DATA_U	85	SD[8:15] are inputs when EN_DATA_U = 0
OE	86	Input
IRQ3	87	3-statable output
EN_IRQ3	88	IRQ3 HIZ when EN_IRQ3 = 0
EN_MISC	89	DRAMACK, CHIDXEN, TO are HIZ when EN_MISC = 0
NP2_PR	90	Input
NP2_NR	91	Input
NP2_VTA	92	Bidirectional*

* Controls the internal receiver threshold selection for EXTEST and CLAMP commands. Samples receiver threshold selection SAMPLE/PRELOAD command.

JTAG Test Access Port (continued)

Boundary-Scan Register (continued)

Table 48. Boundary-Scan Register (continued)

Name	Boundary-Scan Register Bit	Description
NP2_PT	93	3-statable output
NP2_NT	94	Bidirectional
EN_NP2	95	NP2_PT is HIZ and NP2_NT is an input when EN_NP2 = 0
NP1_PR	96	Input
NP1_NR	97	Input
NP1_VTA	98	Bidirectional*
NP1_PT	99	3-statable output
NP1_NT	100	Bidirectional
EN_NP1	101	NP1_PT is HIZ and NP1_NT is an input when EN_NP1 = 0
NP0_PR	102	Input
NP0_NR	103	Input
NP0_VTA	104	Bidirectional*
NP0_PT	105	3-statable output
NP0_NT	106	Bidirectional
EN_NP0	107	NP0_PT is HIZ and NP0_NT is an input when EN_NP0 = 0
TECK	108	Bidirectional
EN_TECK	109	TECK is an input when EN_TECK = 0
IRQ5	110	3-statable output
EN_IRQ5	111	IRQ5 HIZ when EN_IRQ5 = 0
C2	112	3-statable output
CHICKOUT	113	3-statable output
EN_CHI	114	CHICKOUT, C2 HIZ; CHIFS are inputs when EN_CHI = 0
CHICKIN	115	Input
CHIDR	116	Input
IRQ7	117	3-statable output
EN_IRQ7	118	IRQ7 HIZ when EN_IRQ7 = 0
CHIFS	119	Bidirectional
CHIDXEN	120	3-statable output
CHIDX	121	Bidirectional
EN_CHIDX	122	CHIDX input when EN_CHIDX = 0
RCLK	123	Input
ENPNP	124	Input

* Controls the internal receiver threshold selection for EXTEST and CLAMP commands. Samples receiver threshold selection SAMPLE/PRELOAD command.

I/O Specifications

Clock Inputs

Any input which serves to clock storage elements or latch other inputs is a clock input. Rise and fall times are specified at 10%—90% points.

Other Inputs

The setup and hold time specifications are the minimum durations of an input signal respectively before and after the clock edge latching of a particular input signal. These are expressed in terms of 50% transition points.

Outputs

Propagation delay is generally measured from the 50% point of the reference signal transition to the 50% point of the output signal transition.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A	0	—	70	°C
Storage Temperature	T_{stg}	–40	—	150	°C
Voltage on Any Pin with Respect to Ground (Vss)	—	–0.25	—	V_{DD} + 0.25	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison. The HBM ESD threshold presented in Table 49 was obtained by using these circuit parameters.

Table 49. ESD Threshold Voltage

Device	Voltage
T7903	1000 V

Electrical Characteristics

Ambient temperature = 0 °C to 70 °C, V_{DD} = 5.0 V ± 5%, V_{SS} = 0.0 V (unless otherwise specified).

Table 50. Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage:						
Low	V_{IL}	—	–0.5	—	0.8	V
High	V_{IH}	—	2.4	—	V_{DD} + 0.25	V
Output Voltage:		ISA-MWAC Outputs				
Low	V_{OL}	I_{OL} = 24mA	—	—	0.4	V
High	V_{OH}	I_{OH} = –24 mA	2.8	—	—	V
Input Leakage Current:						
TTL Inputs	I_{ILH}, I_{ILL}	V_{IH} = 5.25 V	–10	—	10	µA
Inputs with Pull-Up	I_{ILHP}, I_{ILLP}	V_{IH} = 5.0 V	—	—	500	µA
Power Dissipation	PD_1	25 °C, V_{DD} = 5.0 V	—	650	—	mW
f_{rCLK} = 24.592 MHz	PD_2	25 °C, V_{DD} = 5.62 V	—	—	1000	mW
C_L = 70 pF	LPM*	25 °C, V_{DD} = 5.0 V	—	30	—	mW

* See Register IP0, bit 14 description.

Network Port Interface Specifications

Table 51. Network Port Outputs (ISDN Mode)

Output Name	Sinking		Sourcing		Propagation Delay Max	Loading
	Voltage	Current	Voltage	Current		
NPx_PT	3.5 V	7.5 mA	4.6 V	7.5 mA	—	—
NPx_NT	3.5 V	7.5 mA	4.6 V	7.5 mA	—	—
TECK	0.4 V	1.60 mA	2.8 V	1.00 mA	38 ns	70 pF

Table 52. TECK Clock Input

Clock Name	Voltage Level		Period	Rise Time Max	Fall Time Max
	High	Low			
TECK	2.4 V	0.8 V	125 µs	10 ns	10 ns

Table 53. Network Port Outputs (Synchronous Serial Mode)

Output Name	Sinking		Sourcing		Propagation Delay	Loading
	Voltage	Current	Voltage	Current		
SNDx	0.4 V	–8.0 mA	2.8 V	8.0 mA	40 ns	40 pF
STx	0.4 V	–8.0 mA	2.8 V	8.0 mA	40 ns	40 pF

Electrical Characteristics (continued)

Network Port Interface Specifications (continued)

Table 54. Network Port Inputs (Synchronous Serial Mode)

Input Name	Voltage Level		Rise Time	Fall Time
	High	Low		
STx	2.4 V	0.8 V	40 ns	40 ns
RDx	2.4 V	0.8 V	40 ns	40 ns
RTx	2.4 V	0.8 V	40 ns	40 ns

Concentration Highway Interface Specifications

Table 55. CHI Clock Input

Clock Name	Voltage Level		Minimum Period	Rise Time Max	Fall Time Max	Pulse Width (Min)		Mode
	High	Low				High	Low	
CHICKIN	2.4 V	0.8 V	165 ns	10 ns	10 ns	73 ns	73 ns	CMS = 0, 1

Table 56. CHI Clock Output

Clock Name	Voltage Level		Rise and Fall Time	Load	Duty Cycle Min		Mode
	High	Low	Max		High	Low	
CHICKOUT	2.8 V	0.4 V	10 ns	100 pF	83 ns	83 ns	CMST = 0,1

Table 57. Concentration Highway Input

Input Name	Voltage Level		Rise Time	Fall Time	Setup Time	Hold Time	Mode
	High	Low	Max	Max	Min	Min	
CHIDX	2.4 V	0.8 V	20 ns	20 ns	25 ns	0 ns	RCE = 1
CHIDR	2.4 V	0.8 V	20 ns	20 ns	25 ns	0 ns	RCE = 0
CHIFS	2.4 V	0.8 V	60 ns	60 ns	25 ns	15 ns	FE = 0

Electrical Characteristics (continued)

JTAG Interface Specifications

Table 58. Concentration Highway Outputs

Output Name	Sinking		Sourcing		Propagation Delay	Capacitive Loading	Mode
	Voltage	Current	Voltage	Current			
CHIDX	0.4 V	8.00 mA	2.8 V	8.00 mA	30 ns	100 pF	XCE = 1
CHIFS	0.4 V	8.00 mA	2.8 V	8.00 mA	30 ns	100 pF	FD = 0

Table 59. JTAG Clock Input

Clock Name	Voltage Level		Maximum Period	Rise and Fall Max	Input Capacitance
	High	Low			
JTCK	2.4 V	0.8 V	80 ns	20 ns	3.5 pF

Table 60. JTAG Inputs

Input Name	Voltage Level		Rise and Fall Max	Setup Time Min	Hold Time Min
	High	Low			
JTMS	2.4 V	0.8 V	20 ns	40 ns	35 ns
JTDI	2.4 V	0.8 V	20 ns	40 ns	35 ns

Table 61. JTAG Output

Output Name	Sinking		Sourcing		Propagation Delay	Capacitance Loading
	Voltage	Current	Voltage	Current		
JTDO	0.4 V	3.00 mA	2.8 V	3.00 mA	40 ns	70 pF

Timing Characteristics

Table 62. General ISA Interface I/O Access Timing Parameters (Refer to Figure 18.)

Symbol	Parameter	Min	Typ	Max	Unit
T1	I/O Command Cycle Time	240	—	—	ns
T2	I/O Command Active to Inactive Time	120	—	—	ns
T3	I/O Command Inactive to Active Time	120	—	—	ns
T4	SA, AEN, & $\overline{SBHE}$ Setup Time to Active I/O Command	10	—	—	ns
T5	SA, AEN, & $\overline{SBHE}$ Hold Time After Inactive I/O Command	10	—	—	ns
I1	IOCHRDY Inactive After Active I/O Command Time	—	—	20	ns
I2	IOCHRDY Active Time	125	—	5530*	ns
C1	$\overline{IOCS16}$ Active Delay After Valid SA, AEN, & $\overline{SBHE}$	—	—	50	ns
C2	$\overline{IOCS16}$ 3-state Time After Invalid SA, AEN, & $\overline{SBHE}$	—	—	50	ns

* Maximum value is for a 64-byte page mode access + refresh, or (64 x 2 + 4) + 4 = 136 RCLK cycles = 5530 ns.

Table 63. ISA Interface I/O Read Timing Parameters (Refer to Figure 18.)

Symbol	Parameter	Min	Typ	Max	Unit
R1	Read Access Time; Add I1 + I2 + R2 if Needed	0	—	100	ns
R2	Valid READ Data After Inactive IOCHRDY Time	–125	—	10	ns
R3	3-state Delay Time After Inactive $\overline{IOR}$	—	—	30	ns

Table 64. ISA Interface I/O Write Timing Parameters (Refer to Figure 18.)

Symbol	Parameter	Min	Typ	Max	Unit
W1	Write Data Setup Time to Inactive $\overline{IOW}$	10	—	—	ns
W2	IOCHRDY Active to $\overline{IOW}$ Inactive	0	—	—	ns
W3	Data Hold Time After Inactive I/O Command	10	—	—	ns

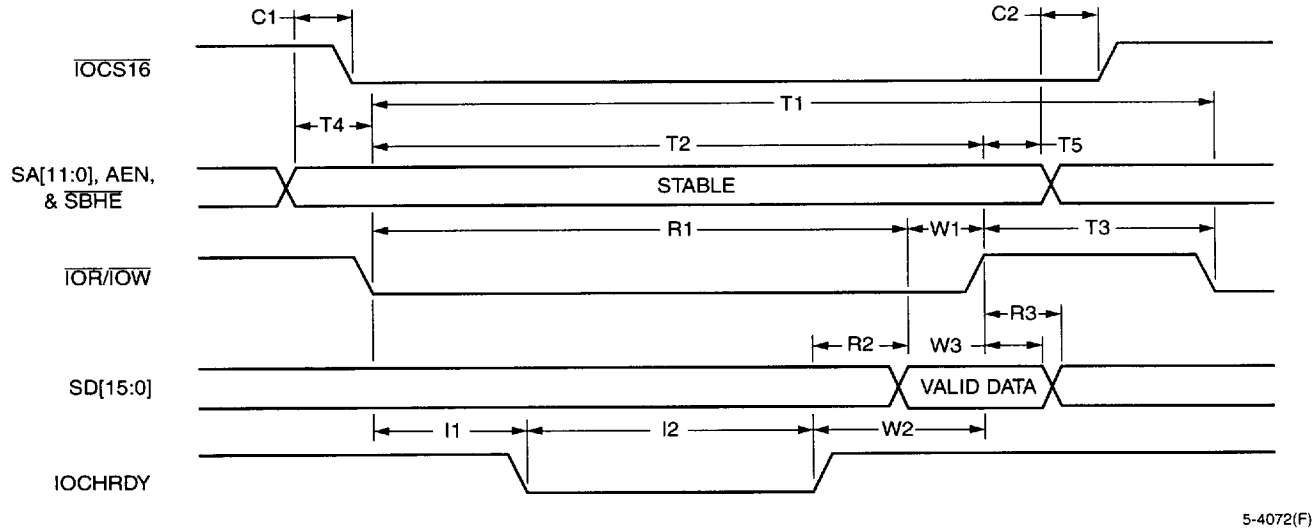


Figure 18. ISA Interface I/O Access Timing

Timing Characteristics (continued)

Table 65. Local DRAM Interface Fast Page Mode and Standard Cycle Read Timing (Refer to Figure 19.)

Symbol	Parameter	Min	Typ	Max	Unit
R1	ASR: Row Address Setup Time	20	—	—	ns
R2	RAH: Row Address Hold Time	10	—	—	ns
R3	RCS: Read Command Setup Time	80	—	—	ns
R4	RCH/RRH: Read Command Hold Time	80	—	—	ns
C1	ASC: Column Address Setup Time	20	—	—	ns
C2	CAH: Column Address Hold Time	60	—	—	ns
C3	CAS: $\overline{CAS}$ Pulse Width	35	—	80	ns
T1	CRP: $\overline{CAS}$ to $\overline{RAS}$ Precharge Time	40	—	—	ns
T2	RCD: $\overline{RAS}$ to $\overline{CAS}$ Delay Time	35	—	—	ns
T5	RAD: $\overline{RAS}$ to Column Address Delay Time	15	—	25	ns
T6	CSH: $\overline{CAS}$ Hold Time	135	—	—	ns
T7	RSH: $\overline{RAS}$ Hold Time	35	—	—	ns
T8	CRP: $\overline{CAS}$ to $\overline{RAS}$ Precharge Time	100	—	—	ns
T9	RAL: Column Address to $\overline{RAS}$ Lead Time	50	—	—	ns
T10	AR: Column Address Hold Time w.r.t. $\overline{RAS}$	100	—	—	ns

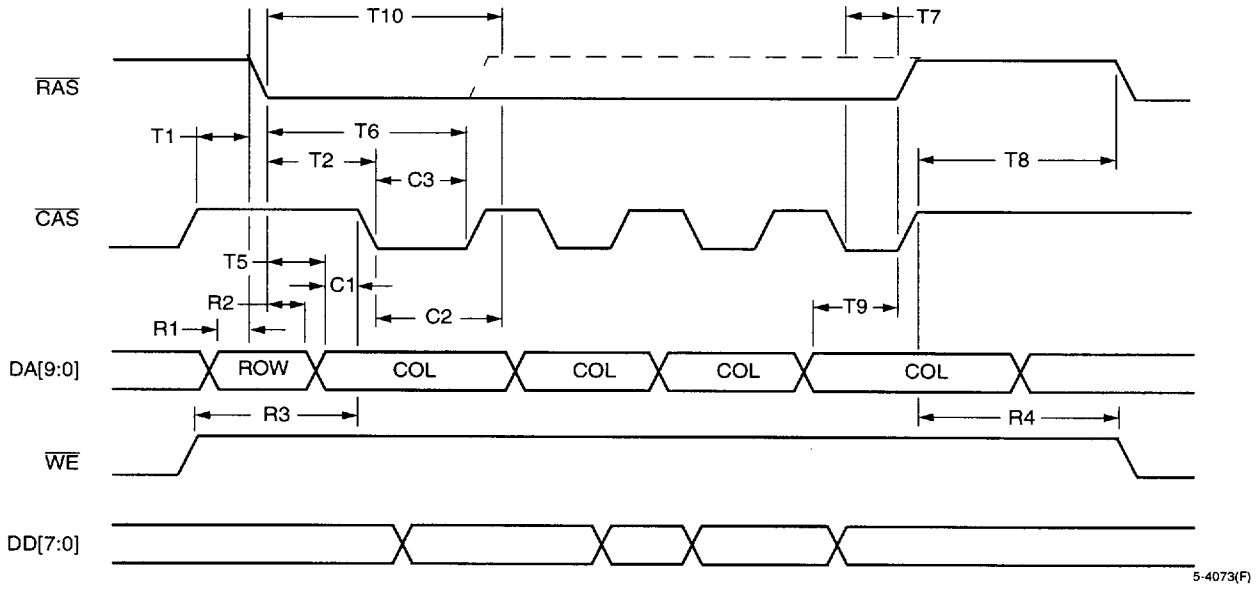


Figure 19. Local DRAM Interface Fast Page Mode and Standard Cycle Read Timing

Timing Characteristics (continued)

Table 66. Local DRAM Interface Fast Page Mode and Standard Cycle Write Timing (Refer to Figure 20.)

Symbol	Parameter	Min	Typ	Max	Unit
W1	WCS: Write Command Setup Time	20	—	—	ns
W2	CWL: Write Command to $\overline{CAS}$ Lead Time	100	—	—	ns
W3	WP: Write Pulse Width	115	—	5530*	ns
W4	WCH: Write Command Hold Time from $\overline{CAS}$	35	—	—	ns
W5	WCR: Write Command Hold Time from $\overline{RAS}$	115	—	—	ns
W6	RWL: Write Command to $\overline{RAS}$ Lead Time	115	—	—	ns
W7	DS: Data Setup Time	1	—	—	ns
W8	DH: Data Hold Time	39	—	—	ns
W9	DHR: Data Hold Time w.r.t. $\overline{RAS}$	115	—	—	ns
T11	PC: Fast Page Mode Cycle Time	75	—	—	ns
T12	CP: $\overline{CAS}$ Precharge Time	35	—	—	ns
T13	RAS: $\overline{RAS}$ Pulse Width	115	—	—	ns
T14	RP: $\overline{RAS}$ Precharge Time	115	—	—	ns

* Maximum value is for a 64-byte page mode access + refresh, or (64 x 2 + 4) + 4 = 136 RCLK cycles = 5530 ns.

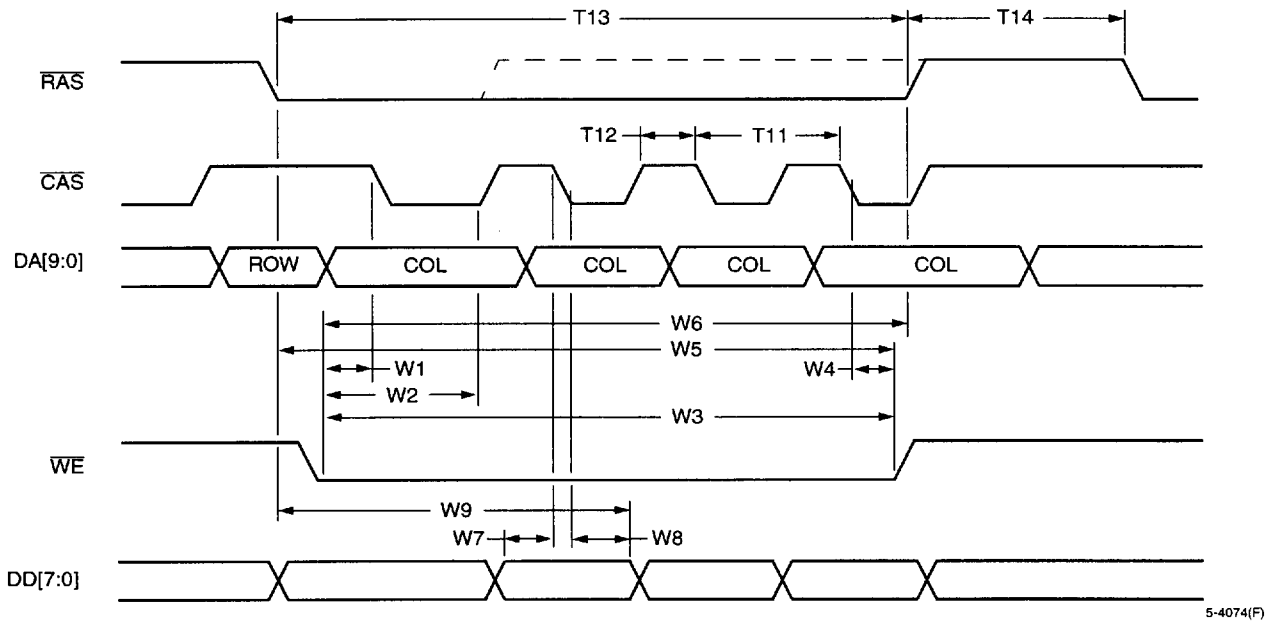


Figure 20. Local DRAM Interface Fast Page Mode and Standard Cycle Write Timing

Timing Characteristics (continued)

Table 67. Local DRAM Interface CAS Before RAS Refresh and DRAMREQ/ACK Timing (Refer to Figure 21.)

Symbol	Parameter	Min	Typ	Max	Unit
F1	RPC: $\overline{RAS}$ to $\overline{CAS}$ Precharge Time	35	—	—	ns
F2	CSR: $\overline{CAS}$ Setup Time	35	—	—	ns
F3	CHR/WRH: $\overline{CAS}$ Hold Time/WEN Hold Time	75	—	—	ns
F4	WRP: WEN to $\overline{RAS}$ Precharge Time	75	—	—	ns
G1	Assert DRAMREQ to DRAMACK Delay Time	—	—	160 + dly*	ns
G2	DRAMACK to 3-state Delay Time	0	—	—	ns
G3	Deassert DRAMREQ to DRAMACK Delay Time	—	—	160	ns
G4	Deassert DRAMACK to Valid Signal Delay Time	0	—	—	ns

* Note that dly could be as high as a 64-byte page mode access + refresh, or (64 x 2 + 4) + 4 = 136 RCLK cycles = 5530 ns.

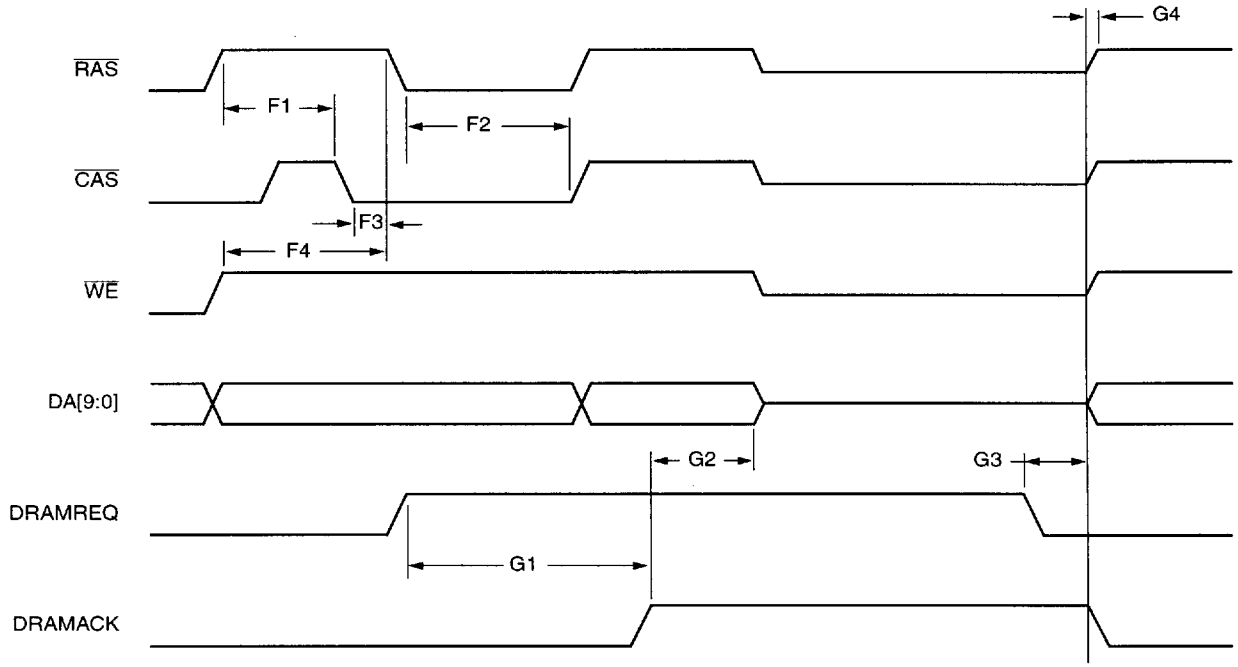


Figure 21. Local DRAM Interface CAS Before RAS Refresh and DRAMREQ/ACK Timing

Timing Characteristics (continued)

Table 68. Concentration Highway Interface (CHI) Timing (Refer to Figure 22.)

Symbol	Parameter	Min	Typ	Max	Unit
C1	Data Setup Time to CHICKIN	25	—	—	ns
C2	CHIFS Setup Time to CHICKIN	25	—	—	ns
C3	Data Hold Time w.r.t. CHICKIN	4	—	—	ns
C4	CHIFS Hold Time w.r.t. CHICKIN	15	—	—	ns
C5	Delay Time for CHIDX/CHIFS	—	—	30/35	ns
C6	Deassert CHIDXEN to 3-state CHIDX	—	—	5	ns
C7	Assert CHIDXEN to Valid CHIDX	—	—	5	ns

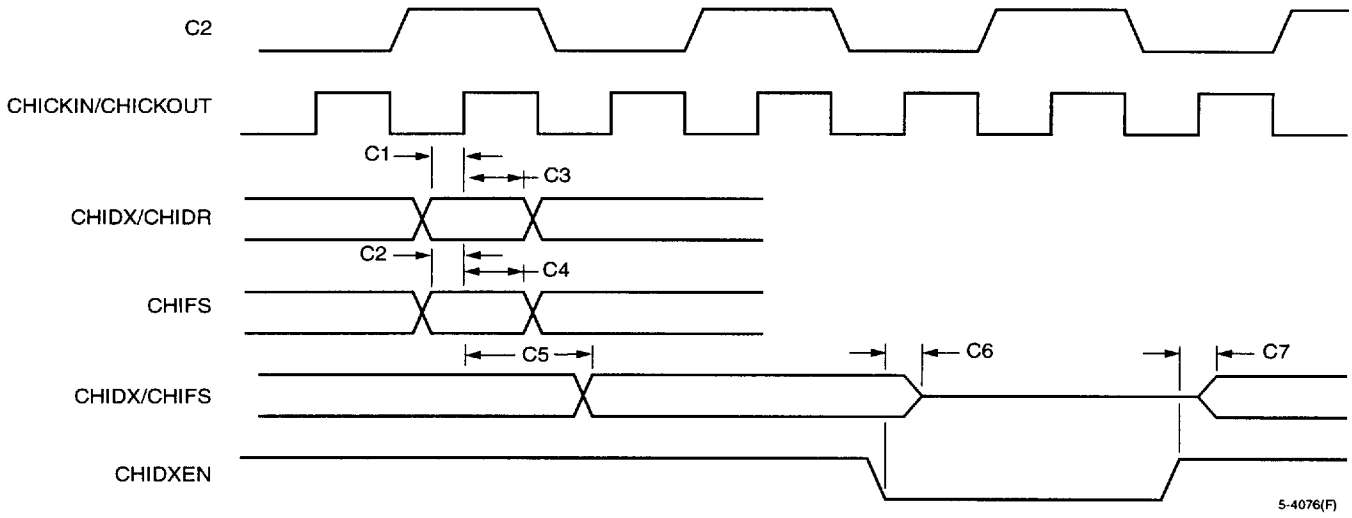


Figure 22. Concentration Highway Interface (CHI) Timing

Timing Characteristics (continued)

Table 69. $\overline{CS0}$ and $\overline{CS1}$ Timing (Refer to Figure 23.)

Symbol	Parameter	Min	Typ	Max	Unit
D1	Valid SA[9:0], AEN, to $\overline{CS0}$/$\overline{CS1}$ Active Time	—	—	50*	ns
D2	Invalid SA[9:0], AEN, to $\overline{CS0}$/$\overline{CS1}$ Inactive Time	—	—	50*	ns

* PIO4/CS0 and PIO5/CS1 are pulled high through 10 kΩ resistors (to invoke extended I/O chip select mode).

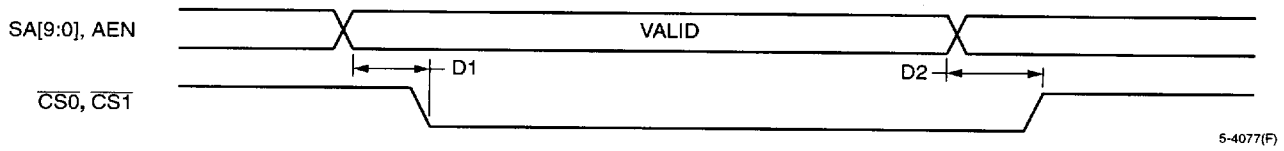


Figure 23. $\overline{CS0}$ and $\overline{CS1}$ Timing

Timing Characteristics (continued)

Table 70. Network Port Synchronous Mode Timing (Refer to Figure 17, Figure 24, and SCKM0 and SCKM1 bits in NP Command.)

Symbol	Parameter	Min	Typ	Max	Unit
T1	Setup Time to Input Clock	40	—	—	ns
T2	Hold Time from Input Clock	40	—	—	ns
D1	Delay Time from Clock	—	—	40	ns
D2	RT to ST Clock Delay (SCKM1 = 0, SCKM0 = 1)	—	—	TBD	ns

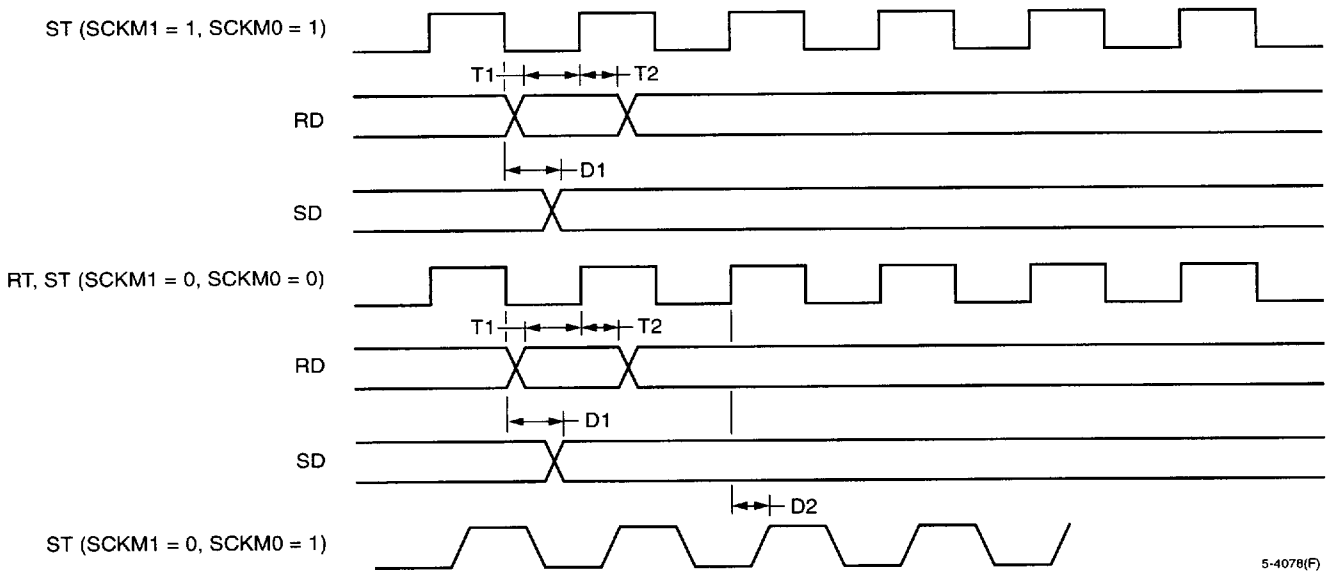
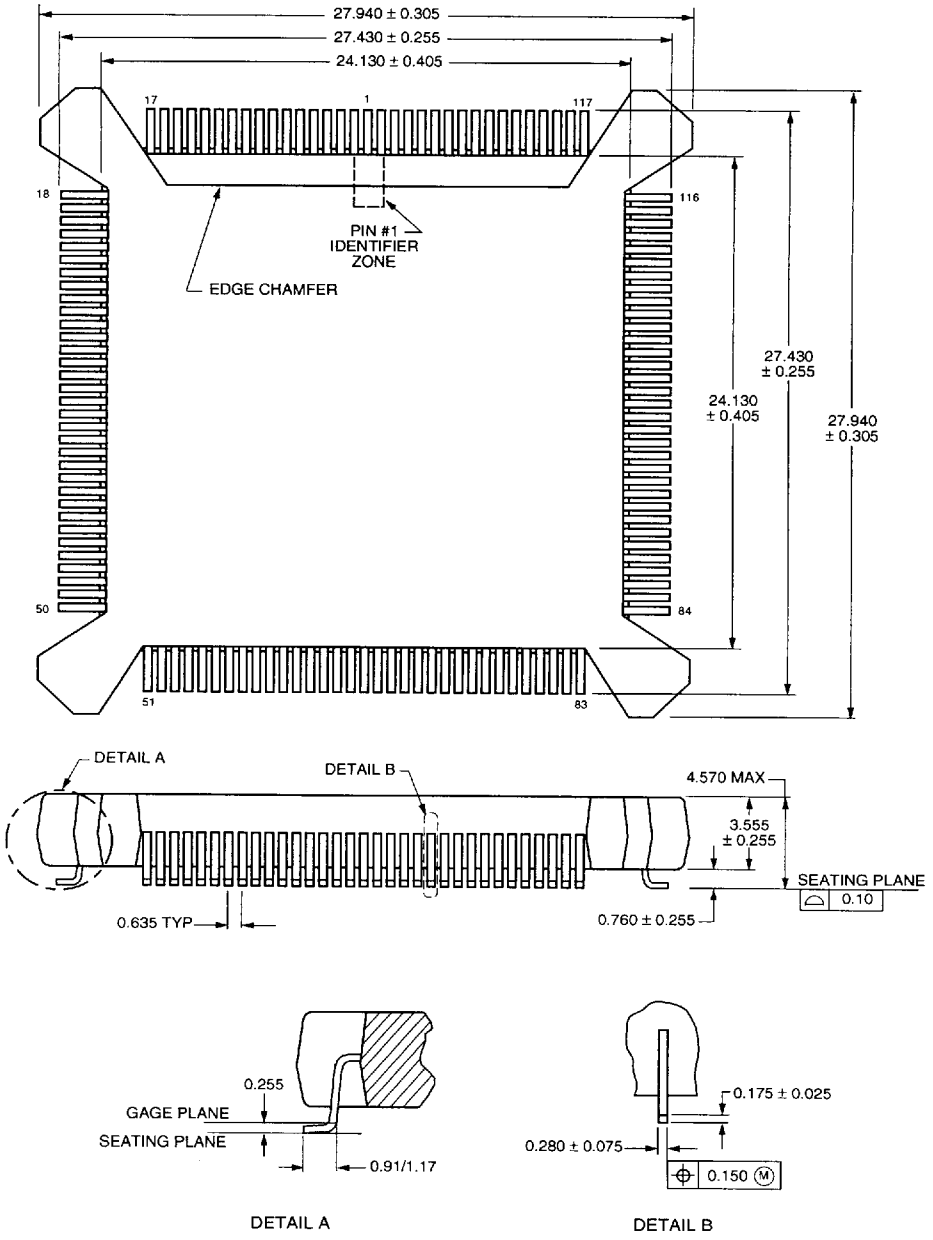


Figure 24. Network Port Synchronous Mode Timing

Outline Diagram

132-Pin JEDEC BQFP/BQFPH

Dimensions are in millimeters.



5-2586r9

Ordering Information

Device Code	Package	Temperature
T-7903 - - - FC	132-Pin JEDEC BQFP	0 °C to 70 °C

Appendix A. Application Examples

The ISA-MWAC supports various combinations of BRI and synchronous serial modes. The examples below summarize some typical configurations. Table A-1 shows the network port pin assignments for the examples.

TA Mode 1

Figure A-1 shows a configuration using one BRI port and two synchronous serial ports. NP0 is set up as a TE; NP1 and NP2 are synchronous ports configured in master timing mode (they generate timing for the external terminal equipment). An example of this application would be connecting video terminal equipment over two SW56 or SW64 connections to the ISDN.

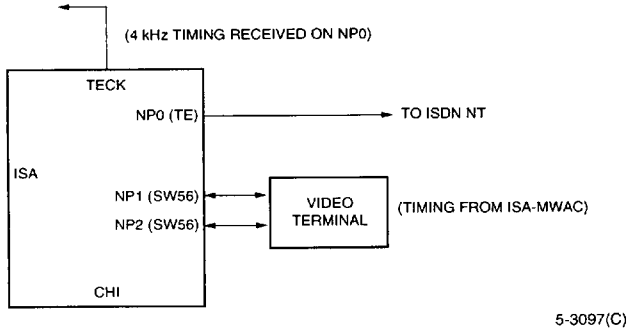


Figure A-1. TA Mode 1 Example

TA Mode 2

Figure A-2 shows an application using one BRI port and two synchronous slave ports. NP0 and NP1 receive timing from two SW56 CSU/DSUs. NP2 is an NT port used for connection to ISDN terminal equipment.

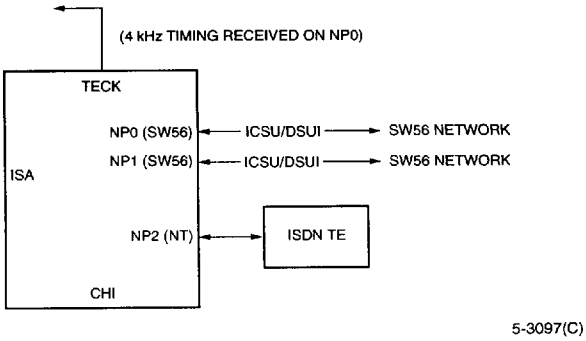


Figure A-2. TA Mode 2 Example

Table A-1. Pin Assignments for Network Ports

BRI Mode	Synchronous Mode	TA Mode 1	TA Mode 2
NP0_PT(O)	SND0 (O)	NP0_PT(O)	SND0 (O)
NP0_NT(O)	ST0 (I)	NP0_NT(O)	ST0 (I)
NP0_PR(I)	RD0 (I)	NP0_PR(I)	RD0 (I)
NP0_NR(I)	RT0 (I)	NP0_NR(I)	RT0 (I)
NP1_PT(O)	SND1 (O)	SND1 (O)	SND1 (O)
NP1_NT(O)	ST1 (I)	ST1 (O)	ST1 (I)
NP1_PR(I)	RD1 (I)	RD1 (I)	RD1 (I)
NP1_NR(I)	RT1 (I)	RT1*(I)	RT1 (I)
NP2_PT(O)	SND2 (O)	SND2 (O)	NP2_PT(O)
NP2_NT(O)	ST2 (I)	ST2 (O)	NP2_NT(O)
NP2_PR(I)	RD2 (I)	RD2 (I)	NP2_PR(I)
NP2_NR(I)	RT2 (I)	RT2*(I)	NP2_NR(I)

* RT1 should be connected to ST1. RT2 should be connected to ST2.

Note: SND = send data; ST = send timing; RD = receive data; RT = receive timing.

Appendix B. ISA-MWAC CHI Translation Table

Programming ISA-MWAC CHI in Accordance with Lucent's CHI Specification

ISA-MWAC CHI settings can be mapped to Lucent's *Concentration Highway Interface (CHI) Specification.*

In order to implement CHI, the options shown in Table B-1 are required.

Table B-1. CHI Implementation Options

The ISA-MWAC supports the double-clocking mode described in the CHI document.

Symbol	Name/Description
FE	**Frame Edge.** Indicates on which edge of the data clock the frame sync pulse is sampled. For the ISA-MWAC, this is bit 12 of the Set CHI Global Mode command (see Commands section of this document). FE is set once globally for all transmit and receive time slots.
XCE	**Transmit Clock Edge.** XCE is normally set once globally for all transmit time slots by setting bit 2 of the Set CHI Data Mode command.
RCE	**Receive Clock Edge.** RCE is set once for all receive time slots by setting bit 6 of the Set CHI Data Mode command.

The bit offset (XBOFF/RBOFF) and time-slot (XTS/RTS) features described in the CHI specification are implemented in the ISA-MWAC via the CYCLE bits in the Time-Slot Descriptor field of the Define Time-Slot command (described in the Commands section of this document).

Table B-2 summarizes the CYCLE settings needed to get to the values presented in the CHI document. The CYCLE bits are accessed in bits 16—31 in the Time-Slot Descriptor field of the DTS command.

Table B-2. CYCLE Settings

CHI Settings				ISA-MWAC Settings		
FE	XCE	XBOFF	CET	FE	XCE	CYCLE
0	0	000	4	0	0	1
0	1	000	3	0	1	1
1	0	000	3	1	0	1
1	1	000	4	1	1	2
FE	RCE	RBOFF	CER	FE	RCE	CYCLE
0	0	000	4	0	0	1
0	1	000	3	0	1	1
1	0	000	3	1	0	1
1	1	000	4	1	1	2

The major difference here is in choosing an exact count of CYCLE rather than the XBOFF—XTS and RBOFF—RTS combinations used in the CHI document. By definition, one CYCLE = two edges.

Appendix C. Programming Examples

Introduction

The following programming example shows how to configure the T7903 to pass the ISDN B1 and B2 channels between network port 0 and the CHI. An example of an application using this configuration would be videoconferencing over two B channels. Although this is a simple application using only a single network port and serial-to-serial data transfer on the B channels, many important programming details are illustrated. Programming the ISA-MWAC for multiple network port operation, HDLC data formatting on the B channels, or other functions would involve simple extensions of the example.

The example requires two long data pipes for the transmit and receive D channel and four short pipes for the B channels. The D-channel data is passed between data buffers in DRAM and the D-channel bits at the NP0 physical interface. The B channels are passed between time slots on the CHI and NP0. The CHI is configured to operate at 4.096 MHz in master mode.

Initial Setup of the Data Pipes, Creating the Linked Lists, and Activating the Network Port

The function `chi_to_np0()` would be called after initializing the Plug and Play ISA interface. It is used to initialize the data pipes and linked lists, and to activate the BRI interface. The first thing that this function does is to place a D-channel receive descriptor into DRAM at location 0x420. This descriptor points to a buffer (via the RBA field) at location 0x1000 (100 bytes are allocated to this buffer). The function `write_dram_word()` is used to place this and all other memory structures into DRAM using 16-bit ISA I/O accesses.

Next, a command queue (a list of T7903 commands) is placed into DRAM starting at address 0x00000 (location 0x00000 is not mandatory—all data structures can be placed anywhere in DRAM). The command queue begins with an IIQ command that initializes an interrupt queue starting at DRAM location 0x00100. Next, the data pipes for all channels are set up via six SDP commands (one SDP command for each channel, for both transmit and receive directions). The SDP commands can be put in the command queue in any order. These SDPs assign modes for each pipe, set pipe direction (DIR = 1 for transmit from DRAM or fixed data to a serial interface; DIR = 0 for receive from a serial interface to DRAM, fixed data interrupt or another serial interface), and provide a pointer to a transmit or receive descriptor in DRAM. The transmit data destined for the NP0 D channel must use long pipe 1, as outlined in the Linked Lists and Anchor Pipes section. Thus, the first SDP selects HDLC—D-channel mode for pipe 1 (HDLC—D mode is required for proper operation of the D channel transmitter's contention resolution mechanism in passive bus configurations). The D-channel data received from NP0 must use long pipe 0 in HDLC mode (not HDLC—D mode). Any other pipes (short or long) can be used for the serial-to-serial B-channel data. In this example, short pipes 17 and 18 carry B-channel data from the CHI to NP0 (to the network), and short pipes 23 and 24 are used to carry the B-channel data received from NP0 to the CHI. Note that all the SDP commands have CLR = 1 programmed. Setting CLR = 1 clears the pipe and is required the first time any pipe is set up. Also note that all the transmit and receive descriptor pointers are null, except for the D-channel receive (pipe 0) SDP. A null transmit descriptor pointer is used when there is presently no data to transmit (as in the case of pipe 0—the D-channel transmit pipe), or if the pipe is serial-to-serial (pipes 17, 18, 23, and 24) or fixed data-to-serial.

The DTS commands in `chi_to_np0()` define the linked lists required for the CHI and NP0. A separate linked list is needed for each serial interface used and for each direction (transmit and receive). Therefore, four DTS lists are required for the example. As described in the Linked Lists and Anchor Pipes section and DTS command description, each list starts with an anchor pipe that is dedicated to a particular interface and direction. This specific association between an interface and its anchor pipe is how all other linked pipes become associated to that interface. Unlike the SDPs, the order of DTS commands in the command queue (i.e., the order that they are executed by the ISA-MWAC) is very important. Each list must begin with the anchor pipe for that list (pipe 1 for the NP0 transmit direction, pipe 0 for the NP0 receive direction, and pipe 16 for both CHI transmit and receive). The subsequent DTS commands for each list must be in the order that the time slots occur on the interfaces. The linked list structures are formed from the PIPE and Previous In/Out Pipe fields. The Next Pipe field of each DTS command points to the list's anchor pipe so that the current end of the list has a pointer to the beginning as the DTS commands are first executed by the T7903. One point to note is that pipe 16, the anchor pipe for the CHI, needs no time-slot descriptor LEN, CYCLE, and DI fields because this pipe does not carry data; it only anchors the CHI DTS command list. These fields are ignored by the T7903 and can be null.

Appendix C. Programming Examples
(continued)

Initial Setup of the Data Pipes, Creating the Linked Lists, and Activating the Network Port (continued)

The next command in the queue is a CGM command, which sets up global parameters for the CHI. In this example, CHICM = 3 sets up the CHI as a master (CHICKOUT and CHIFS are outputs) with a CHICKOUT rate of 4.096 MHz. The CHIFS signal is driven on the rising edge of CHICKOUT (FD = 1), and CHICKOUT runs continuously (BPF = 0).

Next is the pause command, used after all SDP, SSP, DTS, and CGM commands, and then the NP0 command. This command puts NP0 in BRI mode (NPMODE = 0) and configures it as a TE (ISNT = 0). The ACT bit is set to 1, which will cause the network port to initiate activation with the network (send INFO 1). Typical TE-mode programming is used for the following bits: TLEVEL = 0, EZOBS = 0, RLEVEL = 0, FBIT = 1, NBF = 0, FT = 0, EZ = 0, IFA = 0, and FACT = 0. No loopbacks are invoked.

The next command is the CDM command, which completes the CHI setup. The CHI is enabled (XEN = 1 and REN = 1) and single-clock mode is selected (CMST = 0 and CMSR = 0). The falling CHICKOUT edge is selected for data reception (RCE = 0) and the rising edge is selected for transmission (XCE = 1).

The final command in the example's command queue is the WAIT command. Once instructed to begin command queue execution, the T7903 will continue to execute commands until it hits the WAIT command. Upon processing WAIT, command execution is halted and the P bit in register IP0 (bit 15) is cleared to 0.

After placing the command queue into DRAM, execution is begun by writing the ISA-MWAC's internal command queue pointer with the address in DRAM at which the queue starts. This is done by the `write_cqp()` function. See The Staging Area: Accessing the Command Queue Pointer section of this document for more information.

After command queue execution, the pipes and linked lists are fully configured and interrupts will be queued as they occur. The serial interfaces are now ready to be turned on. This is accomplished by the last line of code in `chi_to_np0()`. By writing a 1 to the CHI and NP0 bits in IP0 (bits 4 and 5), the two interfaces' programmed configuration will take effect and they will activate. Since a receive buffer has been set up for the D channel and the Receive Buffer Ready Interrupt has been enabled in the receive descriptor, packets received from the network will be buffered and the host will be interrupted.

```
/* ************************************************************************** */
/* chi_to_np0() connects CHI time slots 0 and 1 to NP0 channels B1            */
/* and B2. NP0 is configured as a TE. The following pipes are used:           */
/*    CHANNEL              TRANSMIT PIPE                RECEIVE PIPE          */
/*   D channel      PIPE 1 (long - HDLC-D mode)     PIPE 0 (long - HDLC mode)  */
/*   B1 channel     PIPE 17 (sht - ser. to ser.)    PIPE 23 (sht - ser. to ser.) */
/*   B2 channel     PIPE 18 (sht - ser. to ser.)    PIPE 24 (sht - ser. to ser.) */
/* Cmds are put in DRAM starting at 0x00000.                                  */
/* The CHI is setup as 4.096 MHz master. BPF = 0 (CHICKOUT is continuous clk). */
/* ************************************************************************** */
void chi_to_np0(void)
{
            long int cq_start = 0;
            long int i = 0;
            int bfsize = 100, j, rba_word0, rba_word1, nda_word0, nda_word1;

            rda = 0x420L;           /* receive descriptor address */
            rba = 0x1000L;          /* receive buffer address */
            nda = 0x420L;           /* next descriptor address */
            rba_word0 = rba & 0x0ffff;
            rba_word1 = (rba >> 16) & 0x0000f;
            nda_word0 = nda & 0x0ffff;
            nda_word1 = (nda >> 16) & 0x0000f;
```

Appendix C. Programming Examples (continued)

Initial Setup of the Data Pipes, Creating the Linked Lists, and Activating the Network Port (continued)

```
/* write receive descriptor to DRAM */
            write_dram_word(i = rda, 0);        /* clear 1st 4 bytes */
            write_dram_word(i = i + 2, 0);
            write_dram_word(i = i + 2, rba_word0);
            write_dram_word(i = i + 2, rba_word1);
            write_dram_word(i = i + 2, nda_word0);
            write_dram_word(i = i + 2, nda_word1);
            write_dram_word(i = i + 2, 0x8000 | (bfsize & 0x1fff);/* RBRDYEN = 1 */
            write_dram_word(i = i + 2, 0);

/* clear the receive buffer space in DRAM */
            for(j = 0; j < bfsize/2; j = j + 2)
                        write_dram_word(rba + j, 0);


/* write IIQ command to DRAM - IIQ pointer = 0x00100 */
            write_dram_word(i = cq_start, 0x0000);
            write_dram_word(i = i + 2, 0x3000);
            write_dram_word(i = i + 2, 0x0100);
            write_dram_word(i = i + 2, 0x0000);

/* write SDP command words to DRAM for D channel tx - PIPE 1 */
/* MODE = HDLC - D channel, pointer to TD = null*/
            write_dram_word(i = i + 2, 0x7481);/* LONG PIPE 1, CLR = 1, DIR = 1 */
            write_dram_word(i = i + 2, 0x5000);
            write_dram_word(i = i + 2, 0x0000);/* null TD pntr */
            write_dram_word(i = i + 2, 0x0000);

/* write SDP command words to DRAM - PIPE 17, MODE = serial-to-serial,*/
/* This is used for connecting CHI TS0 rx to NP0 B1 channel tx. */
            write_dram_word(i = i + 2, 0x8091);/* SHRT PIPE 17, CLR = 1, DIR = 0 */
            write_dram_word(i = i + 2, 0x5000);
            write_dram_word(i = i + 2, 0x0000);/* null pntr */
            write_dram_word(i = i + 2, 0x0000);

/* write SDP command words to DRAM - PIPE 18, MODE = serial-to-serial,*/
/* This is used for connecting CHI TS1 rx to NP0 B2 channel tx. */
            write_dram_word(i = i + 2, 0x8092);/* SHRT PIPE 18, CLR = 1, DIR = 0 */
            write_dram_word(i = i + 2, 0x5000);
            write_dram_word(i = i + 2, 0x0000);/* null pntr */
            write_dram_word(i = i + 2, 0x0000);

/* write SDP command words to DRAM for D channel rx - PIPE 0 */
/* MODE = HDLC, pointer to RD = null                         */
            write_dram_word(i = i + 2, 0x4480);/* LONG PIPE 0, CLR = 1, DIR = 0 */
            write_dram_word(i = i + 2, 0x5000);
            write_dram_word(i = i + 2, rda & 0x0ffff);/* pntr to RD */
            write_dram_word(i = i + 2, (rda >> 16) & 0x0000f);
```

Appendix C. Programming Examples (continued)

Initial Setup of the Data Pipes, Creating the Linked Lists, and Activating the Network Port (continued)

```
/* write SDP command words to DRAM - PIPE 23, MODE = serial-to-serial,*/
/* This is used for connecting NP0 B1 channel rx to CHI TS0 tx.*/
            write_dram_word(i = i + 2, 0x8097);/* SHRT PIPE 23, CLR = 1, DIR = 0 */
            write_dram_word(i = i + 2, 0x5000);
            write_dram_word(i = i + 2, 0x0000);/* null pntr */
            write_dram_word(i = i + 2, 0x0000);

/* write SDP command words to DRAM - PIPE 24, MODE = serial-to-serial,*/
/* This is used for connecting NP0 B2 channel rx to CHI TS1 tx.*/
            write_dram_word(i = i + 2, 0x8098);/* SHRT PIPE 24 */
            write_dram_word(i = i + 2, 0x5000);
            write_dram_word(i = i + 2, 0x0000);/* null pntr */
            write_dram_word(i = i + 2, 0x0000);

/* NP0 linked list for TX direction: PIPE 1 (D) -> PIPE 17 (B1) -> PIPE 18 (B2) */
/* write DTS command words to DRAM for D channel tx */
            write_dram_word(i = i + 2, 0x8021);/* PREV OUT PIPE = PIPE = 1 */
            write_dram_word(i = i + 2, 0x7011);/* VI = 0, VO = 1 */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x4001);/* NEXT OUT PIPE = 1 */
            write_dram_word(i = i + 2, 0x0204);/* LEN = 2, CYCLE = 17 */

/* write DTS command words to DRAM for B1 channel tx (PIPE 17) */
            write_dram_word(i = i + 2, 0x8031);/* P. O. PIPE = 1; PIPE = 17 */
            write_dram_word(i = i + 2, 0x7011);/* VI = 0, VO = 1 */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x0001);/* NEXT OUT PIPE = 1 */
            write_dram_word(i = i + 2, 0x0800);/* LEN = 8, CYCLE = 0 */

/* write DTS command words to DRAM for B2 channel tx (PIPE 18) */
            write_dram_word(i = i + 2, 0x8232);/* P. O. PIPE = 17; PIPE = 18 */
            write_dram_word(i = i + 2, 0x7011);/* VI = 0, VO = 1 */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x0001);/* NEXT OUT PIPE = 1 */
            write_dram_word(i = i + 2, 0x0802);/* LEN = 8, CYCLE = 8 */
```

Appendix C. Programming Examples (continued)

Initial Setup of the Data Pipes, Creating the Linked Lists, and Activating the Network Port (continued)

```
/* NP0 linked list for RX direction: PIPE 0 (D) -> PIPE 23 (B1) -> PIPE 24 (B2) */
/* write DTS command words to DRAM for D channel rx */
            write_dram_word(i = i + 2, 0x8000);/* PREV IN PIPE = PIPE = 0 */
            write_dram_word(i = i + 2, 0x7012);/* VI = 1, VO = 0 */
            write_dram_word(i = i + 2, 0x4000);/* NEXT IN PIPE = 0 */
            write_dram_word(i = i + 2, 0x0204);/* LEN = 2, CYCLE = 17 */
            write_dram_word(i = i + 2, 0x0000);/* output fields = null */
            write_dram_word(i = i + 2, 0x0000);/* output fields = null */

/* write DTS command words to DRAM for B1 channel rx (PIPE 23) */
            write_dram_word(i = i + 2, 0x8017);/* PREV IN PIPE = 0; PIPE = 23 */
            write_dram_word(i = i + 2, 0x7012);/* VI = 1, VO = 0 */
            write_dram_word(i = i + 2, 0x0000);/* NEXT IN PIPE = 0 */
            write_dram_word(i = i + 2, 0x0800);/* LEN = 8, CYCLE = 0 */
            write_dram_word(i = i + 2, 0x0000);/* output fields = null */
            write_dram_word(i = i + 2, 0x0000);/* output fields = null */

/* write DTS command words to DRAM for B2 channel rx (PIPE 24) */
            write_dram_word(i = i + 2, 0xdc18);/* PREV IN PIPE = 23; PIPE = 24 */
            write_dram_word(i = i + 2, 0x7012);/* VI = 1, VO = 0 */
            write_dram_word(i = i + 2, 0x0000);/* NEXT IN PIPE = 0 */
            write_dram_word(i = i + 2, 0x0802);/* LEN = 8, CYCLE = 8 */
            write_dram_word(i = i + 2, 0x0000);/* output fields = null */
            write_dram_word(i = i + 2, 0x0000);/* output fields = null */

/* CHI linked list for TX direction: PIPE 16 -> PIPE 23 (TS0) -> PIPE 24 (TS1) */
/* write DTS cmd. words to DRAM for CHI anchor pipe tx (PIPE 16); TSMODE = anchor */
            write_dram_word(i = i + 2, 0x8210);/* PREV OUT PIPE = 16; PIPE = 16 */
            write_dram_word(i = i + 2, 0x7011);/* VI = 0, VO = 1 */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x1c10);/* NXT OUT PIPE = 16, TSMODE = anch */
            write_dram_word(i = i + 2, 0x0000);/* TSD fields LEN & CYCLE = null*/

/* write DTS cmd. words to DRAM for CHI time slot 0 tx (PIPE 23) */
            write_dram_word(i = i + 2, 0x8217);/* P. O. PIPE = null; PIPE = 23 */
            write_dram_word(i = i + 2, 0x7011);/* VI = 0, VO = 1 */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x0000);/* input fields = null */
            write_dram_word(i = i + 2, 0x0010);/* NEXT OUT PIPE = 16 */
            write_dram_word(i = i + 2, 0x0800);/* LEN = 8, CYCLE = 0 */
```

Appendix C. Programming Examples (continued)

Initial Setup of the Data Pipes, Creating the Linked Lists, and Activating the Network Port (continued)

```
/* write DTS command words to DRAM for CHI time slot 1 tx (PIPE 24) */
    write_dram_word(i = i + 2, 0x82f8);/* P. O. PIPE = null; PIPE = 24 */
    write_dram_word(i = i + 2, 0x7011);/* VI = 0, VO = 1 */
    write_dram_word(i = i + 2, 0x0000);/* input fields = null */
    write_dram_word(i = i + 2, 0x0000);/* input fields = null */
    write_dram_word(i = i + 2, 0x0010);/* NEXT OUT PIPE = 16 */
    write_dram_word(i = i + 2, 0x0802);/* LEN = 8, CYCLE = 8 */

/* CHI linked list for RX direction: PIPE 16 -> PIPE 17 (TS0) -> PIPE 18 (TS1) */
/* write DTS cmd. words to DRAM for CHI anchor pipe tx (PIPE 16) TSMODE = anchor */
    write_dram_word(i = i + 2, 0xc010);/* PREV IN PIPE = 16; PIPE = 16 */
    write_dram_word(i = i + 2, 0x7012);/* VI = 1, VO = 0 */
    write_dram_word(i = i + 2, 0x1c10);/* NXT IN PIPE = 16, TSMODE = anch */
    write_dram_word(i = i + 2, 0x0000);/* TSD fields LEN & CYCLE = null*/
    write_dram_word(i = i + 2, 0x0000);/* output fields = null */
    write_dram_word(i = i + 2, 0x0000);/* output fields = null */

/* write DTS command words to DRAM for CHI time slot 0 rx (PIPE 17) */
    write_dram_word(i = i + 2, 0xc011);/* PREV IN PIPE = 16; PIPE = 17 */
    write_dram_word(i = i + 2, 0x7012);/* VI = 1, VO = 0 */
    write_dram_word(i = i + 2, 0x0010);/* NEXT IN PIPE = 16 */
    write_dram_word(i = i + 2, 0x0800);/* LEN = 8, CYCLE = 0 */
    write_dram_word(i = i + 2, 0x0000);/* output fields = null */
    write_dram_word(i = i + 2, 0x0000);/* output fields = null */

/* write DTS command words to DRAM for CHI time slot 1 rx (PIPE 18) */
    write_dram_word(i = i + 2, 0xc412);/* PREV IN PIPE = 17; PIPE = 18 */
    write_dram_word(i = i + 2, 0x7012);/* VI = 1, VO = 0 */
    write_dram_word(i = i + 2, 0x0010);/* NEXT IN PIPE = 16 */
    write_dram_word(i = i + 2, 0x0802);/* LEN = 8, CYCLE = 0 */
    write_dram_word(i = i + 2, 0x0000);/* output fields = null */
    write_dram_word(i = i + 2, 0x0000);/* output fields = null */

/* write CGM command words to DRAM */
/* OD = 0, FE = 0, FD = 1, BPF = 0, FSI = 0, STECK = 1, CHICM = 3 */
/* BPF = 0 causes CHICKOUT to run continuously */
    write_dram_word(i = i + 2, 0x0800);
    write_dram_word(i = i + 2, 0x9203);

/* write PAUSE command words to DRAM */
    write_dram_word(i = i + 2, 0x0000);
    write_dram_word(i = i + 2, 0x1000);

/* write NP0 command bytes to DRAM */
    write_dram_word(i = i + 2, 0x4201);/* IRM0 = 1, ISNT = 0, ABVI = 1, ACT = 1 */
    write_dram_word(i = i + 2, 0xb002);/* FBIT = 1, EZOBS = 0, NPMODE = 0 */
```

Appendix C. Programming Examples (continued)

Initial Setup of the Data Pipes, Creating the Linked Lists, and Activating the Network Port (continued)

```
/* write CDM command bytes to DRAM */
/* RPIN = 0, RCE = 0, CMSR = 0, CMST = 0, XCE = 1, XEN = 1, REN = 1 */
            write_dram_word(i = i + 2, 0x0007);
            write_dram_word(i = i + 2, 0xe000);

/* write WAIT command bytes to DRAM */
            write_dram_word(i = i + 2, 0x0000);
            write_dram_word(i = i + 2, 0x0000);

/* write cqp to loc of cmd queue to begin command execution */
            write_cqp(cq_start);

            outport(IP0,0x0130);    /* set BO, NP0 and CHI bits in IP0 */
}

/* ********************************************************************** */
/* write_cqp() writes the command queue ptr (located in the T7903's      */
/* internal staging area) with the starting DRAM address of the queue.   */
/* ********************************************************************** */
void write_cqp(long int cq_addr)
{
            int cq_addr_lower16, cq_addr_upper4;
            cq_addr_lower16 = cq_addr & 0x0ffff;
            cq_addr_upper4 = (cq_addr >> 16) & 0x0000f;
            outport(IP5, 0x0040);   /* address of cqp in staging area */
            outport(IP6, 0x6000);   /* enable staging area access */
            outport(IP7, cq_addr_lower16);/* write lower 16 bits of cqp */
            outport(IP7, cq_addr_upper4);/* write upper 16 bits of cqp */
}
```

Appendix C. Programming Examples (continued)

Transmitting a D-Channel Packet

The `transmit_d_packet()` function is used to send a D-channel packet to the network. First, the transmit descriptor (TD) is loaded into DRAM. The descriptor enables the transmit of frame completed (TFC) interrupt and instructs the ISA-MWAC to transmit idles (1s) after sending the packet. The EOF bit is set to tell the ISA-MWAC that this is the only descriptor and data buffer to use for this packet. Next, the data (passed to the function in an array) is loaded into DRAM at the transmit buffer address (TBA). Finally, a new command list consisting of SDP, PAUSE, and WAIT commands is executed. The new pipe 1 SDP overrides the SDP executed in `chi_to_np0()`, and points the ISA-MWAC to the transmit descriptor of the packet to be sent. Note that the pipe does not need to be cleared, since it was cleared in `chi_to_np0()`. Also note that PTR = 1 to indicate that the TD pointer is valid. Upon execution of the new commands, the D-channel packet will be transmitted. The host will be interrupted when the frame has been transferred from internal RAM to the NP0 serial transmit register (see the Interrupts section for more details).

```
/* ********************************************************************** */
/* transmit_d_packet() transmits bcnt bytes from the passed array in a    */
/* single D-channel packet. The transmit descriptor is placed at 0x400.   */
/* The transmit buffer is placed at 0x500.                                */
/* ********************************************************************** */
void transmit_d_packet(int *data, bcnt)
{
          INT pclass_fcnt = 0;/* PCLASS = 0 (D-channel priority = high) */
          int i = 0, j;
          long int tda, tba, nda;
          int tba_word0, tba_word1, nda_word0, nda_word1;
          long int cq_start = 0;/* put the command queue at loc 0 in DRAM */

          nda = 0;                  /* next descriptor address = null */
          tda = 0x400;              /* transmit descriptor DRAM address = 0x400 */
          tba = 0x500;              /* transmit buffer DRAM address = 0x500 */

          tba_word0 = tba & 0x0ffff;
          tba_word1 = (tba >> 16) & 0x0000f;
          nda_word0 = nda & 0x0ffff;
          nda_word1 = (nda >> 16) & 0x0000f;

   /* write transmit descriptor to DRAM */
          write_dram_word(tda, 0xa000 | pclass_fcnt);/* TFCEN = 1, IDL = 1 */
          write_dram_word(tda + 2, 0x8000 | bcnt);/* EOF = 1, DCRC = 0, EOL = 0 */
          write_dram_word(tda + 4, tba_word0);
          write_dram_word(tda + 6, tba_word1);
          write_dram_word(tda + 8, nda_word0);
          write_dram_word(tda + 10, nda_word1);
          write_dram_word(tda + 12, 0);        /* clear status */
          write_dram_word(tda + 14, 0);

   /* write data into transmit data buffer in DRAM */
          for(j=0; j<bcnt; j++)
                    write_dram_byte(tba + j, data[j]);
```

Appendix C. Programming Examples (continued)

Transmitting a D-Channel Packet (continued)

```
/* place commands into DRAM to transmit D-channel packet */
/* write SDP command bytes to DRAM for D-channel tx */
            write_dram_word(cq_start, 0x7401);  /* PIPE = 1 */
            write_dram_word(i = i + 2, 0x5000); /* CMDI, EOL, IBEG, IEND ints off */
            write_dram_word(i = i + 2, tda & 0x0ffff);/* pntr to TD */
            write_dram_word(i = i + 2, (tda >> 16) & 0x0000f);/* pntr to TD */

/* write PAUSE command words to DRAM */
            write_dram_word(i = i + 2, 0x0000);
            write_dram_word(i = i + 2, 0x1000);

/* write WAIT command bytes to DRAM */
            write_dram_word(i = i + 2, 0x0000);
            write_dram_word(i = i + 2, 0x0000);

/* execute commands to send packet */
            write_cqp(cq_start);    /* write cqp to loc of cmd queue */

}
```

Appendix D. CHI Double Clock Mode and *MVIP* Compatibility

Introduction

The T7903's concentration highway interface (CHI) is highly configurable, allowing it to be used in many time division multiplexed (TDM) system buses. One TDM bus standard in wide use today is the Multi-Vendor Integration Protocol (*MVIP*). The *MVIP* bus is a multiplexed digital telephony highway consisting of eight serial TDM streams. Each of these serial streams is capable of carrying thirty-two 64 kbits/s channels, for a total of 2.048 Mbits/s per stream. To be fully compliant to the *MVIP* specification, support of all eight data streams is required. Many products support a subset of the full specification, and are considered *MVIP*-compatible. This appendix outlines the electrical and timing parameters that must be met for a T7903-based network card to be *MVIP*-compatible. Programming and connectivity information are provided. For more information, see the Multi-Vendor Integration Protocol Reference Manual (Natural Microsystems, 8 Erie Drive, Natick, Massachusetts, 01760-1339; Telephone: 508-650-1300).

Electrical and Timing Parameters of the *MVIP* Bus

This description will focus on the details required for interfacing to one of the *MVIP* 2.048 Mbits/s streams. The signals for data stream 0 of the *MVIP* bus are shown in Table D-1.

Table D-1. *MVIP* Signals for Data Stream 0

Signal Name	Description
DSo0	Serial Data Stream Out (to network)
DSi0	Serial Data Stream In (from network)
$\overline{F0}$	Frame Pulse
$\overline{C4}$	4.096 MHz Clock
C2	2.048 MHz Clock

Note that the signal naming conventions are relative to data flow on the network. Data destined for the network is driven onto *MVIP* signal DSo0, and data received from the network is driven on DSi0. The timing relationships for these signals are shown in Figure D-1. $\overline{F0}$ is the *MVIP* frame strobe, $\overline{C4}$ is a 4.096 MHz clock (2 periods per data bit), and C2 is a 2.048 MHz clock. Data from the network interface should be driven onto DSi0 on the rising edge of C2. The suggested sample point for data received from the *MVIP* bus on DSo0 is at the 75% point (the rising edge of $\overline{C4}$). Channel 0, the first of the 32 channels, begins on the first rising edge of C2 after the falling edge of $\overline{F0}$. Note the required phase relationship between C2 and $\overline{C4}$.

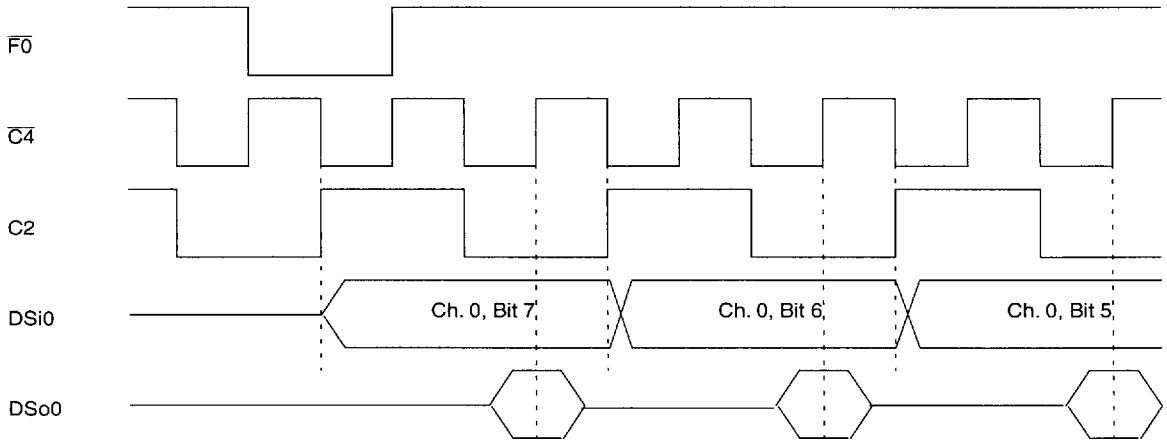


Figure D-1. *MVIP* Bus Timing

Appendix D. CHI Double Clock Mode and *MVIP* Compatibility (continued)

Electrical and Timing Parameters of the *MVIP* Bus (continued)

The MVIP specification gives other electrical and clocking requirements:

- Devices connected to *MVIP* bus lines must have electrical characteristics compatible with HCT-type high-speed logic devices.
- All outputs driving the *MVIP* bus must have 3-state capability and power up in a high-impedance condition. The data stream signals (DSix and DSox) should be pulled up to +5 V via 100 kΩ—1 MΩ resistors. These pull-ups must be located on any board that can source the clocks (*MVIP* master).
- No board may present more than a 20 pF load on any *MVIP* bus line.
- The C2 and $\overline{C4}$ clocks should have jumper-selectable 1000 Ω/1000 pF series terminations on all boards.
- Cards providing a network interface function should be capable of sourcing $\overline{F0}$, C2, and $\overline{C4}$ (*MVIP* master).
- Network cards that derive timing from the network should also operate as *MVIP* slaves. This supports multiple connections in which one card is chosen as the master and the others as slaves.

T7903 CHI Double Clock Mode

The *MVIP* bus uses a clock ($\overline{C4}$) that is two times the data rate (two clock cycles per bit). The CHI interface of the ISA-MWAC can be configured to operate in double clock mode, in which a bit is driven on CHIDX for two CHICKOUT/CHICKIN periods. Any CHICKOUT/CHICKIN edge can be chosen to sample the data received on CHIDR. Double clock mode is individually selected for the transmitter and receiver via the CMST and CMSR bits of the CDM command. Setting both of these bits to 1 will enable double clock mode.

The basic operation of the CHI is the same for both double clock mode and single clock mode (see the Concentration Highway Interface section for single clock mode operation). A time slot's location on the CHI and its length are described using the CYCLE and LEN fields in the DTS command. An important item to note concerning double clock mode is that the CYCLE and LEN fields still refer to single cycles of CHICKOUT/CHICKIN, not pairs of cycles. In other words, for an 8-bit time slot in a single clock mode system, LEN is programmed to 8, while in a double clock mode system, LEN is 16. CYCLE also refers to single periods of CHICKOUT/CHICKIN. For example, in a single clock mode CHI running with a CHICKOUT/CHICKIN rate of 2.048 MHz, there are 256 bits per frame, and thus there are 256 cycles, numbered from 0 to 255. In a double clock mode CHI running with a CHICKOUT/CHICKIN rate of 4.096 MHz, there are still 256 bits per frame, but there are 512 cycles numbered from 0 to 511.

Physical Connection of the CHI to the *MVIP* Bus

Figure D-2 shows the connection of the *MVIP* bus (data stream 0) to the CHI when the CHI is master.

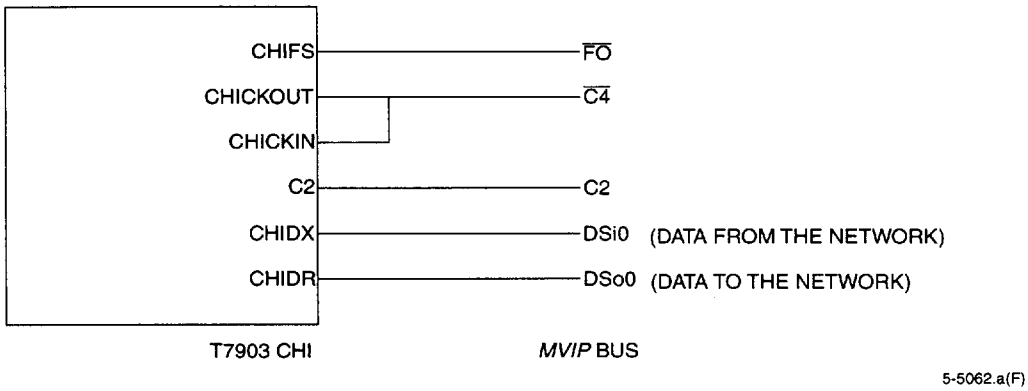


Figure D-2. Connecting the CHI Master to the *MVIP* Bus

Appendix D. CHI Double Clock Mode and *MVIP* Compatibility (continued)

Physical Connection of the CHI to the *MVIP* Bus (continued)

Note that CHICKOUT is connected to CHICKIN. Figure D-3 shows the CHI slave connection to the *MVIP* bus.

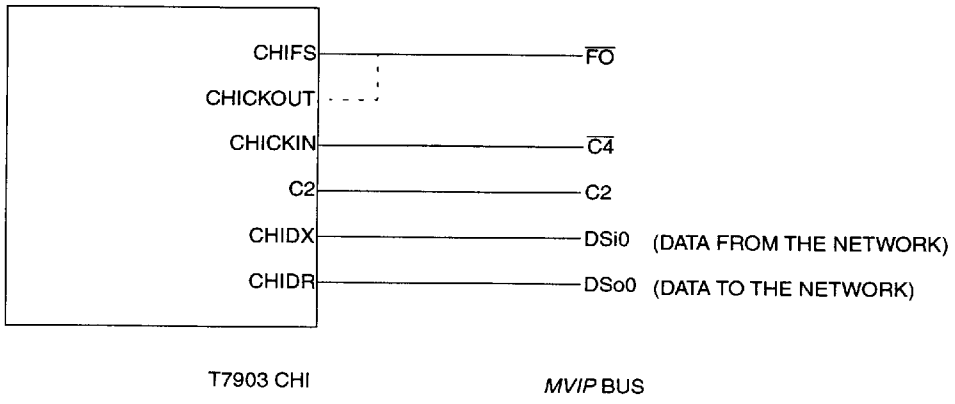


Figure D-3. Connecting the CHI Slave to the *MVIP* Bus

In CHI slave mode, CHICKOUT is not connected to the *MVIP* bus. Since CHICKOUT is 3-stated in CHI slave mode, it may be left connected to CHICKIN, allowing for software-programmable switching between slave and master modes.

Configuring the T7903 for *MVIP* Master Compatibility

The CHI interface of the ISA-MWAC can be configured for *MVIP* master compatibility. Table D-2 shows the required programming for fields in the CGM and CDM commands.

Table D-2. T7903 Programming for *MVIP* Master Compatibility

Command	Field	Bit Position	Value	Notes
CGM	FSI	26	1	Invert CHIFS
CGM	STECK	25	1	TECK is an output (SSYNC, bit 24 ignored)
CGM	CHICKM	23—16	0x3	Master mode: CHICKOUT = 4.096 MHz
CGM	OD	13	0	Active pull-up on CHIDX
CGM	FE	12	0	Sample CHIFS on falling edge of CHICKOUT
CGM	FD	11	1	Drive CHIFS on rising edge of CHICKOUT
CGM	BPF	10—0	0	CHICKOUT runs continuously
CDM	RPIN	7	0	Receive on CHIDR
CDM	RCE	6	1	Receive on the rising edge of CHICKOUT
CDM	CMSR	5	1	Receiver operates in double-clock mode
CDM	CMST	3	1	Transmitter operates in double-clock mode
CDM	XCE	2	0	Transmit on the falling edge of CHICKOUT
CDM	XEN	1	1	Transmitter enabled
CDM	REN	0	1	Receiver enabled

Appendix D. CHI Double Clock Mode and *MVIP* Compatibility (continued)

Configuring the T7903 for *MVIP* Master Compatibility (continued)

The exact programming of the CYCLE field of the DTS commands will depend on the *MVIP* channel being used. The LEN field will normally be 16 (8-bit time slots). In general, program the CYCLE field of the transmit time slot's DTS command to a value two cycles less than the CYCLE field of the receive time slot. For example, to transmit an 8-bit time slot in channel 0 of the *MVIP* bus, program the CYCLE field to 511 and the LEN field to 16. To receive an 8-bit time slot in channel 0 of the *MVIP* Bus, program CYCLE to 1 and LEN again to 16. To access *MVIP* channel 1, add 8 to the channel 0 CYCLE values. Thus, CYCLE = 7 for transmit (remember that cycles wrap back to 0 after 511) and CYCLE = 9 for receive. The process is the same for the other *MVIP* channels.

Configuring the T7903 for *MVIP* Slave Compatibility

Configuration of the CHI interface for *MVIP* slave compatibility is slightly different than master mode configuration. Table D-3 shows the required programming for fields in the CGM and CDM commands.

Table D-3. T7903 Programming for *MVIP* Slave Compatibility

Command	Field	Bit Position	Value	Notes
CGM	FSI	26	0	This bit has no function in slave mode
CGM	STECK	25	1	TECK is an output (SSYNC, bit 24 ignored)
CGM	CHICKM	23—16	0	Slave mode: 8 kHz frames
CGM	OD	13	0	Active pull-up on CHIDX
CGM	FE	12	0	Sample CHIFS on falling edge of CHICKIN
CGM	FD	11	X	This field is ignored in CHI slave mode
CGM	BPF	10—0	X	This field is ignored in CHI slave mode
CDM	RPIN	7	0	Receive on CHIDR
CDM	RCE	6	1	Receive on the rising edge of CHICKIN
CDM	CMSR	5	1	Receiver operates in double clock mode
CDM	CMST	3	1	Transmitter operates in double clock mode
CDM	XCE	2	0	Transmit on the falling edge of CHICKIN
CDM	XEN	1	1	Transmitter enabled
CDM	REN	0	1	Receiver enabled

The main difference is that master mode uses the frame strobe invert (FSI) bit of the CGM command, while for a slave mode CHI, this bit has no function. This affects CYCLE field selection because the T7903 will behave as if frames start on the rising edge of the frame strobe, but the *MVIP* will start them on the falling edge. As was the case for master mode, exact programming of the CYCLE fields of the DTS commands will depend on the *MVIP* channel being used, but the LEN field will normally be 16 (8-bit time slots). To transmit an 8-bit time slot in channel 0 of the *MVIP* bus, program the CYCLE field to 510 and the LEN field to 16. To receive an 8-bit time slot in channel 0 of the *MVIP* bus, program CYCLE to 0 and LEN again to 16. To access *MVIP* channel 1, again add 8 to the channel 0 CYCLE values. Thus, CYCLE = 6 for transmit and CYCLE = 8 for receive. The process is the same for the other *MVIP* channels.

Appendix E. Questions and Answers

Introduction

This section is intended to answer the most common questions that come up when designing with the T7903 ISA-MWAC.

Concentration Highway Interface (CHI)

Q1: Do CHICKOUT and C2 3-state when the CHI is in slave mode?

A1: Yes.

Q2: What is active polarity of CHIDXEN?

A2: CHIDXEN is active-high.

Q3: If multiple T7903s are used in a system, can the CHIs be connected?

A3: Yes. Use one ISA-MWAC in CHI master mode and the others in slave mode. Connect the master's CHIFS to the slave's CHIFS and connect the master's CHICKOUT to the slave's CHICKIN. Note that the master must have its CHICKOUT and CHICKIN pins connected together directly or through a buffer. Slaves do not need their CHICKOUT and CHICKIN pins connected. But, since CHICKOUT is 3-stated in slave mode, they may be. One of the network ports on the T7903 that is CHI master should be activated first to synchronize the CHIs to the network.

Q4: Can the CHI be operated in slave mode with all network ports configured as TEs? And, if so, how can the CHI timing be synchronized to the network timing?

A4: Yes, the CHI can be a slave when all network ports are TEs. To synchronize the CHI timing to the network, configure TECK as an output (CGM command, STECK = 1) and use it as the reference for an external phase-locked loop.

Q5: When used as an output, where is TECK derived from? What happens to TECK in the absence of a network clock?

A5: TECK is a 4 kHz signal that synchronizes to the first active TE interface (thus, to the network) or free-runs when no ports are active.

Q6: In my system, CHI local loopback works when XCE = 1 (transmit on positive clock edges) and RCE = 0 (receive on negative edges) in the CDM command, but not when these are reversed. Why?

A6: When programming the CHI to transmit on the rising clock edge (XCE = 1) and receive on the falling edge (RCE = 0), the CYCLE fields of the receive and transmit time slots (in the DTS commands) should be equal for local loopback to work properly. When reversing the transmit/receive edges (XCE = 0, RCE = 1), set the receive CYCLE field to a value one greater than the value used for the transmit CYCLE field.

Q7: Please explain more about the CHI timing depicted in Figures 7—14 (of the data sheet).

A7: The XCE and RCE bits select the clock edge (rising or falling) that data is to be transmitted and received on, respectively. In Figures 7—14, CYCLE 0 denotes the first clock cycle of a frame that can be chosen to begin transmission or reception of a time slot on. The actual position of CYCLE 0 (relative to CHIFS being sampled high) is determined by the particular choice of mode (master or slave) and FE (the clock edge that CHIFS is to be sampled with). In Figure 7, the choice of slave mode and FE = 1 sets up the interface such that CYCLE 0 always begins on the CHICKIN edge labeled 0. The CYCLE field in the time-slot descriptors (TSD) of the DTS command is then used to choose the CYCLE number that a time slot is to begin on. As an example, let's say that slave mode is used with FE = 1, XCE = 1, RCE = 0, and the CYCLE field of the Tx and Rx DTS commands programmed to two. The time-slot length for Tx and Rx time slots (determined by the LEN field of the TSD) is programmed to eight. Thus, an 8-bit time slot will be transmitted starting at the CHICKIN edge labeled 4 in Figure 7. The T7903 will expect to receive an 8-bit time slot, and will sample the data on eight consecutive falling CHICKIN edges beginning with the CHICKIN edge labeled 5 in Figure 9.

Appendix E. Questions and Answers

(continued)

Time Slots

Q8: What is the best procedure for changing the description of a time slot? For example, a channel is set up for 64 kbits/s and now must be changed to 56 kbits/s. Also, the DTS Insert bit says it will "Insert/Modify" a linked list. Does this mean that if a pipe is already in a linked list, the ISA-MWAC ignores the Previous and Next Pipe fields?

A8: When modifying a time slot, simply issue a new DTS command. The new DTS command must have valid Previous Pipe and Next Pipe fields such that the linked list is maintained. For instance, if modifying the B1 channel DTS in the list D--->B1--->B2, the new DTS command must have its Previous Pipe field pointing to the D pipe (anchor) and its Next Pipe field pointing to the B2 pipe.

Q9: Why was the fourth bullet item in "Restrictions on Time Slots" included in the list? Why would anyone ever try to start a time slot sooner than 0.975 µs after the start of the previous time slot?

A9: This is important at higher CHI rates when using short, adjacent time slots. For example, when running the CHI at 4.096 MHz (244 ns/bit), this limitation means that a time slot must be at least 4 bits long if the following time slot on the interface is to be directly adjacent to it.

Descriptors, DTS and SDP Commands, and Data Structures

Q10: How is the T7903 informed that a transmit descriptor is the last in a linked list of descriptors?

A10: The ISA-MWAC can be told that it has reached the end of a list of transmit descriptors (TDs) by two methods:

1) A null next descriptor address pointer (NDA)

2) EOL = 1 in a dummy descriptor.

If the null NDA method is used, the last descriptor in the TD should have valid data in its associated buffer and the NDA should be set to all 0s. If the EOL = 1 method is used, the last descriptor is a dummy descriptor used only to inform the ISA-MWAC that there is no more data to transmit. The EOL bit is set to 1 in this descriptor, and the associated data buffer is not used.

Q11: Why are there two methods to inform the ISA-MWAC that it has reached the end of a list of TDs?

A11: Transmit buffer management can be interrupt driven (via TFC or EOL interrupts) or dynamic. Dynamic buffer management can be used when the absolute highest data throughput rates are required. In this case, the host must maintain the data buffers without the luxury of waiting for a TFC interrupt, while avoiding underrun conditions (which will be flagged by EOL interrupts, if enabled). If the null NDA method described in the previous question is used, the possibility of a race condition exists because the NDA pointer is written by the host in two 16-bit accesses. As the transmission of the current buffer is completed, the ISA-MWAC will read the NDA. If, during dynamic buffer management, the host has completed writing only half of the NDA (one 16-bit access has been completed), the ISA-MWAC will read a corrupt NDA. To prevent this from happening, the EOL = 1 with dummy descriptor method should be used. The transmit buffer address (TBA) should be set up ahead of time, then all the host has to do is to clear the EOL bit (a single access) to dynamically link the new data with the previous descriptor.

Q12: When is the normal mode (PA = 0) of the CDP command used?

A12: The CDP command is an easy way of restarting a data pipe. For example, let's say that the D channel is set up and signalling with the network is beginning. After loading a transmit buffer with the first D-channel packet, place the descriptor in memory with a pointer to the buffer (TBA) and a null NDA. Then issue an SDP command to transmit the packet. To send the next packet, simply put a new descriptor and its data buffer in memory, overwrite the old descriptor's null NDA field with the new descriptor's address, and issue a CDP command for the pipe. The T7903 will reread the NDA pointer and transmit the new packet from the new buffer.

Appendix E. Questions and Answers
(continued)

Descriptors, DTS and SDP Commands, and Data Structures (continued)

Q13: If, after setting up a serial interface, I later want to add more SDP and DTS commands, do I need a PAUSE command after them?

A13: Yes.

Q14: Explain some more about buffer management for transmit buffers.

A14: The simplest way to manage transmit buffers is have a single transmit descriptor and buffer, with the data in the buffer always transmitted as a single HDLC frame (EOF is set to 1). This buffer can be up to 8 Kbytes in length. To do this, place the data and the transmit descriptor in DRAM with EOF = 1, a null NDA and BCNT equal to the number of bytes of data in the buffer. Execution of an SDP command for this descriptor will cause the data to be transmitted in a single HDLC frame. To send another frame, wait for the TFC interrupt (make sure it was enabled). Then simply refill the buffer, set BCNT to the correct size, and reissue the SDP command.

An alternate method would be to place a new TD (with null NDA and EOF = 1) and buffer in DRAM while waiting for the first frame to finish transmission (TFC interrupt). When the TFC interrupt occurs, overwrite the null NDA of the first TD with the address of a new descriptor and issue a CDP (Continue Data Pipe command). The ISA-MWAC will reread the first descriptor's NDA, then read the new TD and data and transmit the new frame. This has the advantage of allowing preparation of the second frame while the first transmits.

More complicated buffer management may be used when large files are to be transmitted or very high throughput is required. A single HDLC frame may span multiple buffers/descriptors by programming EOF = 0 in all but the last TD. Note that there is a risk of an underrun any time single frames span multiple transmit buffers and the buffers are serviced by the host while the frame is being transmitted. Dynamic buffer management can be used if the interframe delay associated with interrupt-driven operation is not acceptable. Again, depending on the application, the avoidance of underrun conditions may be important.

Q15: Provide some information on how ISDN call setup and teardown can be performed on the T7903.

A15: There are a few different ways to manage call setup and teardown on the ISA-MWAC, and the proper choice really depends on the application.

In all cases, channels must not be enabled until the D-channel protocol software has requested the channels from the network and the channels have been provided. The simplest arrangement is when all B channels are passed between the CHI and the network ports and can be enabled simultaneously after all calls are set up. In this case, use SDP and DTS commands to set up all channels on the network ports and CHI ahead of time. Then, when the channels have been allocated by the network, enable the CHI transmitter and receiver.

Dynamic allocation of B channels is also possible. In nonserial, data-only applications (all data is passed between DRAM and the network ports), use SDP and DTS commands to set up all channels on the network ports ahead of time as above, but use null descriptor pointers in the SDP commands. Then, as channels are provided by the network, load the transmit data buffers and descriptors, then execute SDPs with valid pointers to the new receive/transmit descriptors. Communication over the new channels will begin. When a channel is to be dropped, stop transmission by closing the final frame normally, and use a null NDA in the final descriptor. Make sure that the transmit descriptor has IDL = 1 (bit 13) so that all ones are sent to the network port (freeing up the B channel for other TEs on a passive bus).

Another method of dynamic channel allocation is provided using the DTS command to insert and delete time slots on an interface. A simple example using one TE-configured network port will help illustrate this. To begin call setup on one port, T7903 configuration must include at least the D-channel setup using SDP and DTS commands. The DTS linked lists could consist of only the D-channel DTS commands (one DTS for the transmit list and one for the receive list). Once a B channel is allocated by the network (say B2 for example), insert a B2 DTS command into each list, making sure the PIPE, Next Pipe, and Previous Pipe fields maintain list connectivity. Then, if B1 is to be added, insert this between the D and B2 pipes in the DTS command linked lists via PIPE, Next Pipe, and Previous Pipe fields. Note that the time slots must be placed in the list in the order that they occur on the interface. As the time slots are added, remember to set up the necessary pipes with SDP commands. To tear down a channel, B1 for example, use a DTS command to delete the B1 time slot/pipe by programming the I/D bit to 0. The pipes that are still in the list (D and B2) will automatically be adjusted by the T7903 to maintain their connectivity to each other. Note that only the first 4 bytes of the DTS command are used when deleting (the Next Pipe, Aux. Pipe, and TSD fields are ignored).

Appendix E. Questions and Answers
(continued)

ISA Interface

Q16: Are zero wait-state I/O accesses supported?

A16: No.

Q17: What ISA address bits do the $\overline{CS0}$ and $\overline{CS1}$ outputs decode and does that include $\overline{IOR}$ and $\overline{IOW}$ or can memory accesses also turn on the CS outputs?

A17: The $\overline{CS0}$ and $\overline{CS1}$ pins decode SA[0:9] and AEN only. Therefore, if extended I/O mode is enabled (PIO4 and 5 pulled high during Plug and Play initialization), any I/O or memory accesses that match the T7903's programmed 32-byte I/O range will cause one of the CS pins to assert low. These should be externally ORed with $\overline{IOR}$ and $\overline{IOW}$ if only I/O accesses are to be selected.

Q18: How can the T7903 be made to support 16-bit address decoding on the ISA interface?

A18: Use the circuit shown in Figure E-1 to negate the AEN signal when one of the higher-order address lines is a logic one. Note that the circuit also decodes the Plug and Play Write_Data port at address 0xa79.

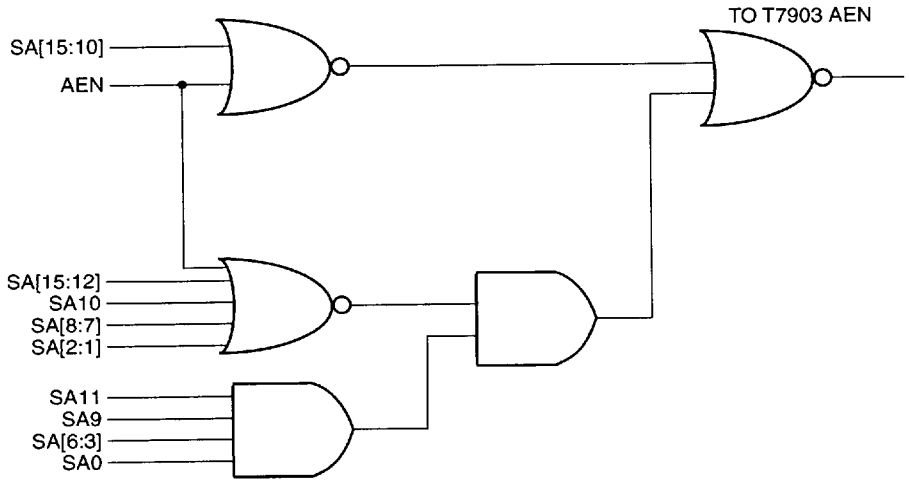


Figure E-1. Method for Supporting 16-bit Address Decoding

Q19: What does the T7903 internal address decode logic do with SA10 and SA11?

A19: Even though the Plug and Play specification provides for 10-bit decoding, SA10 and SA11 are still required to decode the Plug and Play write data port that is located at 0xa79. The T7903 decodes A11 and A10 only when Plug and Play is active. When ISA is active, the chip decodes 10 bits of address.

Q20: When using extended I/O chip select mode, how does the chip generate $\overline{IOCS16}$?

A20: $\overline{IOCS16}$ will assert in response to any access to the T7903's programmed I/O space. This space will take up 16 bytes in normal mode and 32 bytes in extended I/O chip select mode.

Q21: Any hints on using the T7903 with an embedded controller?

A21: Either 8- or 16-bit microprocessors will work. Note that the T7903 was designed for use in ISA systems that include byte-swapper circuitry. If using a 16-bit microprocessor, remember that the odd address ports of the T7903's ISA Plug and Play interface expect 8-bit accesses on the low order data pins (SD[7:0]). If the 16-bit microprocessor being used can't drive the low order data bus on odd address 8-bit accesses, then one of the following must be done. A byte-swapper circuit could be added which takes the high-order CPU data during 8-bit odd writes and places it on the low-order data pins of the T7903. On 8-bit reads to odd addresses, the circuit must take the low-order T7903 data and put it on the CPU's high-order data pins. Alternately, don't use CPU address pin A0, but connect CPU pin A1 to SA0 of the T7903. Connect A2 to SA1, A3 to SA2, etc. In this way, only even CPU addresses need to be used to access the T7903. Note that this method requires no external circuitry, but does double the address space requirements of the T7903.

In 8-bit systems, the T7903 must be informed that only 8-bit accesses are being performed. To do this, invert address line A0 from the processor and connect it to $\overline{SBHE}$. The address lines from the processor should connect to T7903 address pins A0—A11.

Appendix E. Questions and Answers (continued)

Network Ports

Q22: Can the T7903's network ports be directly connected to the S/T-interface of the Lucent Technologies T7256 (Single-Chip NT1 [SCNT1]) without transformers?

A22: Yes, as shown below. All resistors are 10%, 1/8 W. The same circuit should be used to connect to the T7234.

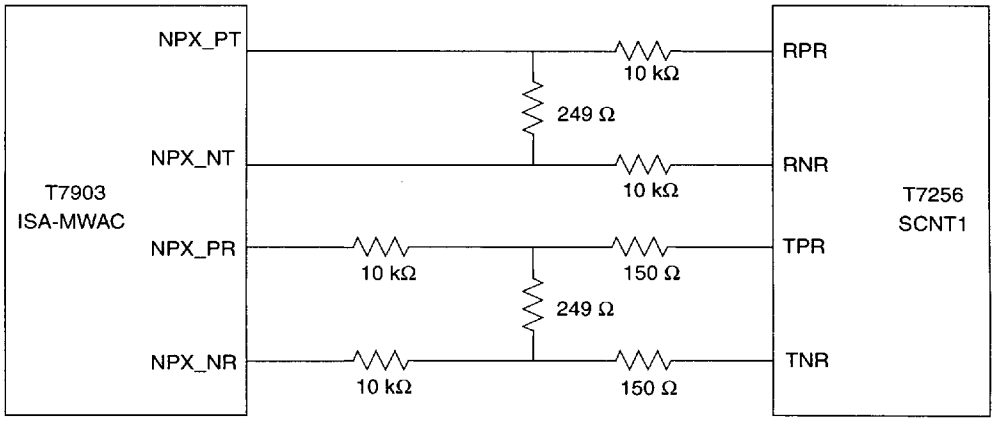


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Figure E-2. Direct Transformerless Connection of T7903 to T7256

Conformance Testing

Q23: For BRI conformance testing, what are the T7903 values for M (the number of good frames required to regain frame alignment) and N (the number of bad frames required to lose frame alignment)?

A23: N is selectable to be either 2 or 3 and M is 3.

Q24: Does the T7903 provide the T3 timer function?

A24: No, all timers must be implemented in software.

Q25: When a network port is configured as a TE, how should the NP bits in register IP0 and the ACT bit in the NP commands be used?

A25: The NP bits in IP0 must be set to allow the port to be activated by the network (respond to the reception of INFO 2 or INFO 4 with INFO 3) or to initiate a call (send INFO 1). The ACT bit in the NP command should be set to initiate a call (send INFO 1).

Q26: Please provide some hints on T3 implementation.

A26: When initiating a call, execute a command list with the ACT bit set in an NP command and enable the network by setting the appropriate NP in IP0 (if not already enabled). Start the software T3 timer, and execute another command clearing the ACT bit to 0. This does not stop transmission of INFO 1, but it will prevent unwanted activation attempts later. If the T7903 does not complete activation with the network in time (causing T3 to expire), clear the NP bit to cease transmission. Finally, set the NP bit to 1 again to prepare for future activation attempts.

Q27: After receiving INFO 2 from the network, the T7903 responds with INFO 3 but there is garbage data in the B1 and B2 channels. This causes some conformance tests to fail. What should be done?

A27: The network port B channels must be initially configured to send all 1s. This is accomplished through the use of short data pipes operating in fixed data mode. In the T7903 initialization command list, use SDP commands to set up short pipes for the transmit direction on the B1 and B2 time slots of the network port. These short pipes must be configured in fixed data mode (MODE = 0x6). Also in this command list, use set short pipe data (SSP) commands to set the short pipe data to all 1s. Later, new SDP commands can be executed to assign and configure the B-channel pipes for other modes (such as long pipes in HDLC mode).

Appendix E. Questions and Answers

(continued)

Miscellaneous

Q28: Does execution of SDPs for B channels interfere with data being transmitted on the D-channel pipe?

A28: No, they are independent.

Q29: Do multiple TE port configurations require that all network connections come from the same switch? If so, is there a specification that guarantees that multiple BRI lines delivered to a customer premises will be from the same switch?

A29: Yes, multiple TE port configurations require that all network connections come from the same switch. Otherwise, the possible differences in network timing frequency will cause data slips. There is no specification that guarantees multiple, same-switch drops. But, network experts have indicated that running lines from different switches to the same drop point is not normal procedure and should not occur.

Q30: Are all T7903 V_{DD}/V_{SS} pins tied internally?

A30: Yes.

Q31: Three BRI port data applications require 12 HDLC channels for B-channel data and six for the D channels. Can the ISA-MWAC handle this?

A31: Your application needs 18 long pipes. Since there are only 16 long pipes available, two ISA-MWACs could be used, providing enough long pipes for five ports. Another solution would be to use a single-channel HDLC formatter like the T7121 connected to the CHI.

Q32: Can two ISA-MWACs share the same DRAM?

A32: The ISA-MWAC has DRAMREQ (input) and DRAMACK (output) pins to allow arbitration. But, the timing involved in arbitrating DRAM between two ISA-MWACs is not trivial. It is suggested that separate DRAMS for each ISA-MWAC be used.

Q33: How do the DRAM column and row addresses map into a 20-bit memory address supplied in IP5 and IP6?

A33: The column address makes up DRAM address bits 18 and 8—0. The row address makes up DRAM address bits 19 and 17—9.

Q34: Can a host get to the command queue pointer or internal registers without going over the ISA bus?

A34: No.

Q35: Explain the difference between EXTEST and CLAMP in JTAG.

A35: EXTEST drives the current holding register values onto the pins. The BS registers are also placed in the scan chain (not the BYPASS register). A new string of boundary-scan bits are then shifted in. The CLAMP command also drives the current holding register values onto the pins, but puts the BYPASS register in the scan chain (not the BSR). In other words, an EXTEST command is the same as a CLAMP command followed by a SAMPLE/PRELOAD command.

Q36: If I use a shared memory architecture, how long can I hold the T7903 out of DRAM?

A36: You must assume that the T7903 will need the DRAM immediately after the host takes it. If the FIFO fill level is set to 64 bytes (FL = 1; bit 13, IP0), the host has a minimum of 64 bytes * 8 bits/byte * 1/(bit rate of fastest channel) before a receive pipe may overflow or a transmit pipe may underrun. For a 64 kbits/s channel, this is 8 ms.

Appendix E. Questions and Answers (continued)

Miscellaneous (continued)

Q37: Can you suggest any other transformer manufacturers that may make transformers suitable for use with the T7903?

A37: The following are some of the manufacturers that make transformers for BRI S/T line interface applications. Where part numbers are listed, preliminary characterization indicates that the part may be suitable for use with the Lucent Technologies T7903. It should be noted that accredited layer 1 conformance testing was not performed. Full conformance testing should be completed to ensure compliance.

1) ***Advanced Power**** **Components plc**
U.S. Man Rep:
APC-Terry Manton
336 West Passiac St.
Rochelle Park, NJ 07662
Phone: (201) 368-1750
FAX: (201) 368-1704

European Office:
Advanced Power
Components LTD
47 Riverside,
Medway City Estate
Strood, Rochester
Kent, ME2 4DP
United Kingdom
Phone: 44 1634 290588
FAX: 44 01634 290591

Part # APC6622D—This module contains transmit power-off switch, interface resistors, reinforced isolation transmit/receive transformers, protection circuitry, and EMI choke.

2) ***Vacuumschmelze**† **(VAC)***
U.S. Office:
Vacuumschmelze
186 Wood Avenue South
Iselin, NJ 08830
908-494-3530

European Office:
***Vacuumschmelze* GmbH**
V-G33, Mr. Heiko Gerberbauer
37 Gruener Weg
D-63450 Hanau
Germany
Phone: 49 6181 38 2026
FAX: 49 6181 38 2780

No VAC transformers have been characterized with the T7903.

3) ***Pulse Engineering‡, Inc.***
U.S. Office:
***Pulse Engineering*, Inc.**
P.O. Box 12235
San Diego, CA 92112
Phone: (619) 674-8100
FAX: (619) 674-8262

Part # PE-68995—Single, reinforced isolation transformer.
Part # PE-65495—Dual, basic isolation transformer.
Part # PE-65795—Dual, basic isolation transformer, surface mount.

* *Advanced Power* Components is a registered trademark of Advanced Power Technology, Inc.
† *Vacuumschmelze* is a registered trademark of Vacuumschmelze GmbH.
‡ *Pulse Engineering* is a registered trademark of Pulse Engineering, Inc.

Appendix E. Questions and Answers

(continued)

Debugging

Q38: I'm having problems getting pipes to work. Any suggestions?

A38: First, make sure that all anchor pipes for an interface are set up before enabling the interface (setting NP and CHI bits in register IP0) and before executing NP or CDM commands. **See the four rules listed in the Linked List and Anchor Pipes section.** Make sure you clear the pipe in the SDP command (CLR = 1, bit 7) the first time an SDP is issued. Also, make sure that the proper mode is selected (HDLC-D mode for D-channel transmitters, HDLC mode for D-channel receivers or any other transmit/receive data channels from DRAM that require HDLC).

Q39: In my application, multiple transmit descriptor/buffers are set up with EOL interrupts and TFC interrupts enabled. But, TFC interrupts are never reported, only EOLs. Why?

A39: You may have both the EOL and EOF bits set to 1 in your last TD. The T7903 will not use the data in the last buffer if its descriptor has EOL = 1.

Q40: Setting NAI = 1 in IP6 does not seem to be inhibiting autoincrementing of the DRAM address pointer for read accesses. Why?

A40: With NAI = 1, consecutive reads of IP7 will automatically increment only the lower 2 bits of the DRAM address pointer. Program NAI = 0.

Q41: I'm having trouble getting local loopback to work on the D channel. I'm force activating as a TE and not talking to a switch. Any suggestions?

A41: Set the EZ bit in the NP command to 1 when using TE D-channel local loopback without a network connection. This is necessary when force activating (FACT = 1 in NP command) as a TE and not talking to an actual switch or NT1.

Q42: Is there any internal state/status information available that would be useful for debugging?

A42: The only internal state information that is available is the command queue pointer in the staging area. It can be read to see if the device is accessing expected locations in DRAM.

Q43: The B channels don't work properly. They send data out but close the frame too early (without appending CRC), without continuing on to the next descriptor. IDL = 0 doesn't work either.

A43: MODE is incorrectly set to HDLC-D for a B channel. Use HDLC mode.

Q44: I'm having trouble getting remote loopback to work on the B channels.

A44: Make sure that no B-channel pipes are set up. If they are, use the DTS command to delete them.

Q45: We are using a powerup reset circuit (RC time constant through a Schmitt trigger) to reset the T7903 on our ISA adapter card design. This seems unreliable. What should we do?

A45: Increase the time constant, or connect the T7903 reset pin to the reset_drv signal on the ISA bus.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903

Introduction

Line interface circuitry plays a critical role in ISDN S/T-interface terminal equipment (TE) design. The designer must comply with the requirements established by the manufacturer of the line interface chip (proper component values, transformer turns ratio, etc.) to ensure ITU-T I.430 conformance. Designers must also be aware of requirements on electromagnetic interference (EMI), overstress immunity, and safety. The Lucent Technologies T7903 ISA-MWAC has a robust analog front end which simplifies most conformance issues. However, careful line interface circuit design is important in order to ensure that all requirements are met.

The purpose of this application brief is to provide all the necessary information required to design a product that meets I.430 conformance requirements for TEs at the S/T reference point. Critical I.430 issues are explained, as well as important EMI and safety considerations. An interface circuit for the T7903 network ports (when configured as TEs) is presented, and its performance relative to important I.430 specifications is discussed. Interface circuit modifications for NT operation are also discussed.

Since EMI, safety, and overstress immunity requirements are application-dependent, the circuit implementation given in this note should be considered only as a guide. The actual circuitry needed for a specific application will depend on system characteristics and agency requirements.

ITU-T I.430 Layer 1 Requirements at the S/T-Interface

ITU-T Recommendation I.430 (March 1993) is an international standard that defines the layer 1 electrical characteristics at the S/T reference point. ETSI (European Telecommunications Standards Institute) Standard ETS 300 012 outlines the specific requirements for Europe, while ANSI (American National Standards Institute) Standard ANSI T1.605-1991 defines the requirements for the United States. These ETSI and ANSI standards are based on ITU-T I.430. Most of this note focuses on the I.430 requirements for TEs. Information on NT requirements is given in the Requirements for NT Ports section of this document.

The line interface circuit is a critical part of meeting the following I.430 requirements:

- Transmitter output impedance when inactive and powered down or when transmitting a binary one (I.430 Section 8.5.1.2)
- Transmitter output impedance when transmitting a binary zero (I.430 Section 8.5.1.2)
- Transmitter pulse shape and amplitude for 50 Ω, 400 Ω, and 5.6 Ω loads (I.430 Sections 8.5.3 to 8.5.5)
- Unbalance about earth (I.430 Section 8.5.6)
- Receiver input impedance (I.430 Section 8.6.1.1)

Figure F-1 shows the basic interface circuit for one network port of the T7903 (when configured as a TE). The line interface transformers should be 2.0:1 turns ratio for both the transmit and receive directions. The following list summarizes the suitable Lucent 2.0:1 turns ratio transformers that are available as of this writing:

2768B: Dual, through-hole, operational insulation.
2798B: Dual, surface-mount, operational insulation.
2800B: Dual, surface-mount, for PCMCIA, operational insulation.
2776E: Single, through-hole, reinforced insulation.

Two Lucent 2776E 2.0:1 transformers are recommended for international applications or any application requiring reinforced insulation between the network and line interface device. The 2768B, 2798B, or 2800B surface-mount dual 2.0:1 transformers are recommended for North American applications or in any application requiring only operational insulation. Relay REL1 opens the transmit path when power is shut off. Safety requirements dealing with insulation, as well as surge protection and common-mode noise suppression, are discussed in later sections of this application brief.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

ITU-T I.430 Layer 1 Requirements at the S/T-Interface (continued)

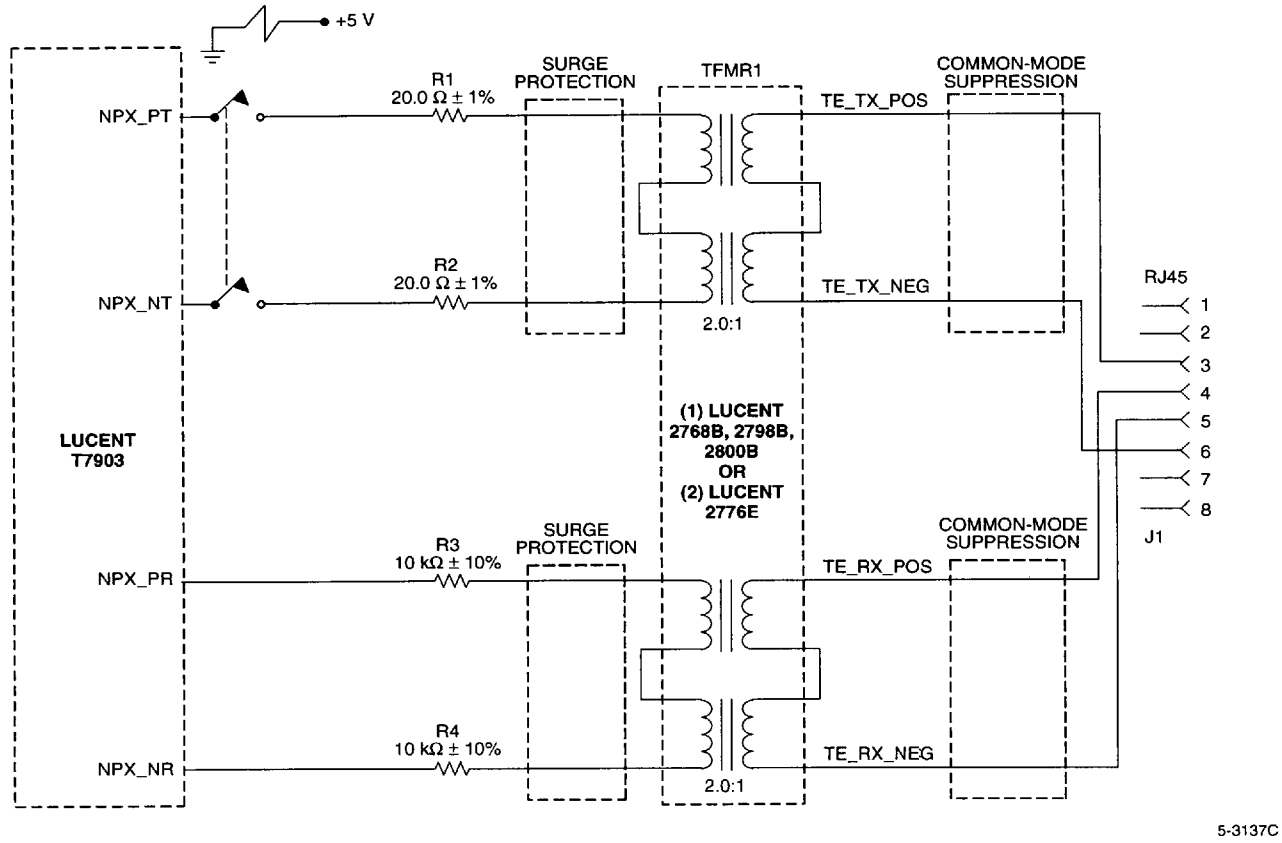

Figure F-1. Basic S/T-Interface Circuit for a T7903 Network Port (TE Mode)

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Transmitter Pulse Shape and Amplitude for 50 Ω, 400 Ω, and 5.6 Ω Loads

The I.430 pulse templates for 50 Ω and 400 Ω loads are shown in Figures F-2 and F-3. The 50 Ω load is the standard line termination, while the 400 Ω test ensures that the TE will not overdrive when other TEs are simultaneously transmitting pulses of the same polarity. An additional TE specification requires that the transmitter output voltage be less than or equal to 150 mV when driving a 5.6 Ω load. The 5.6 Ω load represents the condition when another TE is transmitting the opposite polarity pulse than the TE under test. The T7903's analog front end provides the proper output pulse shape and amplitude for all required load impedances when the proper external components are used.

The device requires two external resistors to generate internal bias currents and voltages. An 11.5 kΩ resistor is connected from the CSENS device pin to V_{SS} to derive the transmitter output currents, and a 22.1 kΩ resistor is connected from the V_{REF} pin to V_{DD} for setting the clamp threshold. These resistors must be 1.0% tolerance or less. Also, a resistance of 40 Ω (1.0%) is required between the device's transmitter output pins and the transformer to provide proper termination. This 40 Ω should be split evenly between the two legs of the transmitter. The contact resistance of the relay shown in Figure F-1 should be included in the 40 Ω total if it is 1 Ω or more.

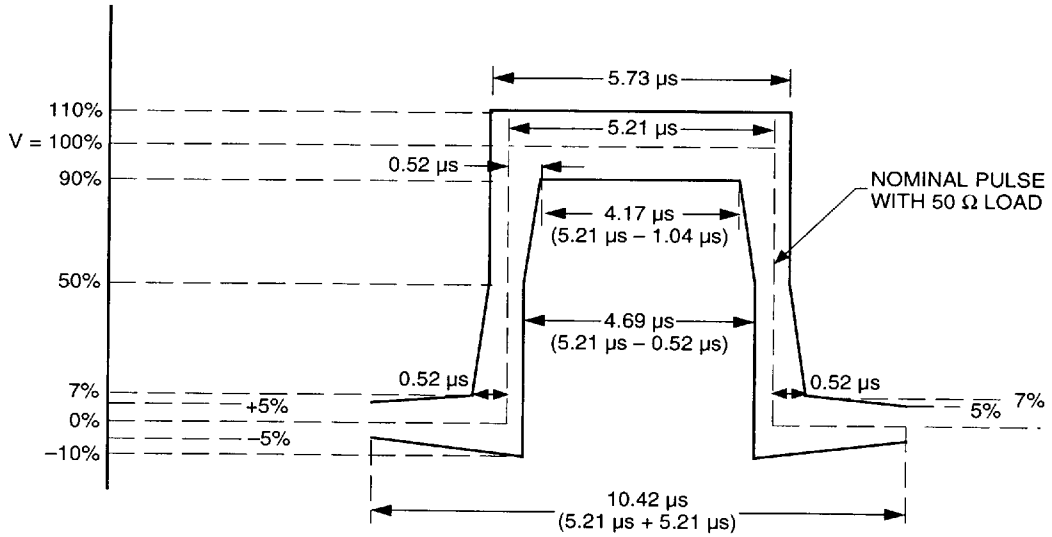

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Figure F-2. Transmitter Output Pulse Template for 50 Ω Load at the S/T-Interface

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Transmitter Pulse Shape and Amplitude for 50 Ω, 400 Ω, and 5.6 Ω Loads (continued)

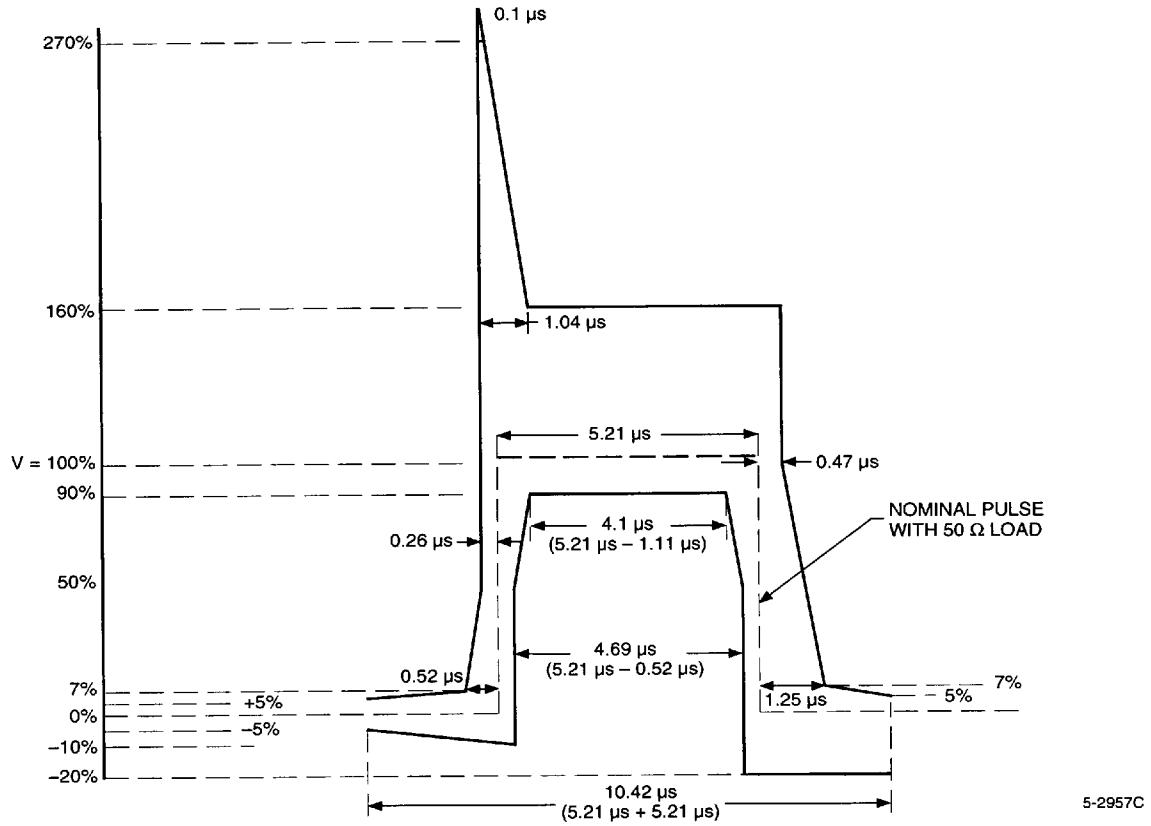


Figure F-3. Transmitter Output Pulse Template for 400 Ω Load at the S/T-Interface

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Transmitter Output Impedance When Inactive and Powered Down or When Outputting a Binary One

A TE transmitter's output impedance must exceed the template shown in Figure F-4 when inactive and powered down or when transmitting a binary one. Between the frequencies of 2 kHz and about 50 kHz, performance relative to this template is mainly a function of the open circuit inductance of the line interface transformer. The Lucent transformers are designed to provide adequate margin to this portion of the template.

The high-frequency portion of the template is dominated by interface capacitance. From the template, the maximum allowed capacitance for a TE is found to be 795 pF (total interface capacitance as viewed from the line-side of the transformer). This limit is found by calculating the capacitance that yields 200 Ω at 1 MHz (the high-frequency corner of the template) using $200\ \Omega = 1/[2\pi(1\ \text{MHz})C]$. This total capacitance is made up of board, device, and protection parasitics between the transmitter leads, transformer parallel capacitance, and the TE connecting cord.

To calculate the capacitance budget for the interface circuitry, the capacitance of the connecting cord must be determined. I.430 defines a "standard ISDN basic access TE cord" as having a maximum of 350 pF. Since some conformance testing agencies require the use of this maximum capacitance cord during testing, 350 pF must be assumed. Subtracting 350 pF from the 795 pF limit leaves 445 pF. The parallel capacitance of the Lucent transformers is specified at a maximum of 100 pF, which leaves 345 pF for parasitics. Reflecting this to the device side of the transformer by dividing by the turns ratio squared ($2.0^2 = 4.0$) and then subtracting 5 pF for device pin parasitics results in 81 pF for surge protection and EMI reduction circuitry. It should be noted that this is the maximum when device-side protection is used. Since all device side parasitics are scaled by a factor of 4.0, increased template margin can be gained by using line-side protection.

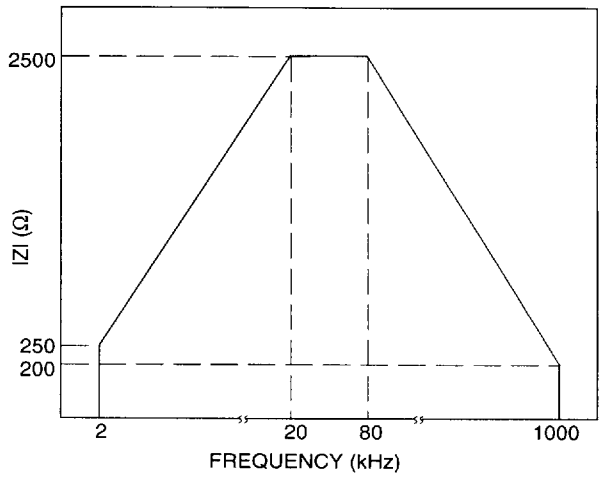


Figure F-4. I.430 Transmitter Output Impedance Template

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Transmitter Output Impedance When Inactive and Powered Down or When Outputting a Binary One (continued)

Another I.430 requirement for a TE transmitter when inactive and powered down or when transmitting a binary one is that at a frequency of 96 kHz, the peak current resulting from an applied voltage of 1.2 V (peak) should not exceed 0.6 mA. Under powered up conditions, the transmitter pins of the T7903 present an adequate impedance to this test signal. But, when powered down, the chip's internal protection diodes shunt the line, as shown in Figure F-5.

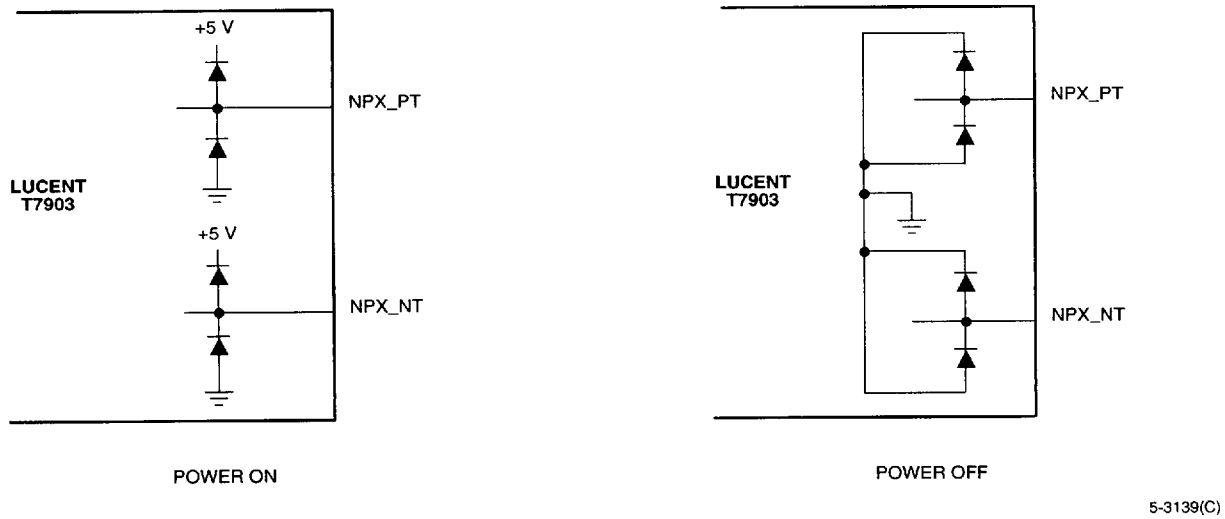


Figure F-5. T7903 Internal Protection Circuitry

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Transmitter Output Impedance When Inactive and Powered Down or When Outputting a Binary One (continued)

To prevent excessive current flow during the peak current test, a relay (or other switchable isolating device) should be placed between the transmitter pins and the external line interface circuit. The relay should open when power is removed from the chip, thus isolating the chip's transmitter from the rest of the interface. This device is shown in Figure F-1 as REL1 (an example of this type of relay is the *Aromat** type TN2E-5V).

Figure F-6 shows alternate methods for opening the transmitter circuit when power is removed. The first example uses two P-type MOSFETs in the transformer's device-side center tap, driven by an NMOS inverter. P-type devices were used because the transmitter pins are biased at 5 V. If N-type MOSFETS were used, a gate voltage of 5 V + Vgs would be required which may not be available in some 5 V systems. Note that a single P-type MOSFET in the center tap does not provide isolation in both directions because of P-tub conduction between drain and source. The second example in Figure F-6 shows the use of a solid-state relay in the center tap.

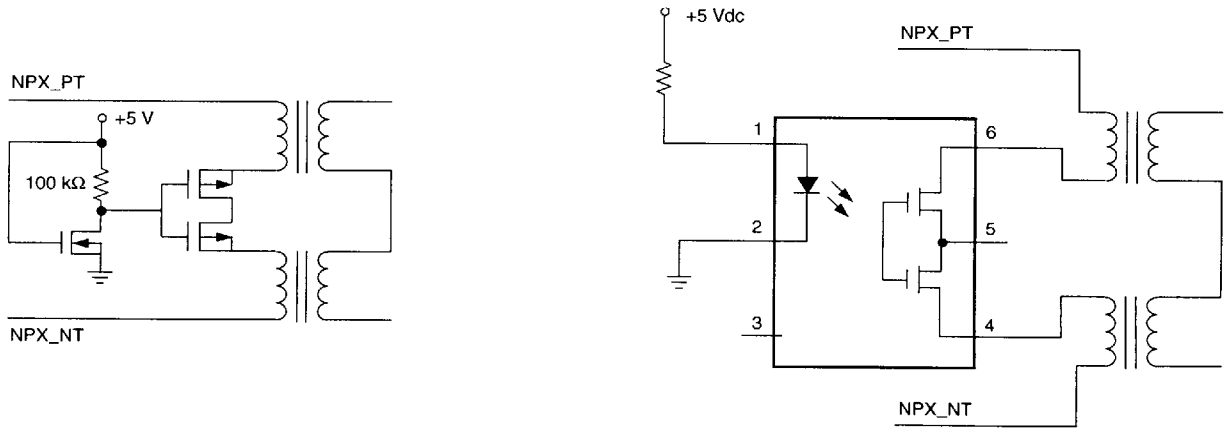


Figure F-6. Alternate Methods to Open the Transmit Circuit Upon Loss of Power

* *Aromat* is a registered trademark of Aromat Corporation.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Transmitter Output Impedance When Outputting a Binary Zero

A TE's transmitter must have an output impedance equal to or greater than 20 Ω when transmitting a binary zero. I.430 states that this limit applies for both 50 Ω and 400 Ω loads. The test is performed by measuring the pulse amplitude for load values of +10% and −10% of the nominal value. For example, in the 400 Ω case, output pulse amplitude should be measured with loads of 360 Ω and 440 Ω. The output impedance is then found from:

$$Z_0 = \frac{R_2R_1(V_2 - V_1)}{R_2V_1 - R_1V_2}$$

where R_1 is 360 Ω (400 Ω − 10%), R_2 is 440 Ω (400 Ω + 10%), and V_1 and V_2 are the voltages across R_1 and R_2, respectively.

The T7903 uses a voltage-clamped current source transmitter. The clamp is on when driving a 50 Ω load and the internal driver's output impedance is fairly high. For the 400 Ω load, the transmitter clamp begins to current-limit and the driver's output impedance is lower than in the 50 Ω case. Thus, the external interface circuit must supply much of the impedance to meet the I.430 output impedance requirement. This external impedance is made up of transformer resistance, cord resistance, and external added resistance. The T7903 requires 40 Ω of resistance (1% tolerance) on the device side of the transformer (see Figure F-1). Using a minimum value for this resistance (− 1%) and reflecting it to the primary of the transformer (the line side) gives 9 Ω. The transformer dc resistance is comprised of primary resistance (≅ 1.9 Ω) and reflected secondary resistance (≅ 1 Ω), bringing the total to 11.9 Ω. The final components of the transmitter output impedance are the reflected impedance of the internal driver itself (≅ 5 Ω), the standard ISDN cord resistance of 6 Ω, and the resistance of an EMI choke (≅ 0.4 Ω), bringing the total well above the 20 Ω requirement.

Unbalance About Earth

The TE transmitter must conform to two I.430 requirements for unbalance about earth: longitudinal conversion loss (LCL) and output signal balance (OSB).

Any asymmetries in the line interface circuit will produce unwanted differential noise components when common-mode (longitudinal) voltages are applied.

The ratio of the applied common-mode signal (E_L) to the differential noise signal (V_T) is the longitudinal conversion loss of the circuit and is expressed by $LCL = E_L - V_T$ when the levels are in dB. I.430 LCL requirements are as follows:

- From 10 kHz to 300 kHz—LCL must be greater than or equal to 54 dB.
- From 300 kHz to 1 MHz—LCL must be greater than or equal to 54 dB at 300 kHz, minimum value decreasing from that frequency at 20 dB/decade.

A differential transmitter will produce unwanted longitudinal voltage components if asymmetries exist in the line interface circuit. The ratio of the transmitter's differential signal level (V_T) to the produced longitudinal signal (V_L) is the output signal balance of the interface, which is expressed by $OSB = V_T - V_L$ when the levels are in dB. I.430 OSB requirements are as follows:

- 96 kHz—OSB must be greater than or equal to 54 dB.
- From 96 kHz to 1 MHz—OSB must be greater than or equal to 54 dB at 96 kHz, minimum value decreasing from that frequency at 20 dB/decade.

The TE receiver must conform to the LCL requirements given above.

TE performance relative to these unbalance specifications is a function of:

- The transformer's center tap accuracy
- Balance of other interface components (chip, resistors, chokes, etc.)
- Board trace and cord pair symmetry

The main factor that affects line interface balance is the transformer. For good balance, the transformer's center taps must be accurate. This means that the coils connected to the center tap must be the same inductance and have similar interwinding capacitance (this is also called direct capacitance and is the parasitic capacitance between the transformer's primary and secondary windings). The Lucent transformers have accurate line-side center taps, providing margin to the I.430 unbalance requirements. But, if other sources of unbalance are large, this margin may be inadequate. Also, as inductance and capacitance are added to the interface circuit for EMI suppression, the resonant frequency of the interface may be lowered enough to impact margin even further at higher frequencies.

Board layout and component selection can also affect the balance of the S/T-interface. Differential board traces should be run parallel to each other and on the same board layer. Also, any circuit element used in one lead of a differential pair should be used in the other lead. An example of this is shown in Figure F-1.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Unbalance About Earth (continued)

The 40 Ω required for proper transmitter operation is split between the two transmit leads (R1 and R2), and a double-pole relay is used instead of a single-pole type (the center tap circuits shown in Figure F-6 are also recommended for preserving interface balance). There should be no ground plane under the interface circuitry from the transformer to the network interface connector. This reduces some of the unbalance effects caused by parasitics to ground and may also be required to meet creepage and clearance specifications (described later in this note).

One approach in solving balance problems is to add a low-frequency (high-inductance) common-mode choke on the line side of the transformer. This has the effect of increasing impedance in each leg of the pair at lower frequencies (up to 1 MHz), thus minimizing the unbalance effects over the frequency range covered by I.430 requirements. An additional benefit to using a high-inductance choke is that low-frequency EMI into and out of the S/T-interface will be reduced. Typical inductance values for this type of choke are in the 1 mH—10 mH range. The use of low-frequency, common-mode chokes is discussed in more detail later in this document.

Receiver Input Impedance

TE receiver input impedance requirements are identical to the requirements for transmitter output impedance when inactive and powered down or when transmitting a binary one. Therefore, receiver capacitance considerations are identical to those described previously for the transmitter.

The T7903 receiver uses the same internal protection circuit as the transmitter (shown in Figure F-5). When power is removed from the chip, the internal protection will shunt the receiver pins. However, the receiver's 10 kΩ resistors (R3 and R4, in Figure F-1) will help limit current during the power-off peak current test; thus a relay is not required.

Electromagnetic Interference (EMI) Design Considerations

An important aspect of any design is limiting radio frequency electromagnetic interference, or EMI. Not only is it important to reduce the emissions radiated out of the S/T-interface, but the equipment's susceptibility to interference on the line must be limited. Fortunately, EMI suppression circuitry will generally help reduce the levels of EMI in both directions.

Radiated EMI can be caused by poor board layout, high clock rates, etc. Also, since the balance about earth of any differential interface will not be perfect, differential signals from the transmitter can be converted to common-mode signal components and radiated out of the interface.

Limiting susceptibility to EMI is important since common-mode sources are nearly always present. Some examples of external common-mode sources include power lines, motors, fluorescent lights, etc. These noise signals can be converted to differential signal components in the receive path, and bit errors can result (susceptibility to EMI).

Radiated emissions can be either differential or common-mode, but usually the most difficult type of EMI to control is common-mode. To some extent, common-mode emissions can be minimized by using proper board layout techniques. The designer should use the following design techniques:

- Reduce clock frequencies and increase rise/fall times when possible.
- Keep clock sources (crystals, VCXOs, etc.) away from the board edge.
- Minimize the distance between the T7903 and the network interface connector.
- Route the traces of differential signals parallel to each other and on the same board layer.
- If the +5 V supply is noisy, use a 5 Ω resistor between +5 V and the V_{DD} pins on the T7903 to decouple the noise (a ferrite bead may also help).

The above layout techniques are helpful, but generally will not be sufficient for most S/T-interface designs. Figure F-7 shows an approach to common-mode noise reduction, reducing EMI out of and into the interface by using common-mode chokes and transformer center tap capacitors. The chokes provide a high impedance to common-mode currents, and the capacitors at the transformer center taps provide a low impedance to ground for common-mode voltages. The chokes also provide some differential-mode emission suppression.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Electromagnetic Interference (EMI) Design Considerations (continued)

Typical inductance values for high-frequency EMI reduction chokes are 2 µH to 50 µH. If EMI out of the line interface is small, the center tap capacitor shown on the transmitter may not be needed. However, the capacitor on the receiver center tap is recommended since differential receiver performance can be degraded by excessive common-mode noise injected externally.

It should be noted that the emission levels radiated from any design are a result of many system variables, such as the antenna characteristics of the line interface and cable and system clock rates. Therefore, the circuitry required to limit EMI to acceptable levels will vary from system to system.

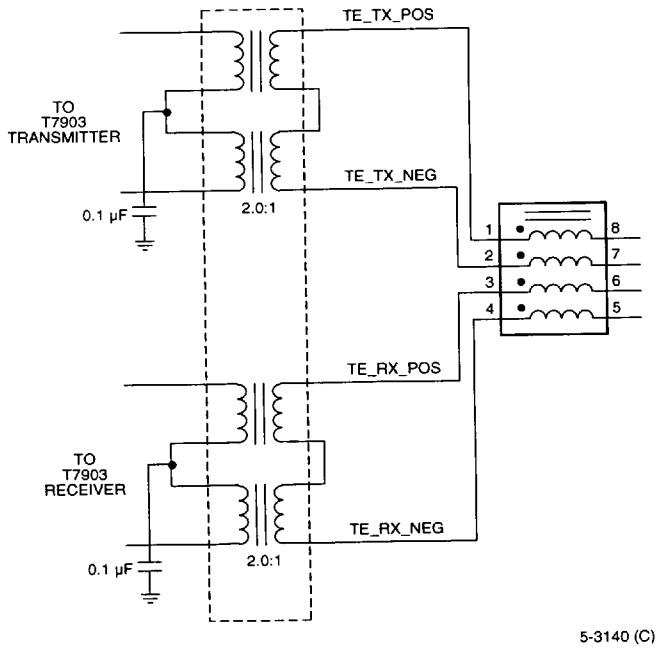


Figure F-7. Common-Mode Suppression Circuit

Surge Protection Considerations

Surge protection (overvoltage protection) is used to protect the line interface integrated circuit from voltage spikes originating from such events as lightning strikes and electrostatic discharge (ESD). Protection can be located on either the line side (primary protection) or the device side (secondary protection) of the transformer. Line-side protection has less impact on impedance templates than secondary-side protection, since any parasitic capacitance is not multiplied by the square of the transformer turns ratio. Some drawbacks to line-side protection schemes are that they are often more expensive and generally only protect against differential overstresses. Device-side protection schemes can benefit from the fact that overstresses are generally common-mode. Since the transformer and common-mode suppression circuitry will attenuate common-mode voltages, device-side protection can often be inexpensive. But, device-side protection may have a greater impact on impedance template margin due to the capacitance multiplication mentioned previously. In either case, surge protection design is highly dependent upon the specific overvoltage requirements relevant to an application.

Often, the enhanced diode bridge shown in Figure F-8 is used for surge protection. When used on the device side of the transformer, this circuit is effective against both differential and common-mode overstress. The zener diode is necessary to maintain a high impedance at the interface when a sinusoidal voltage of up to 1.2 V peak (line side) is applied during I.430 peak current testing. Zener diodes should be specified for transient voltage suppression applications, with fast response time and high surge current capability. Schottky or other fast recovery diodes are best suited for the bridge devices. Their maximum current capability must be determined from the maximum overvoltage requirements. The transmitter and receiver resistors can then be split to limit the current accordingly. Figure F-8 shows an example of split resistances in which 10 Ω is used between the transformers and the protection networks.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Surge Protection Considerations (continued)

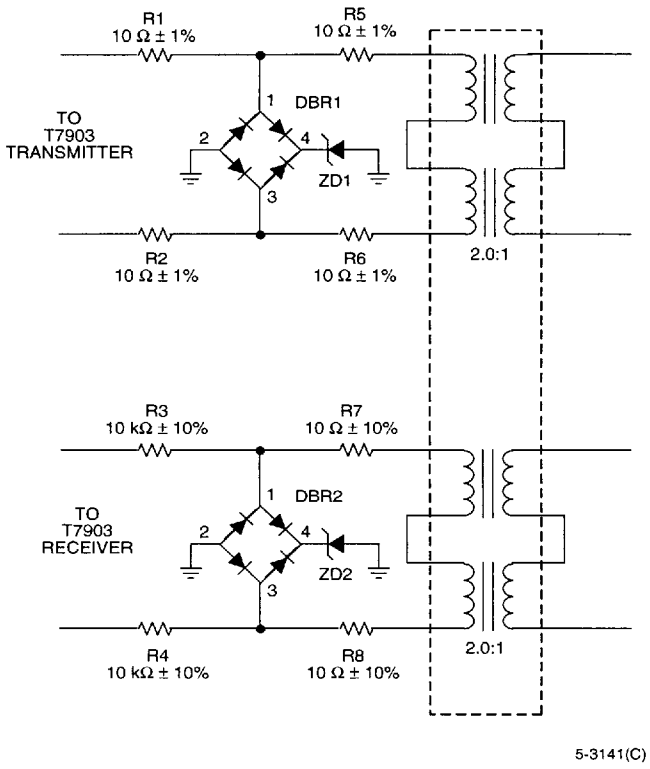


Figure F-8. Surge Protection Example

To find the minimum zener voltage necessary to prevent forward biasing of the protection circuit during the peak current testing of the transmitter pair, the 1.2 V peak test voltage is reflected to the secondary giving 2.4 V peak (see Figure F-9). Each transmitter pin is weakly pulled up to V_{DD} by pull-up resistors inside the T7903 (approximately 100 kΩ). Thus, the 2.4 V sinusoid is superimposed on 5 V and a peak voltage of 6.2 V appears on each transmitter rail with respect to ground. For conduction to occur, one diode plus the zener must be forward biased. Subtracting one diode drop (0.6 V) from 6.2 V yields a minimum zener voltage of 5.6 V. A typical value would be 6.8 V.

The zener voltage calculation for the T7903 receiver protection circuit is slightly different than previously described, and is also illustrated in Figure F-9. The receiver interface circuit is biased by an internal common-mode voltage of 1.9 V, on which the reflected test voltage (2.4 V) is superimposed. Therefore, the maximum voltage seen across one diode of the bridge and the zener is 3.1 V. Subtracting 0.6 V for the bridge diode drop leaves 2.5 V for the minimum zener voltage. To account for power supply variance and other factors, the actual zener voltage should be somewhat higher than this minimum. Often, the same value used for the transmitter is used for the receiver. The interface capacitance limits described earlier in this note must be considered when designing surge protection. Low-capacitance diodes in the bridge circuits are suggested. The effectiveness of any protection scheme is generally checked through safety and immunity testing. Safety tests usually employ some kind of surge overstress while immunity tests include EMI, ESD, and fast transient/burst testing (see the Standards section of this Appendix for a list of safety standards).

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Surge Protection Considerations (continued)

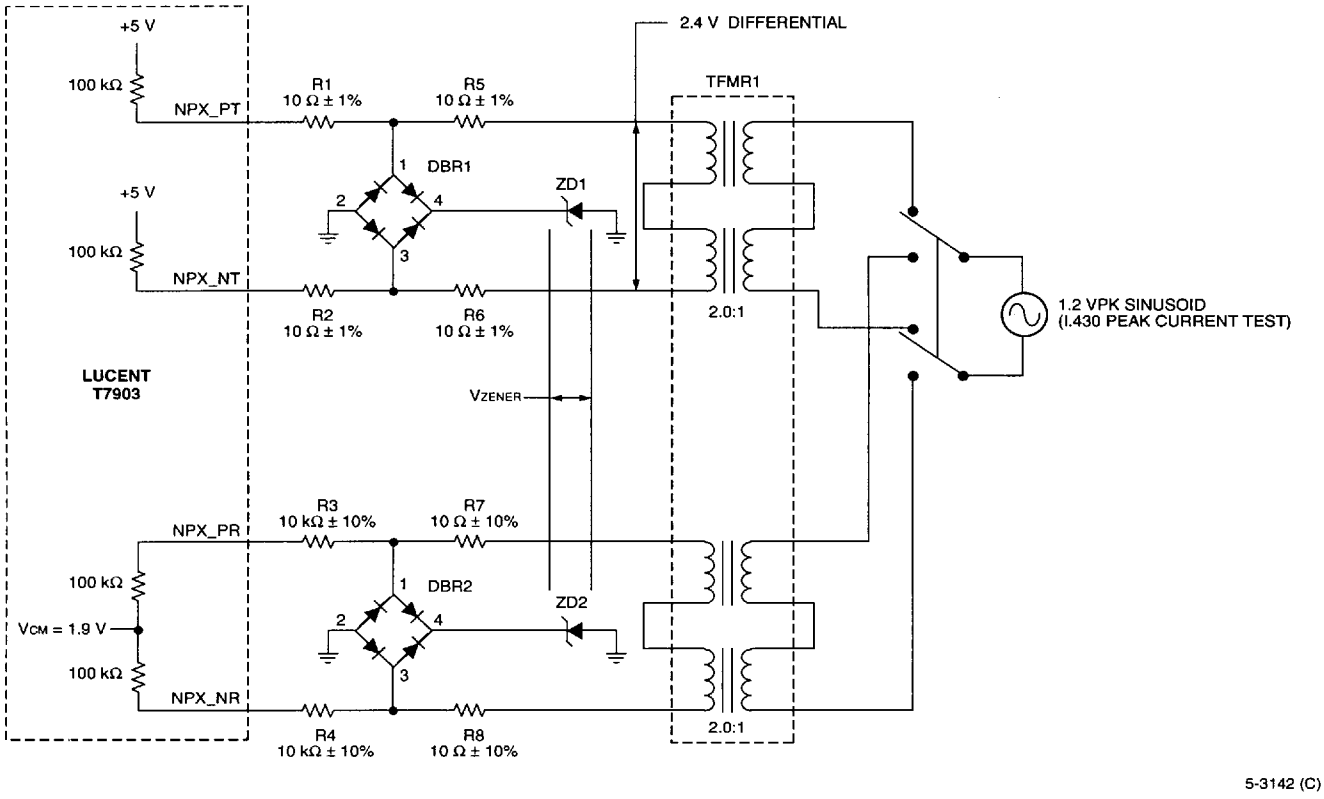


Figure F-9. I.430 Peak Current Test

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Safety Requirements and Considerations

Safety requirements currently vary from country to country. In the U.S., *UL* 1950 (Safety of Information Technology Equipment, Including Electrical Business Equipment), *UL* 1459, and FCC part 68 are relevant to ISDN terminal equipment designers. International standards relevant to terminal equipment sold outside the U.S. include EN 60950 (Safety of Information Technology Equipment, Including Electrical Business Equipment) and EN 41003 (Particular Safety Requirements for Equipment to be Connected to Telecommunications Networks). The following describes various issues important for international certification.

Current interpretation of EN 60950 and EN 41003 standards may require the use of double or reinforced insulation between the primary and secondary coils of transformers used at the S/T reference point. These types of insulation provide two levels of protection against shock. As described previously in this note, Lucent Technologies makes four transformers for use with the T7903. The 2768B, 2798B, and 2800B are dual 2.0:1 turns ratio transformers. They use an insulation type that is classified as operational insulation (does not provide protection from shock), and therefore may not satisfy the requirements for international safety certification. The 2776E is a single, 2.0:1 transformer designed using reinforced insulation. This transformer is recommended for use in terminal equipment sold internationally. Currently, either of these two transformers are viable solutions in North America.

Another important design parameter for a transformer is dielectric strength. The 2768B, 2798B, and 2800B transformers can withstand the application of 1500 Vrms, 60 Hz. The 2776E can withstand 3000 Vrms, 60 Hz.

Although device-side center tap capacitors are recommended (see Figure F-7), capacitors on the line-side center taps of the transmit and receive transformers could be used for common-mode rejection. Although these capacitors should be as large as possible, 680 pF is the recommended maximum to ensure compliance with international leakage current requirements. It is also recommended that line-side capacitors be formed by using two capacitors in series, providing two levels of fault protection, which may be required internationally. These capacitors should be VDE approved "Y" types (250 Vac VDE class X1/Y).

To meet creepage and clearance requirements in EN 60950 and EN 41003, there should be no ground plane, power plane, or signal traces under or within 2.5 mm of the line interface circuit. This distance must be maintained for all line interface board traces and components between the line side of the transformers and the network interface connector.

For terminal equipment marketed internationally, printed-circuit boards must have a fire rating of V1 or better. Fire ratings are defined in section 1.2.13.2 of standards *UL* 1950 and EN 60950.

For user-accessible products (such as personal computer adapter boards) to be sold internationally, a plastic shield that covers the network circuitry (both top and bottom of the board) may be required. The shield should have a fire rating of V2 or better.

T7903 Line Interface Circuit Example and ITU-T I.430 Test Results

Figure F-10 shows a complete line interface circuit suitable for TE applications using the T7903 ISA-MWAC (when configured as a TE). Use of the 2776E transformer allows international compliance. To summarize:

- MOSFETs Q1—Q3 isolate the T7903 transmitter pins from the network when power is removed. Note that Q1 and Q2 have an on resistance of about 5 Ω each. Subtracting this from the 40 Ω total for the transmit loop leaves 30 Ω that must be supplied by external resistors (R1—R4).
- Resistors R1—R8 supply the necessary impedance for proper termination of the transmitter and receiver, and provide current limiting during overvoltage conditions.
- ESD/surge protection is provided by low-capacitance diode bridges (D1—D8) and zener transient voltage suppressors ZD1 and ZD2.
- Reinforced insulation between the network and low-voltage circuitry is provided by the Lucent Technologies 2776E transformers T1 and T2. A single 2768B, 2798B, or 2800B transformer could be used in North American-only applications.
- Center tap capacitor C1 and high-frequency choke T3 are for common-mode EMI reduction. Note that a capacitor identical to C1 could be placed between Q1 and Q2 to reduce common-mode noise injection towards the network.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

T7903 Line Interface Circuit Example and ITU-T I.430 Test Results (continued)

This circuit was used in a T7903-based personal computer (PC) adapter card. Layer 1 I.430 preconformance testing was performed on this card, and all S/T-interface related tests passed. The following sections provide details of the results. The Component List Table F-4 gives a component list for the interface circuit. The Relevant Standards section of this Appendix lists relevant standards and where to obtain copies, and gives information on various test firms.

The circuit in Figure F-10 was verified for ITU-T I.430 conformance through laboratory measurements (using a *Siemens** K1403 ISDN S_0 Analyzer) and preconformance CTS2 testing at *Wandel & Goltermann*† ATE Systems. It should be noted that CTS2 is the document that outlines the conformance test procedures for ETSI ETS 300 012 compliance in Europe.

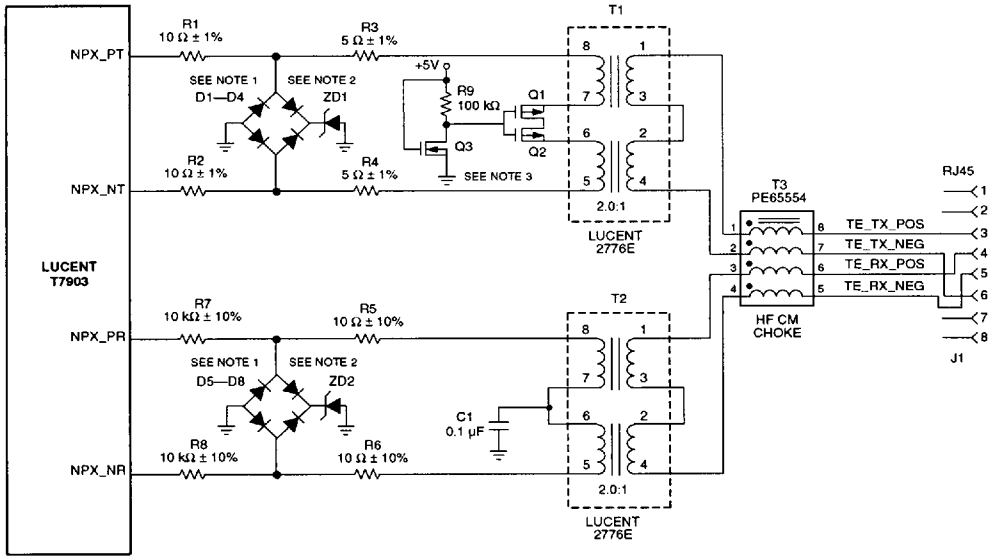
The following tests were conducted using a standard ISDN connecting cord. The parameters for this cord (from ETS 300 012) are as follows:

- Capacitance = 350 pF (+0%, –10%)
- Z > 75 Ω
- Crosstalk loss (C_L) > 60 dB
- R = 3 Ω per lead (+0%, –10%)
- Length between 7 m and 10 m

Transmitter Output Impedance When Outputting a Binary One

Figures F-11 and F-12 show the transmitter output impedance while the TE board was powered down (ITU-T I.430 state F1) and when powered up but inactive (state F3), respectively. There was good margin to the template in both tests (the measured impedance must lie above the template throughout the 2 kHz to 1 MHz range). It is evident from these figures that the interface circuit capacitance was kept to a minimum, providing more than adequate margin at higher frequencies.

* *Siemens* is a trademark of Siemens Aktiengesellschaft.
† *Wandel & Goltermann* is a registered trademark of Wandel & Goltermann Technologies.



5-3244(C)

1. All diodes (D1—D8) are type 1N-4151 or equivalent.
2. ZD1 and ZD2 are *Motorola** zener transient voltage suppressors, part number 1.5SMC6.8AT3.
3. Q1 and Q2 are *Philips*† type BST84 transistors. Q3 is a *Philips* type BST80 transistor.

* *Motorola* is a registered trademark of Motorola, Inc.
† *Philips* is a registered trademark of Philips Manufacturing Company.

Figure F-10. A Complete Line Interface Circuit for the T7903

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

T7903 Line Interface Circuit Example and ITU-T I.430 Test Results (continued)

Transmitter Output Impedance When Outputting a Binary One (continued)

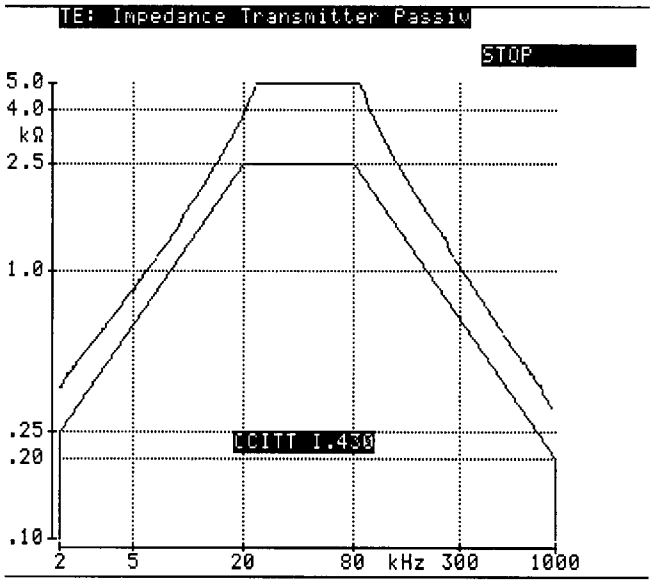


Figure F-11. Transmitter Output Impedance, Power Off

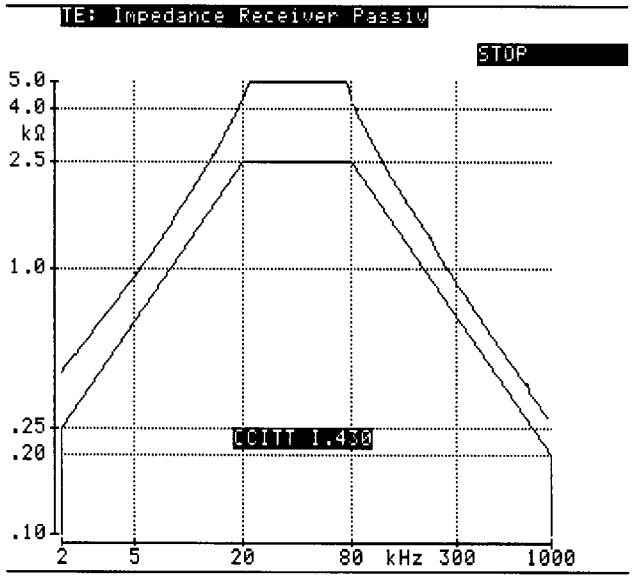


Figure F-12. Transmitter Output Impedance, Power On

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

T7903 Line Interface Circuit Example and ITU-T I.430 Test Results (continued)

Transmitter Output Impedance When Outputting a Binary One (continued)

Table F-1 gives the results for the output (transmitter) peak current test. Good margin was maintained to the 0.6 mA maximum.

Table F-1. Output Peak Current Test Results

TE State	Frequency	Pass Limit	Result
F1	96 kHz	0.6 mA	0.418 mA
F3	96 kHz	0.6 mA	0.369 mA

Transmitter Output Impedance When Outputting a Binary Zero

Table F-2 gives the transmitter output impedance when outputting binary zeros (pulses). All results show good margin to the 20 Ω minimum requirement.

Table F-2. Output Impedance—Binary Zero

Load	Pulse Polarity	Pass Limit	Result
50 Ω	Positive	≥20 Ω	29.8 Ω
50 Ω	Negative	≥20 Ω	29.8 Ω
400 Ω	Positive	≥20 Ω	28.8 Ω
400 Ω	Negative	≥20 Ω	28.8 Ω

Transmitter Pulse Shape and Amplitude for 50 Ω, 400 Ω, and 5.6 Ω Loads

Figures F-13 through F-18 show the transmitter output for 50 Ω, 400 Ω, and 5.6 Ω loads. As described previously, the pulse must be completely within the template for 50 Ω and 400 Ω loads, and under 150 mV in amplitude for the 5.6 Ω load. All pulse shape and amplitude tests passed with good margin.

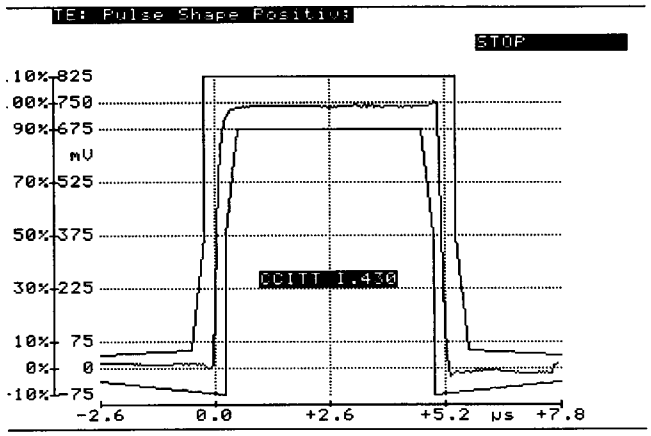


Figure F-13. Positive Pulse, 50 Ω Load

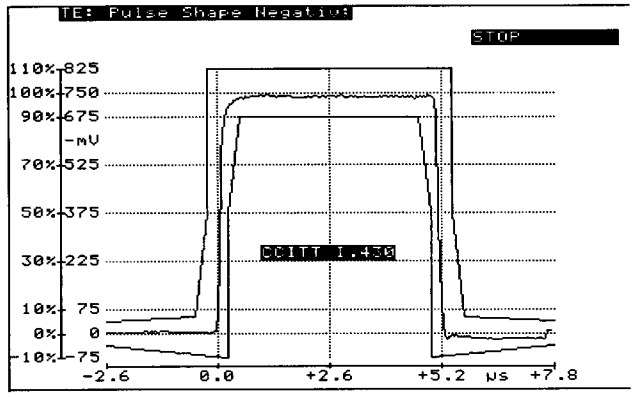


Figure F-14. Negative Pulse, 50 Ω Load

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

T7903 Line Interface Circuit Example and ITU-T I.430 Test Results (continued)

Transmitter Pulse Shape and Amplitude for 50 Ω, 400 Ω, and 5.6 Ω Loads (continued)

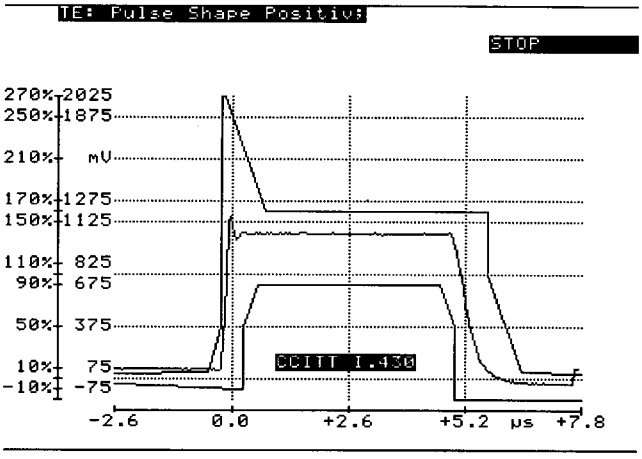


Figure F-15. Positive Pulse, 400 Ω Load

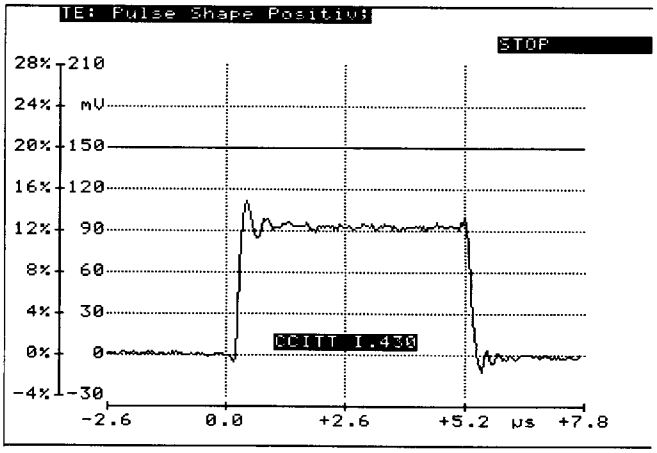


Figure F-17. Positive Pulse, 5.6 Ω Load

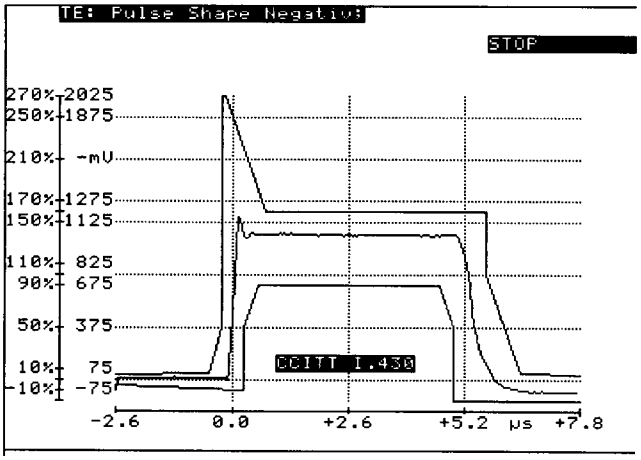


Figure F-16. Negative Pulse, 400 Ω Load

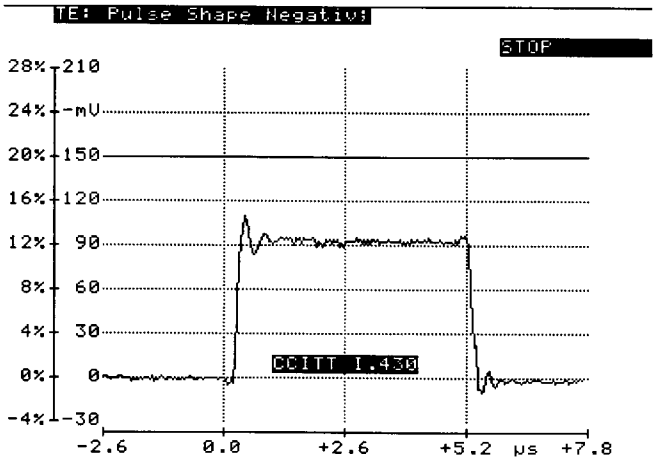


Figure F-18. Negative Pulse, 5.6 Ω Load

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

T7903 Line Interface Circuit Example and ITU-T I.430 Test Results (continued)

Transmitter Pulse Shape and Amplitude for 50 Ω, 400 Ω, and 5.6 Ω Loads (continued)

Unbalance about Earth. Longitudinal conversion loss (LCL) was tested for two board configurations. The first configuration used a low-frequency choke for increased balance, and the second configuration had the low-frequency choke removed (the board traces were shunted by zero Ω resistors). The signal balance of the circuit without the low-frequency choke was good enough to pass all LCL tests. Figures F-19 through F-22 show the LCL plots for the receiver and transmitter in both the powered down (F1) and the powered up (F3) states. Note that the LCL response must be above the template shown in the plots.

Good layout practices should eliminate the need for the low-frequency choke. If balance is still a concern, laying out the board to accept either a low-frequency choke or zero Ω resistors may prove useful. Since signal balance is layout sensitive, the decision of which components to populate can be made after preconformance testing, possibly saving some board cost.

Output signal balance tests are not required in ETS 300 012 (a reference is made to prEN 50096; see the Standards section of this Appendix) and are therefore not tested in the CTS2 test suites. Poor output signal balance will increase low-frequency EMI emissions. If this occurs, the low-frequency choke is recommended.

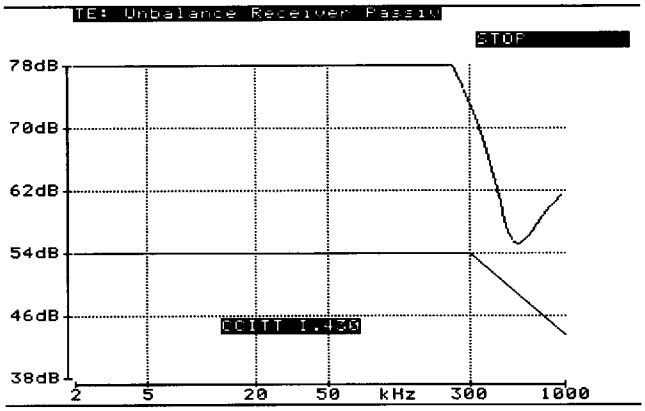


Figure F-20. Receiver LCL, Power On

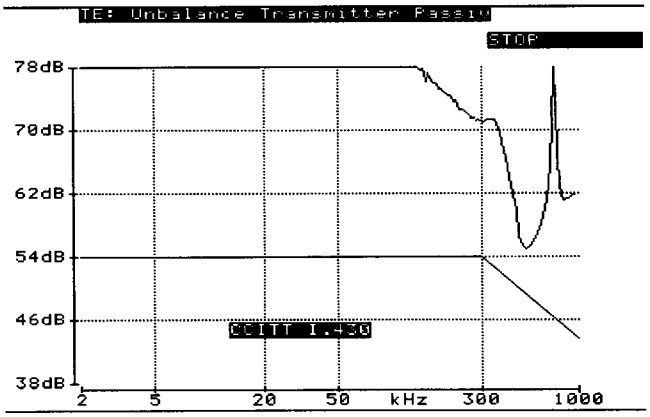


Figure F-21. Transmitter LCL, Power Off

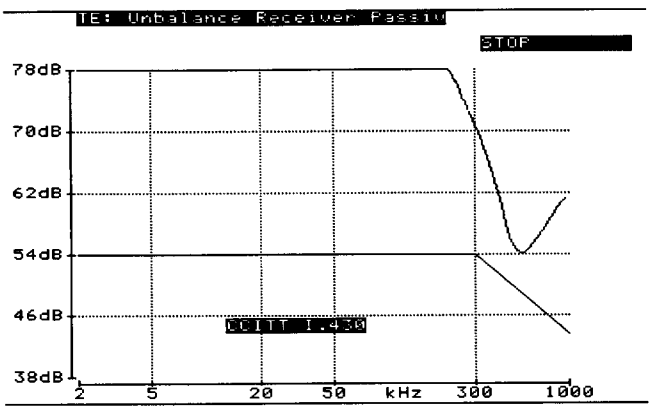


Figure F-19. Receiver LCL, Power Off

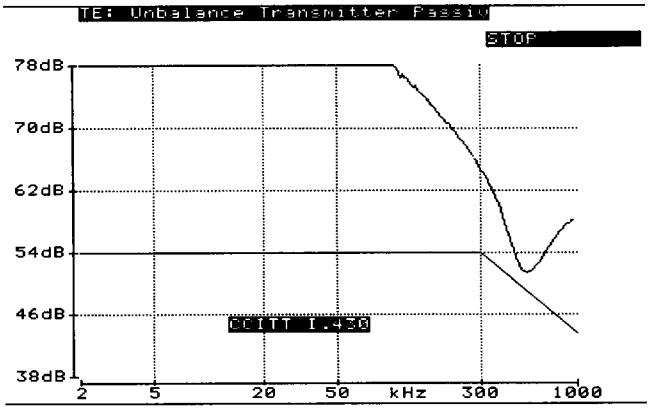


Figure F-22. Transmitter LCL, Power On

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

T7903 Line Interface Circuit Example and ITU-T I.430 Test Results (continued)

Transmitter Pulse Shape and Amplitude for 50 Ω, 400 Ω, and 5.6 Ω Loads (continued)

Receiver Input Impedance. Figures F-23 and F-24 show the receiver input impedance of the T7903 board with the power off (state F1) and with the power on (state F3), respectively. There was good margin to the template in both tests.

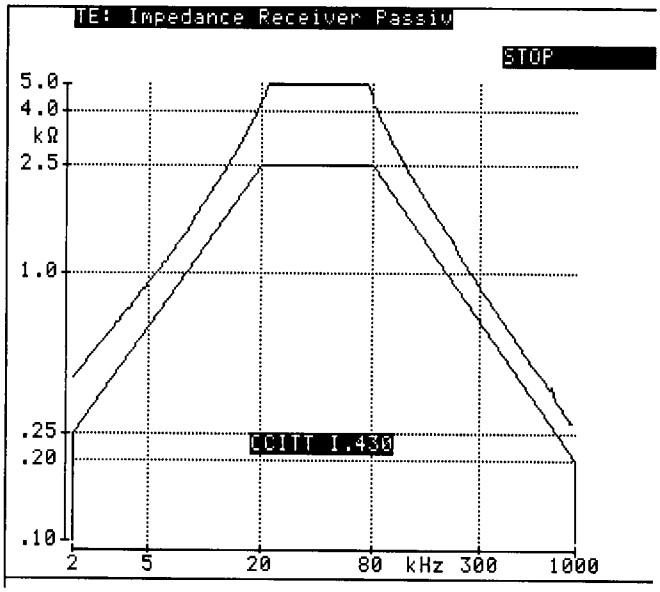


Figure F-23. Receiver Input Impedance, Power Off

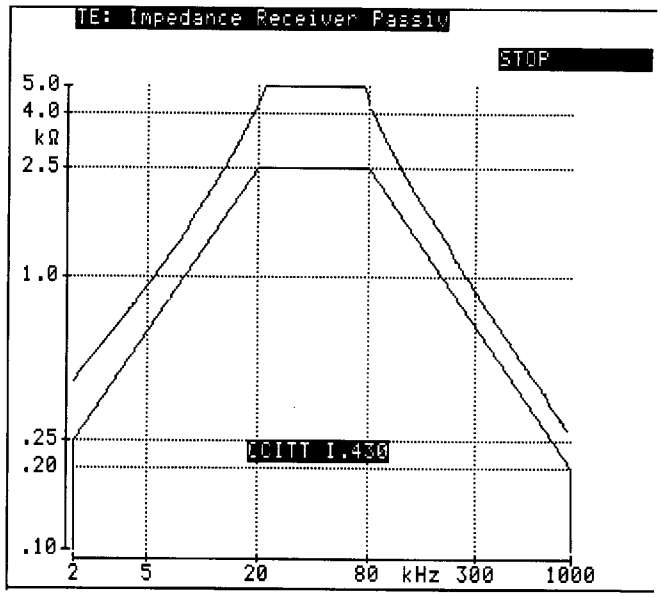


Figure F-24. Receiver Input Impedance, Power On

Table F-3 gives the results for the input (receiver) peak current test. Good margin was maintained to the 0.6 mA limit for both test conditions.

Table F-3. Input Peak Current Test Results

TE State	Frequency	Pass Limit	Result
F1	96 kHz	0.6 mA	0.429 mA
F3	96 kHz	0.6 mA	0.371 mA

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Requirements for NT Network Ports

For the most part, I.430 requirements for an NT are the same as for a TE, but there are some notable differences, as described below.

Transmitter Differences:

- The 1 MHz corner of the NT impedance template is slightly higher than for a TE.
- There is no peak current requirement for NT transmitters.
- There are no 400 Ω or 5.6 Ω tests for NTs.

Receiver Differences:

- The 1 MHz corner of the NT impedance template is slightly higher than for a TE.
- The peak current requirement for NT receivers is lowered to 0.5 mA.

The impedance template difference will slightly reduce the capacitance budget at 1 MHz. But, because the standard ISDN cord is not required for an NT, this change has little effect. The same is true for the peak current limit of 0.5 mA.

There is only one change to the circuit in Figure F-10 for NT support. On the transmit side, the MOSFETs in the transformer center tap are not needed, since there is no NT transmitter peak current requirement. Note that the MOSFETs would not affect operation for an NT, and could be used if desired. An application in which this is necessary would be for a network port that is to be software configurable as either an NT or TE connection.

Conclusions

This application brief describes T7903 ISDN S/T line interface circuitry and how several important ITU-T I.430 specifications impact it. EMI, overvoltage, and safety considerations are also included. A recommended line interface circuit is shown. I.430 layer 1 test results are presented for a PC-based ISDN adapter card design using the recommended circuit. These results verified that the recommended line interface circuit, when used with proper board layout techniques, is a viable solution for international ISDN applications.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Component List

Table F-4 lists the description, manufacturer, part number, and comments for the components shown in Figure F-10.

Table F-4. T7903 Interface Circuit Parts List

Component Designation in Figure F-10	Description	Part Number	Manufacturer	Comments
R1, R2	10 Ω, 1%, 0.125 W resistor	—	—	R1 and R2 are specified at 1% to ensure that pulse amplitude requirements are met.
R3, R4	5 Ω, 1%, 0.25 W resistor	—	—	R3 and R4 are specified at 1% to ensure that pulse amplitude requirements are met. These limit current during overvoltage conditions.
R5, R6	10 Ω, 10%, 0.25 W resistor	—	—	R5 and R6 limit current during overvoltage conditions.
R7, R8	10 kΩ, 10%, 0.125 W resistor	—	—	These combine with internal resistors to determine receiver sensitivity.
R9	100 kΩ, 10%, 0.125 W resistor	—	—	Pull-up for NMOS inverter.
D1—D8	Diode	1N-4151	*Philips, National Semiconductor*[1], etc.	Low-capacitance diodes used to shunt overvoltage.
ZD1, ZD2	Zener transient voltage suppressor	1.5SMC6.8AT3	*Motorola*	A 6.8 V zener was used because of its good availability.
Q1, Q2	P-channel MOSFET	BST84	*Philips*	Similar surface-mount types are available. On resistance is important.
Q3	N-channel MOSFET	BST80	*Philips*	Used as an inverter. Parameters are not critical.
T1, T2	2.0:1 transformer	2776E	Lucent Technologies	—
C1	0.1 µF capacitor	—	—	—
T3	Common-mode EMI choke	PE65554	*Pulse Engineering*	Similar chokes manufactured by Filmag, *Coilcraft*[2], *Vacuumschmelze*, etc.

1. *National Semiconductor* is a registered trademark of National Semiconductor Corporation.
2. *Coilcraft* is a trademark of Coilcraft, Inc.

Appendix F. Application Brief, Designing the ISDN Line Interface Circuitry for the T7903 (continued)

Standards

The following is a list of relevant ISDN, safety, EMI, and immunity standards.

- ANSI T1.605-1991 ISDN Basic Access Interface for S and T Reference Points (Layer 1 Specification)
- ITU-T Recommendation I.430 Basic User-Network Interface; Layer 1 Specification
- EN 41003 Particular Safety Requirements for Equipment to be Connected to Telecommunications Networks
- prEN 50096 ISDN; Equipment with ISDN User-Network Interface at Basic and Primary Rate-EMC Requirements
- EN 60950 Safety of Information Technology Equipment, Including Electrical Business Equipment
- ETSI ETS 300 012 ISDN Basic User-Network Interface; Layer 1 Specification and Test Principles
- ETSI prETS 300 047 ISDN; Basic Access-Safety and Protection
- IEC 801-2 through 5 Electromagnetic Compatibility for Industrial-Process Measurement and Control Equipment Parts 2-5
- *UL* 1950 Safety of Information Technology Equipment, including Electrical Business Equipment

Sources for Standards

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112-5704 U.S.A.
phone (Continental U.S.): 1-800-854-7179
phone (International): (303) 792-2181

Test Firms

Various test firms are available that can help with design and engineering, precertification testing, and full certification. The following are a few located in the U.S.:

***Wandel & Goltermann* ATE Systems GmbH & Co.**
3000 Aerial Center, Suite 110
Morrisville, NC 27560 U.S.A.
phone: (919) 460-3000
FAX: (919) 460-3030

- *Wandel & Goltermann* ATE Systems specializes in ISDN Layer 1 testing for the S_0 reference point in accordance with CTS2 and ETS 300 012 requirements. They develop the test hardware and software used by many PTTs in Europe, and provide design verification testing using these test platforms.

TUV Product Service
19035 Wild Mountain Rd.
Taylor's Fall, MN 55084-1758
phone: (612) 583-3322

- TUV Product Service provides accredited (FCC, TUV, VDE, etc.) EMI, safety, and immunity testing.

Communication Certification Laboratory (CCL)
1940 West Alexander St.
Salt Lake City, UT 84119-2039
phone: (801) 972-6146

- CCL provides accredited testing services.

Appendix G. Disabling Plug and Play on the T7903

Introduction

In most ISA-based systems, T7903 pin ENPNP (pin 69) is strapped to V_{DD}, enabling the chip's Plug and Play mode. When powered up in this mode (or after hardware reset), the T7903's ISA interface is initially disabled. The host must initiate a complete Plug and Play configuration sequence to assign an interrupt request pin and an I/O base address for the chip and to activate its ISA interface. In Plug and Play PCs, this configuration sequence is performed by either the BIOS, the operating system, or sometimes both. In non-Plug and Play applications, the host microprocessor is responsible for the configuration sequence. The advantages of using Plug and Play in PC applications is obvious, but even in non-Plug and Play systems, there are reasons for using this feature. For instance, no external address decoder is required since the Plug and Play interface uses programmable decoding. But, there are instances when disabling the Plug and Play feature is useful, such as when the device is used on the target side of a PCI bridge chip or when the software overhead of programming the Plug and Play interface is undesirable. Also, the T7903 supports only one Plug and Play logical device, but support may be required for multiple logical devices on a board. In this case, the T7903 can be used (with Plug and Play disabled) in conjunction with an off-the-shelf Plug and Play chip. By strapping ENPNP to V_{SS}, the T7903's Plug and Play interface is completely disabled and the device is configured for connection to general-purpose 16- or 8-bit processor interfaces.

Appendix G. Disabling Plug and Play on the T7903 (continued)

System Connection When Disabling Plug and Play

When Plug and Play is disabled on the T7903, the I/O base address defaults to 0x0000, IRQ15 (pin 120) is enabled as the interrupt request lead (all other IRQs are 3-stated), and the microprocessor interface is fully active. Figure G-1 shows a typical connection. Four microprocessor address lines are used to address the 16-byte register space inside the T7903.

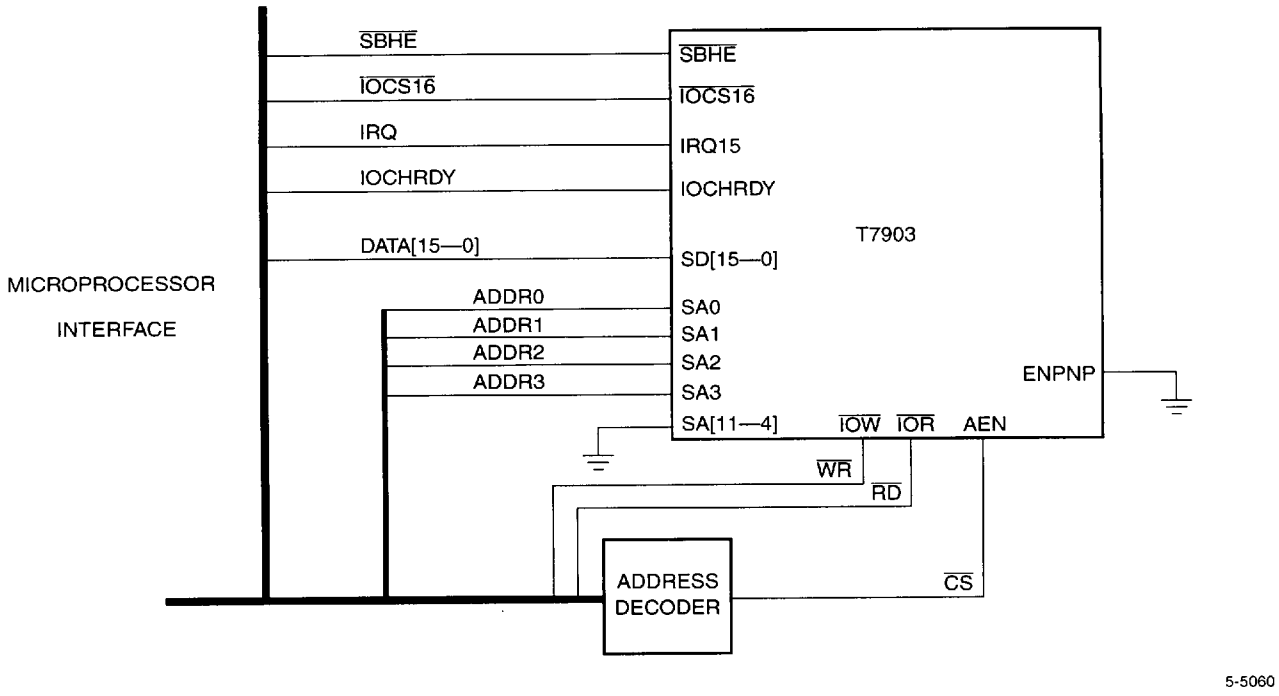


Figure G-1. Typical System Connection for T7903 with Plug and Play Disabled

The remaining address lines from the microprocessor can be used to decode a chip select signal ($\overline{CS}$ in Figure G-1) that should be connected to the T7903's AEN input (pin 124). All bus accesses will be ignored by the T7903 unless AEN is asserted low. Since the T7903 has a base I/O address of 0x0000 when Plug and Play is disabled, address inputs SA[11—4] should be connected to Vss. IRQ15 is connected to the microprocessor's interrupt request input. T7903 inputs $\overline{IOW}$, $\overline{IOR}$, and $\overline{SBHE}$, and outputs $\overline{IOCS16}$ and IOCHRDY have the same function and timing as they do when the chip is used in Plug and Play mode.

Extended I/O chip select mode is not supported when Plug and Play mode is disabled; thus pins 79 and 80 become PIO4 and PIO5, respectively. No straps are required on these pins since their PNPID function is not used. Note that ENPNP is sampled only during hardware reset, which occurs at powerup and when the RESET pin is asserted high (not when software reset is asserted).

Appendix H. Using SRAM in Place of DRAM for the T7903

Introduction

The T7903 requires external memory for storage of command and interrupt queues and for buffering data to and from the serial interfaces. To minimize address pin requirements and cost, while simultaneously providing the ability to address large memory spaces, DRAM was originally chosen for use with the T7903. The minimum amount of DRAM required is application dependent, with the maximum addressable memory size being 1 Mbyte. Since DRAM availability and cost may be a concern, this appendix describes a circuit that can be used to connect SRAM to the T7903's DRAM interface.

The SRAM Circuit

Figure H-1 shows a circuit to interface a 32 Kbyte SRAM to the T7903's DRAM interface.

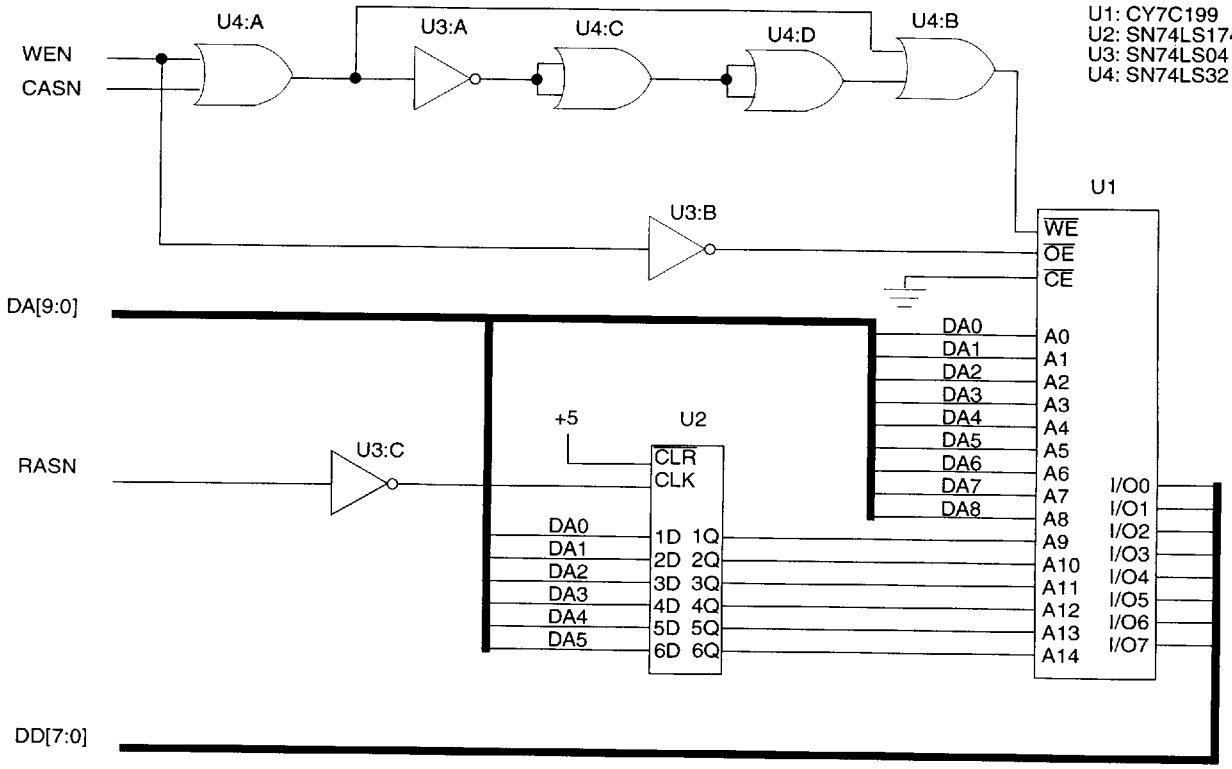


Figure H-1. Circuit to Interface SRAM to the T7903

All signals on the left side of the figure come from the T7903 DRAM interface pins. A separate access to SRAM is generated for each column address strobed by the T7903 during fast page mode DRAM accesses. Device U2 (SN74LS174) contains six D-type flip-flops that are used to latch the six least significant row address bits out of the T7903 at the start of each memory access. These six row address bits, in combination with the nine column address bits, are used to create a 15-bit address necessary to access up to 32 Kbytes of SRAM. Devices U4 (SN74LS32) and U3A (SN74LS04) are used to generate SRAM write strobes for each falling edge of the column address strobe ($\overline{CAS}$) driven by the T7903.

The SRAM circuit was designed for use with SRAMs having 20 ns or faster access time. The SRAM shown in Figure H-1 is a Cypress Semiconductor CY7C199. Note that larger SRAMs are easily supported by latching additional row address bits (requiring another SN74LS174 device).