National Semiconductor

PRELIMINARY

TP3421 ISDN S/T Interface Device with GCI (General Circuit Interface)

General Description

The TP3421 S Interface Device (SID™) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on National's advanced 1.5 micron M²CMOS process, and requires only a single +5V supply. All functions specified in CCITT recommendation I.430 and ANSI T1.605-1988 for ISDN Basic Access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in a TE (Terminal Equipment), in an NT-1 or NT-2 (Network Termination) or as a PABX line-card or trunk-card device.

As specified in I.430, full-duplex transmission at 192 kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. 2 'B' channels, each of 64 kb/s, and 1 'D' channel at 16 kb/s are available for users' data. In addition, the TP3421 provides the 800 b/s "S1" & "Q"multiframe channels for Layer 1 maintenance.

All I.430 wiring configurations are supported by the TP3421 SID, including the "passive bus" for up to 8 TE's distributed within 200 meters of low capacitance cable, and point-to-point and point-to-star connections up to at least 1500 meters (24AWG). Adaptive receive signal processing ensures low bit error rates on any of the standard types of cable commonly found in premise wiring installations when tested with the noise sources specified in I.430.

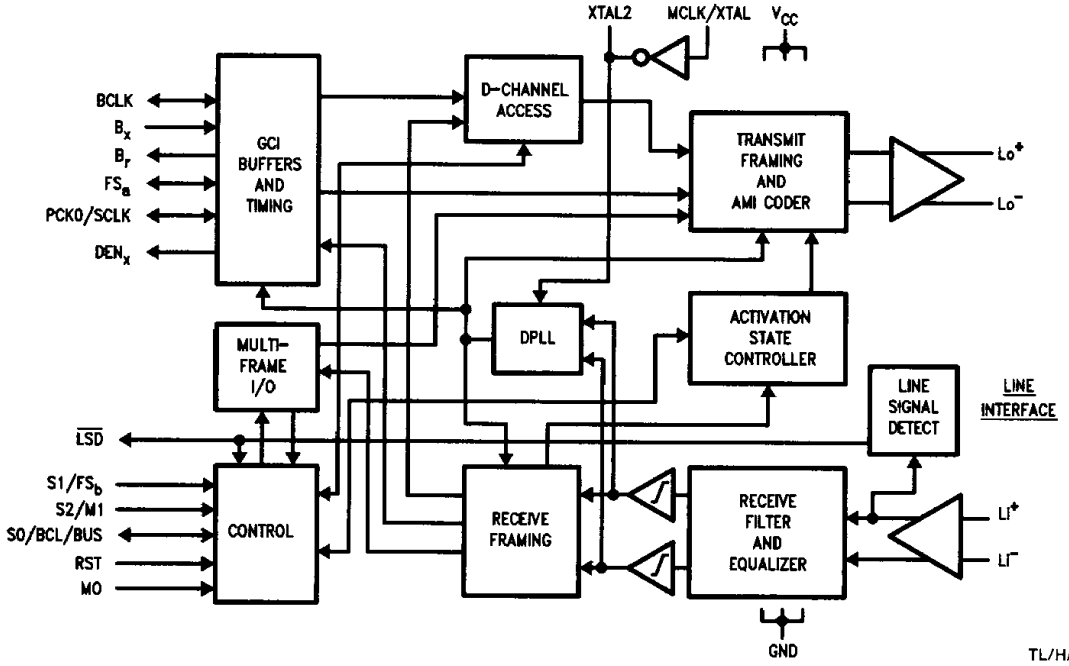
Features

- 2B + D 4-wire 192 kb/s transceiver
- Selectable TE or NT mode
- Provides all CCITT I.430 layer 1 functions
- Exceeds I.430 range: 1.5 km point-to-point
- Adaptive receiver for high noise immunity
- Adaptive and fixed timing options for NT-1
- Clock resynchronizer and elastic buffers for NT-2/LT
- Slave-slave mode for NT-2 trunks
- S and Q channels with automatic 3x checking
- GCI (General Circuit Interface) compatible
- TP3054/7 Codec/filter Combo compatibility
- Single +5V supply
- 20-pin package

Applications

- Same Device for NT, TE and PBX Line Card
- Point-to-Point Range Extended to 1.5 km
- Point-to-Multipoint for all I.430 Configurations
- Line Monitor Mode for Test Equipment

Block Diagram



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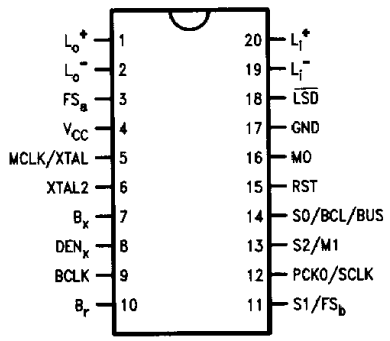
Connection Diagrams

TP3421 SID



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Top View

Order Number TP3421J or TP3421N
See NS Package Number J20A or N20A

Pin Descriptions

Note: For definitions of the modes TEM, TES and NT, see the Initialization section.

Name	Description
GND	Negative power supply pin, normally 0V (ground). All analog and digital signals are referenced to this pin.
V_{CC}	Positive power supply input, which must be +5V ±5% relative to GND.
MCLK/XTAL	The 15.36 MHz Master Clock input, which requires either a crystal* to be tied between this pin and XTAL2, or a CMOS logic level clock input from a stable source. When using a crystal, a total of 33 pF load capacitance to GND must also be connected.**
XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, and 33 pF of load capacitance to GND.**
BCLK	The Bit Clock pin, which determines the data shift rate for 'B' and 'D' channel data at the GCI. When NT mode or TES mode is selected, BCLK is a TTL/CMOS input which may be any multiple of 8 kHz from 256 kHz to 4.096 MHz. It need not be synchronous with MCLK. When TEM mode is selected, this pin is a CMOS output at 1.536 MHz This clock is phase-locked to the received line signal and is synchronous with the data on B_x and B_r.
FS_a	In NT modes and TES mode, this pin is the GCI Frame Sync pulse TTL/CMOS input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data into B_x. In TEM mode only, this pin is a digital output pulse which defines the B1 channel at both B_x and B_r.
B_x	TTL/CMOS input for 'B' and 'D' channel data to be transmitted to the line; must be synchronous with BCLK.
B_r	n-channel output for 'B' and 'D' channel data received from the line which is synchronous with BCLK. When not shifting data, this pin is high-impedance; a pull-up resistor to V_{CC} is required.
DEN_X	In TEM and TES modes, this pin is a CMOS output which is normally low and pulses high to indicate the active bit-times for 'D' channel Transmit data at the B_X input. It is intended to be gated with BCLK to control the shifting of D-channel data from a Layer 2 device to the TP3421 transmit buffer. In NT modes, this pulse occurs in every 8 KHz frame and indicates the location of D channel data input on the B_X pin.
RST	The Reset pin, which must be pulled low at power-on Reset and for normal operation. A high-going pulse on this pin will reset the device in a configuration determined by the Configuration pins.
PCKO/SCLK	In TEM and NT modes this is PCKO, which is a 32 kHz clock output synchronized to the GCI clocks; it is provided for synchronization of a switching regulator in line-powered equipment. In TES mode this is the SCLK output, which is a 1.536 MHz clock locked to the received line signal and intended to be used as the BCLK source. When used on a multi-channel line card, this output may be commoned with the SCLK outputs of other transceivers. A detector circuit ensures that this pin will stay high-impedance to prevent conflict if any other device is driving the SCLK.
$\overline{LSD}$	The Line Signal Detect output, an n-channel open-drain output which is normally high-impedance, but pulls low when the device is powered down and a received line signal is detected. It is intended to be used to "wake-up" a microprocessor from a low-power idle mode. This output is high impedance when the device is powered up.
L_o+, L_o-	Transmit AMI signal differential outputs to the line transformer. When used with a 2:1 step-down transformer, the line signal conforms to the output pulse masks in I.430.
L_i+, L_i-	Receive AMI signal differential inputs from the line transformer. The L_i- pin is also the internal voltage reference pin, and must be decoupled to GND with a 10 μF capacitor in parallel with a 0.1 μF ceramic capacitor.

*Crystal specification: 15.36 MHz parallel resonant; $R_s \leq 150\Omega$, C_L = 20 pF and C_O < 7 pF.
**The 33 pF includes any board capacitance.

Pin Descriptions (Continued)

CONFIGURATION PINS

M0 GCI Mode Selection input pin. To select GCI channel 0 connect M0=0; pin M1 must be used to select TEM or NT1 Mode. To select GCI multiplexed mode connect M0=1; the GCI channel is then selected by pins S0, S1 and S2, and the Control Register must be used to select TE or NT mode.

S0/BCL/BUS The function of this pin is dependent on the device mode selected via the MO pin and the Control Register, as follows:

- S0: in NT modes, and if M0=1, this is the S0 input pin for the lsb of the 3 pin GCI channel selection.
- BUS: in NT modes, and if M0=0, this pin is the the BUS select input pin for use in NT−1 applications: when BUS=0 fixed timing recovery is selected for use on passive bus wiring, and when BUS=1 adaptive timing recovery is selected for use on point-to-point and extended passive bus wiring.
- BCL: In TEM mode only, this pin is an output BCLK at 768 kHz. It is used as the $BCLK_x$ input to the TP3054/7 or TP3075/6 Codec/filter Combos, which clock data at a rate of 1 bit per BCLK cycle.

S1/FS_b

- S1: if M0=1 only (GCI multiplexed mode), this is an input pin for the GCI channel selection.
- FS_b: if M0=0 and M1=0 (TEM mode), this is a Frame Sync output pulse which indicates the active slot for the B2 channel on the GCI.

S2/M1

- S2: if M0=1 only, (GCI multiplexed mode), this is an input pin for the msb of the GCI channel selection.
- M1: if M0=0 this pin is the selection for TE Master or NT1 mode as follows: M1=0 selects TEM mode; M1=1 selects NT1 mode (see also BUS input).

Functional Description

INITIALIZATION

The TP3421 SID device can be operated at either end of an S Interface loop. At the upstream end the mode is called "NT" mode, in which the device is the source of INFO2 and INFO4 frames; choose this mode for PBX (NT2) line cards and NT1 equipment. A selection of adaptive or fixed receiver timing (NTA or NTF mode) must also be made, see Device Modes section.

At the downstream end of the loop the mode is called "TE" mode, in which the device is the source of INFO1 and INFO3 frames; choose this mode for terminal equipment and NT2 trunk side interfaces. Furthermore the digital interface may be configured to be either the master of the timing on the BCLK and FS pins (TE Master mode) or a slave to timing from another device (TE Slave mode). Configuring the TP3421 SID into the required operating modes is accomplished by polarization of pins, as shown in Table I; for TE Slave mode and applications in an NT2/LT the appropriate command must also be written via the GCI Monitor channel prior to the Power-Up command.

TE Master mode is selected solely by appropriate strapping of pins M0 and M1. The device is then powered up by pulling the B_x data input pin low momentarily, thereby starting the GCI clocks needed for transfer of additional control data.

When the NT1 configuration is selected, the device is powered up directly by receiving GCI clocks on BCLK and FS_a inputs (normally by the U transceiver).

When NT2 or TE Slave (TES) mode is selected, the device must first be correctly configured by writing the appropriate command via the GCI Monitor Channel, and then writing the PUP command on the C/I channel.

TABLE I. Mode Selection and Power-Up Control

	Device Mode			
Pin Name	**TE Master**	**TE Slave**	**NT1**	**LT/NT2**
M0	i = 0	i = 1	i = 0	i = 1
S2/M1	i = M1 = 0	i = S2	i = M1 = 1	i = S2
S1/FS_b	o = FS_b	i = S1	Not Used	i = S1
S0/BCL/BUS	o = BCL = 768 kHz	i = S0	i = BUS =0 for NTF =1 for NTA	i = S0
Mode Command	—	TES	—	NTA/NTF
Power-Up	Pull B_x Low	PUP Command	Send BCLK	PUP Command

Note: i means input, o means output.

Functional Description (Continued)

POWER-DOWN

Power-down is normally invoked by the PDN command in the GCI C/I Channel. Additionally, in TES, NT1 and NT2 modes, loss of GCI clocks (BCLK and/or FS_a) automatically forces power-down, and in TES, TEM and LT/NT2 modes the DI command is received in the C/I channel after the S-interface is deactivated.

In the power-down state the device retains its programmed modes, which may be changed if required via the GCI Monitor Channel. The Line Signal Detector circuit is enabled, allowing the $\overline{LSD}$ output to pull low if a wake-up signal is detected from the far-end. All other circuits are inactive, including the oscillator, and the L_O+/L_O- outputs are high-impedance. Upon power-up, all analog and I.430 circuits are enabled, the crystal oscillator starts and the activation state machine is reset. The $\overline{LSD}$ output is also disabled.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate-Mark Inversion (AMI) coding with inverted binary is used, as illustrated in *Figure 1*. This coding rule requires that a binary ONE is represented by 0V high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty-cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c.-balanced line signal.

The frame format used in the TP3421 SID follows the CCITT recommendation specified in I.430 and illustrated in *Figure 2*. Each complete frame consists of 48 bits, with a line bit rate of 192 kb/s, giving a frame repetition rate of 4 kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a 0^+ bit followed by a 0^- balance bit to indicate the start of a frame, and forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT) to the Terminal Equipment (TE) transmission direction the frame contains an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE. The last bit of this frame is used as a frame balancing bit. In the TE to NT direction, d.c.-balancing is carried out for each channel, as illustrated in *Figure 2*.

LINE TRANSMIT SECTION

The differential line-driver outputs, L_O+ and L_O-, are designed to drive a transformer with an external termination resistor. A suitable 2:1 transformer, terminated in 50Ω, results in a signal amplitude of nominally 750 mV pk on the line which fully complies with the I.430 pulse mask specifications. When driving a binary 1 symbol the output presents a high impedance in accordance with I.430. When driving a $0+$ or $0-$ symbol a voltage-limited current source is turned on. Short-circuit protection is included in the output stage; over-voltage protection is required externally, see the Applications section.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1:1 transformer, or a 1:2 transformer of the same type used for the transmit direction. At the front-end of the receive section is a continuous filter which limits the noise bandwidth. To correct pulse attenuation and distortion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics. This equalizer is always enabled when either TE mode or NT Mode Adaptive Sampling is selected, but is disabled for short passive bus applications when NT Mode Fixed Sampling is selected. An adaptive threshold circuit maximizes the Signal-to-Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 15.36 MHz. Clocks for the digital interface timing may either be derived from this recovered clock, as in TE Master mode, or may be slaved to an external source, as in the T-interface side of an NT-2 (TES mode). In TES and NT modes, re-timing circuitry on the TP3421 allows the MCLK frequency to be plesiochronous with respect to the network clock, i.e. the 8 kHz FS_a input. With a tolerance on the MCLK oscillator of 15.36 MHz ±100 ppm, the lock-in range of the DPLL allows the network clock frequency to deviate up to ±50 ppm from nominal.

When the device is powered-down (either on initial powering-on of the device or after using a PDN command), a Line-Signal Detect circuit is enabled to detect the presence of incoming data if the far-end starts to activate the loop. The LSD circuit is disabled by a Power-Up (PUP) command.

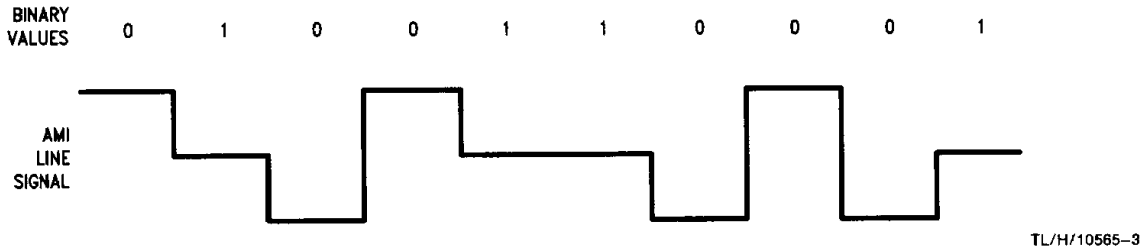

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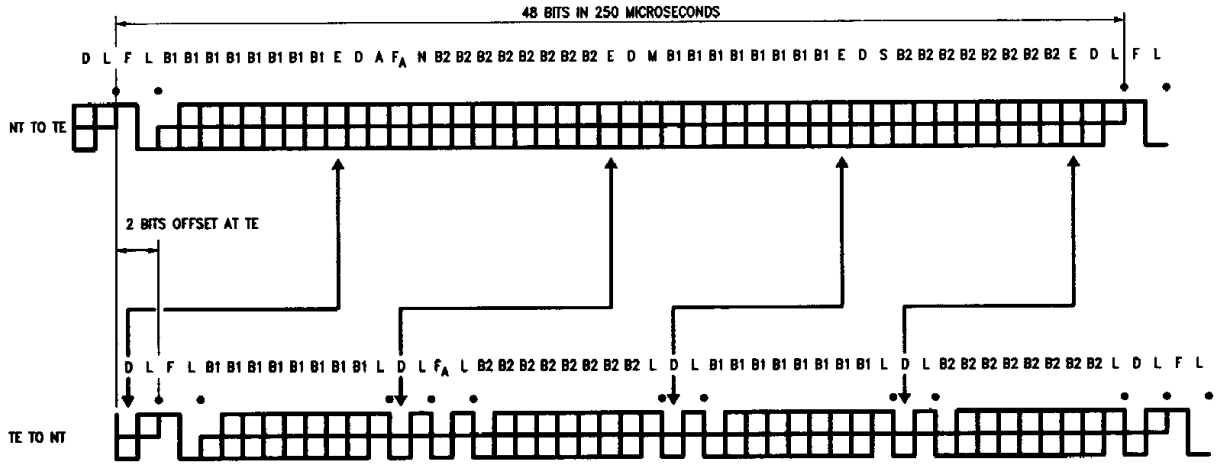
FIGURE 1. Inverted AMI Line-Coding Rule



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Legend:

F = **Framing bit**
L = **DC Balancing bit**
D = **D-channel bit**
E = **D-echo-channel bit**
F_A = **Auxiliary framing bit or Q Channel bit**
M = **Multiframe Sync bit**
N = **bit set to a binary value N = $\overline{F_A}$**
B1 = **bit within B-channel 1**
B2 = **bit within B-channel 2**
A = **bit used for activation**
S = **S Channel bit**

• Dots mark the boundaries of those parts of the frame that are independently DC-balanced

FIGURE 2. Frame Format

Functional Description (Continued)

General Circuit Interface

Enabled by tying the RST pin low at power-on reset, the GCI interface is designed for systems in which PCM and control data are multiplexed together into 4 contiguous bytes per 8 kHz frame. Furthermore, in Subscriber Line Cards and NT1–2's up to 8 GCI channels may be carried in 1 frame of a GCI multiplex, with a combined bit rate from 256 kb/s up to 3088 kb/s. Pin-programmable GCI-channel assignment for 8 GCI channels is provided.

GCI PHYSICAL INTERFACE

The interface physically consists of four wires:

— Transmit Data to Line: B_x
— Receive Data from Line: B_r
— Bit Clock at 2 cycles/bit: BCLK
— 8 kHz Frame Sync: FS_a

Data is synchronized by the BCLK and FS_a clock inputs. FS_a insures re-initialization of the time-slot counter at the beginning of each 8 kHz frame, with the rising edge of FS_a being the reference time for the first GCI channel bit. Data is clocked in both directions at half the BCLK input frequency. Data bits are output from the device on a rising edge of BCLK and sampled on the second falling edge of BCLK; unused slots are high impedance. B_r is an open-drain n-channel output, with internal detection for contention resolution on the Monitor and C/I channels between devices attempting to use the same GCI channel (typically in a TE application).

A device may be either the Master or Slave of the GCI timing. In TE Master mode it is the source of BCLK and FS_a, which are synchronized to the data received from the line. In TES Slave mode and NT modes BCLK and FS_a must be sourced externally, typically from a system backplane.

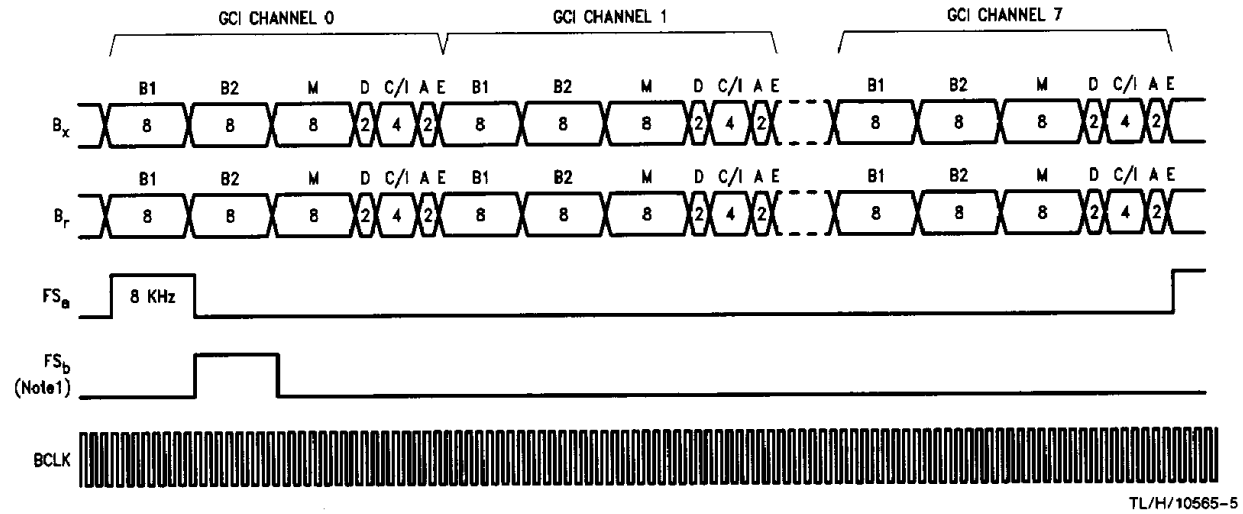
For applications such as the network side of an NT-2, e.g. a PBX trunk card, the TE Slave (TES) Mode is provided. This "slave-slave" mode allows the transmission side of the device to be a slave to the received frame timing, while the GCI is also in a slave mode i.e., FS_a and BCLK are inputs. The GCI includes elastic buffers which allow any arbitrary phase relationship between the FS_a input and the received I.430 frame. Also, jitter and low-frequency wander between the frames across the device is absorbed, up to at least 18 μs pk-pk at frequencies below 10 Hz.

TES Mode also provides a synchronized clock output (SCLK) which is phase-locked to the received line signal; SCLK may be used as the BCLK source. The SCLK outputs of a number of devices may be wire-OR'd together; a detector circuit senses the pin before the SCLK output driver is enabled to prevent more than one activated device driving the wire-OR bus.

GCI FRAME STRUCTURE

Figure 3 shows the frame structure at the GCI interface. One GCI channel supports one TP3421 using a bandwidth of 256 kbit/s, consisting of the following channels multiplexed together in an 8 kHz frame:

— B1 channel at 8 bits per frame;
— B2 channel at 8 bits per frame;
— Monitor (M) channel at 8 bits per frame;
— Signalling and Control (SC) channel, which is structured as follows:
  D channel at 2 bits per frame;
  C/I channel at 4 bits per frame;
  A bit, for acknowledgement of M channel bytes;
  E bit, which indicates the end of the byte.



Note 1: In TE Master Mode only.

FIGURE 3. GCI Interface Frame Structure (Showing 8-Channel Multiplex with BCLK = 4.096 MHz)

Functional Description (Continued)

General Circuit Interface (Continued)

For line card applications such as PBX's (LT/NT2 mode on the line side or TE Slave mode on the trunk side) multiple GCI channels (32 bits each) may be multiplexed on B_X and B_r. On a typical 2.048 Mb/s time-division multiplexed interface, 8 GCI channels may be multiplexed with a BCLK of 4.096 MHz. GCI channel selection is by means of strapping the S2, S1 and S0 pins high or low, as shown in Table II.

TABLE II. GCI Channel Programming

S2	S1	S0	Channel Number	Timeslots
0	0	0	0	0–3
0	0	1	1	4–7
0	1	0	2	8–11
0	1	1	3	12–15
1	0	0	4	16–19
1	0	1	5	20–23
1	1	0	6	24–27
1	1	1	7	28–31

GCI Monitor Channel

The Monitor channel (byte 3) is used for the system controller to access the Control Register functions shown in Table III, and for the device to report changes in the Multiframe Receive Register, as listed in Table IV. Each access to or from one of the listed registers requires a 1-byte data read or write operation. As shown in Tables III and IV, this byte from the originating device contains both a function address and a data field. In addition a protocol is used, based on the E and A bits in byte 4, to provide an acknowledgement of each Monitor channel byte in either direction, see *Figure 4*.

When no Monitor Channel message is being transferred the E bit, and the A bit in the reverse direction, are both high-impedance (and pulled high by the external resistor if no other device is active in that channel). To initiate a transfer, the sending device first verifies that it has received the A bit = 1 for at least 2 consecutive GCI frames from the other device before starting the transfer. It then sends the byte in the Monitor channel, with the associated E bit = 0, and repeats the byte in the next GCI frame. Normally, the receiving device will verify receiving the same byte in 2 consecutive frames and acknowledge this by setting A = 0 for at least 2 frames. If not, the message is aborted by sending A = 0 for only 1 frame.

On detecting the acknowledgement, the sending device then sends E = 1 to indicate this is the last (and only) byte of the transfer. The receiver acknowledges by sending A = 1 in the following frames. If a Monitor channel message originated by the TP3421 is aborted, it will repeatedly attempt the transfer until it is successfully acknowledged.

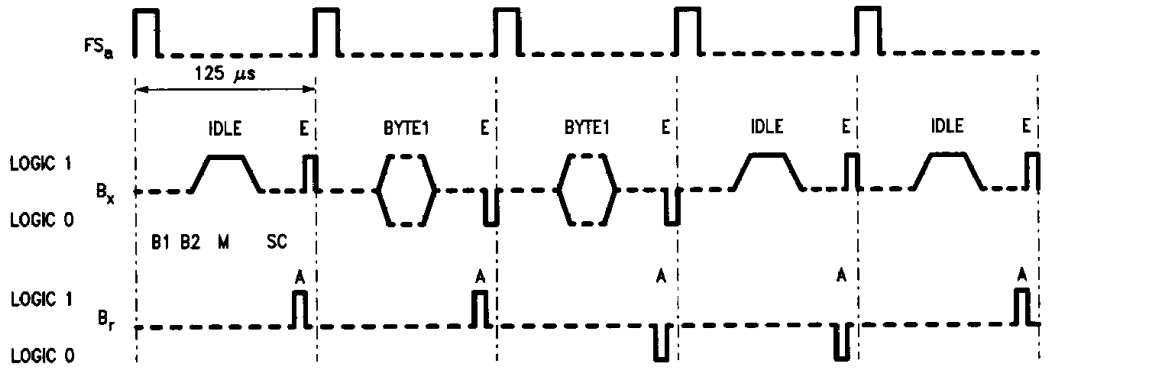


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FIGURE 4. GCI Monitor Channel Protocol

Functional Description (Continued)

TABLE III. Monitor Channel Control Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Device Modes									
*NT Mode, Adaptive Sampling	NTA	0	0	0	0	0	1	0	0
NT Mode, Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Slave Mode	TES	0	0	0	0	0	1	1	0
TE Master Mode	TEM	0	0	0	0	0	1	1	1
Monitor Mode Activation	MMA	0	0	0	1	1	1	1	1
B1 Channel Enable/Disable									
B1 Channel Enabled	B1E	0	0	0	1	0	1	0	0
*B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enable/Disable									
B2 Channel Enabled	B2E	0	0	0	1	0	1	1	0
*B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
B Channel Exchange									
*B Channels Mapped Direct, B1 to B1, B2 to B2	BDIR	0	0	0	0	1	1	0	0
B Channels Exchanged, B1 to B2, B2 to B1	BEX	0	0	0	0	1	1	0	1
End of Message Indication									
*EOM Indication Enabled	EIE	0	0	0	1	0	0	0	0
EOM Indication Disabled	EID	0	0	0	1	0	0	0	1
Multiframe Circuit									
Multiframe Circuit Enabled	MCE	0	0	0	1	0	0	1	0
*Multiframe Circuit Disabled	MCD	0	0	0	1	0	0	1	1
Multiframe Receive Message 3x Checking									
*Enable 3X Checking	EN3X								
Disable 3X Checking	DIS3X								
Multiframe Transmit Register									
Write to Multiframe Transmit Register	MFT	0	0	1	1	M1	M2	M3	M4
Loopback Test Modes									
Loopback B1 towards Line Interface	LBL1	0	0	0	1	1	0	0	0
Loopback B2 towards Line Interface	LBL2	0	0	0	1	1	0	0	1
Loopback 2B + D towards GCI	LBS	0	0	0	1	1	0	1	0
Loopback B1 towards GCI	LBB1	0	0	0	1	1	1	0	0
Loopback B2 towards GCI	LBB2	0	0	0	1	1	1	0	1
*Clear All Loopbacks	CAL	0	0	0	1	1	0	1	1

*Indicates initial state following power-on.

TABLE IV. Monitor Channel Status Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Multiframe Receive Register Requires Service	MFR	0	0	1	1	M1	M2	M3	M4

Functional Description (Continued)

DEVICE MODES

NTA — NT Mode, Adaptive Sampling should be selected when the device is in an NT on any wiring configuration up to the maximum specified length for operation. Multiple terminals, if required, must be grouped within approximately 100 meters of each other (depending on cable capacitance, see I.430). The GCI is a slave to external BCLK and FS sources.

NTF — NT Mode Fixed Sampling may be selected when the device is in an NT on a passive bus wiring configuration up to approximately 200 meters in length (depending on cable type). In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed, to enable multiple terminals (nominally up to 8) to be connected anywhere along the passive bus. Again, the GCI is a slave to external BCLK and FS sources.

TEM — TE Master Mode should be selected when the device is in a TE. The TP3421 is then the source of the BCLK and FS signals, and access to the Transmit D channel, including the priority and contention resolution control, is enabled as described in the section on TE Mode D-Channel Access.

TES — TE Slave Mode, otherwise known as "Slave-slave" mode, should be selected when the device is used on the T-interface side of an NT-2. The GCI is then driven by BCLK and FS sources in the NT-2. Data buffers and a clock re-synchronizer enable this interface to function with jittering sources for BCLK and FS. All D Channel access control circuitry is disabled, i.e. D Channel data at the B_X input is continuously transmitted to the line; there is no monitoring of the D-echo channel from the network direction. Also, the SCLK function is enabled at the PCKO/SCLK pin.

MMA — Intended for test equipment applications, this instruction allows the receive line interface ($L_I \pm$) to be connected to the TE-to-NT direction twisted pair and to activate on the received INFO 3 signals while being the master of the GCI. The received 2B + D can then be passively monitored (the line transmit output $L_O \pm$ would not be connected). TE Master mode must be selected prior to power-up by connecting M0 = 0 and M1 = 0.

B CHANNEL CONTROL

BDIR) / BEX) — These commands provide for the exchange of data between the B1 and B2 channels as it passes through the device (Note 1).

Note 1: When enabling a B channel in conjunction with the BEX Command, the channels are referenced at the Digital System Interface, not the line interface e.g. to connect the B1 slot on the DSI with the B2 slot on the line interface, use the BEX and B1E commands.

B1E) / B1D) / B2E) / B2D) — When either or both B channels are disabled, binary 1s are transmitted on the line in those B channel bit positions, regardless of data at the B_X input, and the B_r output is high-impedance in those bit positions.

MULTIFRAME TRANSMIT REGISTER

MFT / MCE / MCD — With the device in TE Mode, data entered in bit positions M1, M2, M3 and M4 is transmitted towards the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT Mode, data entered in the M bit positions is transmitted towards the TE in multiframe bit positions S11, S12, S13 and S14 respectively. The Multiframe Channel must be enabled by an MCE command to use these channels; an MCD command will disable them, (see Multiframe Maintenance Channel section).

MULTIFRAME MESSAGE CHECKING

EN3X / DIS3x — EN3x enables the checking of certain S and Q channel messages before generating the MFR indication. DIS3x disables this circuit, so that the received S or Q word generates MFR once per multiframe (see Multiframe Maintenance Section).

LOOPBACK TEST MODES

Three classes of loopback mode are available on the SID, selected by writing the appropriate Control instruction.

LBS — This loopback at the system interface is a full loopback of the 2B + D channels from the B_X input to the B_r output. It may be set when the device is either activated, in which case it is transparent (i.e. the composite signal is also transmitted to the line), or when it is deactivated.

LBL1/2 — These loopbacks turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.

LBB1/2 — These loopbacks at the Digital System Interface loop the B1 (LBB1) or the B2 (LBB2) channel data from the B_X input to the B_r output. The B_X input data is also sent to the line transmit output.

EXTERNAL SELF-ACTIVATING LOOPBACK

A quick self-test of the device is possible by connecting together the line sides of the transmit and receive transformers. NTA or NTF mode must be selected, and the device can then be activated by the normal command sequence (Note 2).

Note 2: This test mode is not possible by direct connection of $L_O \pm$ and $L_I \pm$ pins due to incompatible internal bias voltages.

MONITOR CHANNEL STATUS INDICATORS

MFR — This message indicates when the Multiframe receive data buffer requires servicing, after 1 or 3 consecutive identical Multiframe words have been detected, see Table IV. All Multiframing functions can be disabled via an MCD Command if desired.

Functional Description (Continued)

GCI C/I CHANNEL

The C/I (Command/Indicate) channel in GCI byte 4 is used solely to access the Activation Control and Status indicators in the TP3421. Table V shows the coding of the 4 bit messages. A change in status is repeated in the transmit C/I channel in at least 2 consecutive GCI frames, while a change in received message is verified in 2 consecutive GCI frames before taking the appropriate action.

TABLE V. C/I Control Channel Coding

Code	TE Master		TE Slave		NT1		NT2	
C4C3C2C1	Ind.	Com.	Ind.	Com.	Ind.	Com.	Ind.	Com.
0000	DR	PUP/DR	DR	PUP/DR	TIM	DR	TIM	PUP/DR
0001	X	PDN	X	PDN	X	X	X	PDN
0010	X	X	X	X	X	X	X	X
0011	EOM (1)	X	X	X	X	X	X	X
0100	EI	X	EI	X	EI	RSY	EI	X
0101	X	X	X	X	X	X	X	X
0110	X	X	X	X	X	X	X	X
0111	X	X	X	X	X	X	X	X
1000	AP	AR8	AP	AR	AP	AR	AP	AR
1001	CON (1)	AR10	X	X	X	X	X	X
1010	X	ARL	X	ARL	X	ARL	X	ARL
1011	X	X	X	X	X	X	X	X
1100	AI8	X	AI	X	AI	UAR	AI	UAR
1101	AI10	X	X	X	X	X	X	X
1110	AIL	X	AIL	X	AIL	X	AIL	X
1111	DI	DI	DI	DI	DI	DI	DI	DI

(X) codes reserved

(1) codes sent only two times when event occurs.

C/I CHANNEL COMMANDS

PUP/DR When in the power-down state this is the power-up command, which powers up all the circuitry, starts the XTAL and resets the state machine to the deactivated state. In TEM mode, the GCI clocks must be started by pulling the B_X pin low prior to sending PUP/DR. The PUP/DR or DR command is also used in the power-up state as the Deactivate Request, which forces transmission of INFO 0.

PDN This is the power-down command, which forces the device to first send the DI indicator in the C/I channel on B_T for 2 GCI frames, and then to power-down at the end of the assigned GCI channel. It should only be used after the TP3421 has been put in a known state, e.g. in a TE after a DI status has been reported, since it does not force sequencing through any of the deactivation states.

AR Used in NT and TES applications, this is the Activation Request which starts transmission of the appropriate activation sequence.

UAR Used in NT applications only, this command must be used after the AI is generated on detection of INFO 3 from the terminal(s). UAR completes the activation, causing transmission of INFO 4 frames with the 2B + D operational.

AR8 Used in TE Master mode only, this command functions as an Activate Request followed by an immediate access to the transmit D channel with a packet of the high priority class (see the section on TE Mode D-Channel Access).

Functional Description (Continued)

AR10 Used in TE Master mode only, this command functions as an Activate Request followed by an immediate access to the transmit D channel with a packet of the low priority class (see the section on TE Mode D-Channel Access).

ARL The Activate Request for Loopback, which operates a full loopback of the 2B + D channels from the B_x input to the B_r output. It may either be set when the device is activated, in which case it is transparent (the composite signal is also transmitted to the line) or when it is deactivated, in which case it is non-transparent.

DI When used as a command, DI allows the device to automatically power-down if the S Interface is already deactivated.

RSY Effective only in NT modes, and only after Activation has been completed, this instruction forces the NT to transmit INFO 2 frames instead of INFO 4, normally to allow testing at the U interface. Provided INFO 3 is still being received from the TE(s), an AI Status message will be generated and loop synchronization maintained, but 2B + D transmission is inhibited. To restore full loop activation, with the NT sending INFO 4, a UAR command is required in the normal way.

C/I CHANNEL STATUS INDICATORS

TIM Timing Request indicator, which occurs when a deactivated NT has detected a "wake-up" signal, passed a Line Signal Detect upstream and received GCI clocks. TIM acts as confirmation that the device has powered up. This indicator also occurs in an activated NT in response to a DR command.

DR Deactivate Request indicator which is generated when any of the following events occurs:

— just after power-up when the S line signal has not yet been identified;

— detection of INFO 0 on an activated (or partially activated) line;

— after a PUP command while activation is pending.

AI This is the Activation Indication generated when activation is completed in response to an AR command.

AI8 This is the Activation Indication, generated in TE Master mode only, when activation is completed in response to an AR8 command; the D channel access procedure is set in the high priority class.

AI10 This is the Activation Indication, generated in TE Master mode only, generated when activation is completed in response to an AR10 command; the D channel access procedure is set in the low priority class.

AIL This is the Activation Indication Loopback, which indicates that the complete loopback requested via an ARL command is in effect.

AP This is the Activation Pending indication, which occurs in a TE when INFO 2 or INFO 4 frames are detected. An AR command must be sent to allow activation to be completed.

EI This is the Error Indication, which occurs when loss of frame alignment is detected. Also, in a TE, if the line is already activated and the received line signal changes from INFO 4 to INFO 2 (during loop testing) this indicator is generated.

DI This is the Deactivation Indication, which is generated in response to a DI command. After the indicator is acknowledged by the A bit, the device may be powered down, by the PDN command in a TE or by stopping the GCI clocks in an NT1 or NT2.

EOM This is the End of Message indicator, which occurs when the closing flag of a D-channel packet has been transmitted by a TE on the S Interface, indicating successful completion of a packet. The generation of this code can be disabled via the Monitor Channel using the EID command.

CON This is the Contention indicator, which occurs when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision. A new AR8 or AR10 command is necessary to restart the D channel access procedure.

ACTIVATION/DEACTIVATION: TP3421 IN NT MODE

Activation (i.e. transmission and loop synchronization) may be initiated from either end of the loop. To initiate Activation from the NT, the TP3421 must be powered up (see Initialization Section), followed (Note 3) by an AR command in the C/I Channel. Network timing, i.e., an 8 kHz input to FS_a, must be present at this time. The device then begins to send data framed as INFO 2 type, in which bits in the B, D and D-echo channels are set to binary 0. These frames are detected by the TE, which replies with data framed as INFO 3 type, synchronized to received frames. A flywheel circuit in the TP3421 NT searches for 3 consecutive correctly formatted receive frames to acquire frame synchronization. If Multiframing is enabled (MIE), 60 correct frames (3 multiframes) are required to achieve full loop synchronization. When it is correctly in sync with received frames, the NT device sends AI in the C/I channel. A UAR command is required to cause the NT to send INFO 4 frames, in which the B and D channels are enabled for transmission (this command may be delayed until the upstream link indicates that it is also fully activated).

Note 3: A delay of ≥ 2 ms is recommended to ensure that all internal circuits have settled.

Functional Description (Continued)

When Activation is initiated by a TE, the TP3421 in NT mode will detect the incoming INFO 1 signal and, if it is powered-down will pull the $\overline{LSD}$ pin low, which can be used to "wake-up" a microprocessor. The device must then be powered up by the specified initialization procedure. Upon identifying the INFO 1 signal, the device sends AP in the C/I channel. An AR command is required to start sending INFO 2 frames, which allows the Activation sequence to proceed as described above.

Once Activated, loss of frame alignment is assumed by the TP3421 when a time which is equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the NT does detect alignment loss it will start to transmit INFO 2. At this point EI is sent in the C/I channel and the receiver searches to identify the incoming signal and attempt to re-acquire loop synchronization. If it successfully re-establishes synchronization with the incoming signal (INFO 3 frames), AI is sent in the C/I channel and re-activation can be completed by sending a UAR command. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, Status Indicator TIM is sent in the C/I channel, with the transmitted frames changed to INFO 0.

I.430 recommends 2 timers should be available in an NT. An Activation Request to the TP3421 should be associated with the start of an external Timer 1, if required. Timer 1 should be stopped when the AI status message is generated following successful Activation. If Timer 1 expires before AI is generated, however, the DR command should be written to the device to force de-activation. Timer 2, which is specified to prevent unintentional reactivation, is not required since the TP3421 can uniquely recognise INFO 1 frames.

ACTIVATION/DEACTIVATION: TP3421 IN TE MODE

To activate the loop with the TP3421 at the TE end the device must first be powered-up (see Initialization Section), followed by a Control Instruction type AR (Note 3). This is the Activation Request to begin transmission of INFO 1 frames after verifying that INFO 0 is being received from the NT. INFO 1 is a continuous pattern of 0+, 0−, and 6 '1's repeated. At this point the TE is running from its local oscillator and is not receiving any sync information from the NT. When the NT recognises this "wake-up" signal, it begins to transmit INFO 2, synchronized to the network clock (following activation of the "U" interface, if applicable). This enables the phase-locked loop in the TE's receiver to correctly identify bit timing from the NT and to synchronize its own transmission to that of the NT. On identifying INFO 2 for 3 consecutive frames, the TE changes its transmit data to INFO 3 and awaits the return of INFO 4 from the NT. Identification of INFO 4 completes the Activation sequence, which the device indicates by sending AI in the C/I channel.

When Activation is initiated by the NT, if the TP3421 in TE mode is powered down, it will pull the $\overline{LSD}$ pin low on receiving a line signal, which can be used to "wake-up" a microprocessor. The specified initialization procedure is required to enable the device to power-up, identify the received signal, and acquire bit and frame synchronization. Once INFO 2 has been identified, the TP3421 will send AP in the C/I channel. The microprocessor must respond by sending AR in order for Activation to proceed. INFO 3 frames are then transmitted. Finally, when the NT replies with INFO 4 frames, AI is sent in the C/I channel.

As in NT mode, once Activated, loss of frame alignment is assumed by the TP3421 when a time equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the TE does detect alignment loss it will cease transmitting immediately. At this point EI is sent in the C/I channel, and the receiver searches to re-acquire loop synchronization if INFO 2 or INFO 4 frames are still being received. If synchronization is re-established, AI is sent. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, the loop is de-activated, and DI is sent to indicate De-activation.

I.430 does not provide for Deactivation to be initiated by a TE. However, a power-down state may be forced if required, normally after Deactivation has been established by the network (see POWER-DOWN section).

If required, an external Timer 3 should be started when an Activation Request is sent to the TP3421. The subsequent AI indication should be used to stop the timer. If the timer expires before an AI is generated, PUP/DR must be sent to the device to force the transmission of INFO 0.

TE MODE D-CHANNEL ACCESS

In TE Master and Slave modes the TP3421 SID arbitrates access for Layer 2 Transmit frames to the D-channel bit positions in accordance with the I.430 Priority Mechanism (I.430 Section 6.1). This mechanism is to resolve contention for the D channel towards the network when 2 or more TEs are connected to a Passive Bus. The shifting of D-channel transmit data from the Layer 2 device into the SID buffer is controlled by gating the DEN_X output with BCLK. When no Layer 2 frame is pending, "1"s are always transmitted by the SID in D-bit positions at the S Interface. DEN_X output pulses are inhibited and no D-channel data is shifted into the B_X input. An external Layer 2 device requiring to start transmission of a packet should first prime its Transmit buffer such that the opening flag is ready to be shifted across the digital interface. Then a C/I command, either AR8 for a Priority Class 1 (signaling) packet or AR10 for a Priority Class 2 packet, will initiate the D-channel access sequence.

In response to the command, the DEN_X output is enabled to pre-fetch the opening flag from the Layer 2 device into the D-channel buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S Interface (in a point-to-multipoint wiring configuration) is transmitting in the D-channel. This is assured by counting consecutive "1"s in the E-bit position of frames received from the NT. At least 8 consecutive "1"s must be detected before transmission of the pending D-channel frame begins, in accordance with Table VI.

Functional Description (Continued)

TABLE VI. D-Channel Access Criteria

Number of Consecutive "1"s in the E-Channel	D-Channel Access
7	Abort. Possible re-try by the transmitting TE.
8	Signalling packet (Priority Class 1) may begin (Note 1).
9	Signalling packet may begin unconditionally.
10	Any packet type may begin (Priority Class 2) (Note 2).
11	Any packet type may begin unconditionally

Note 1: Only if, since the SID last transmitted a complete Class 1 packet, a sequence of ≥ 9 consecutive "1"s has been detected in the E-channel.

Note 2: Only if, since the SID last transmitted a complete packet of either class, a sequence of ≥ 11 consecutive "1"s has been detected in the E-channel.

If another TE is active in the D-channel, DEN_X pulses are inhibited once the opening flag is in the Transmit buffer, to prevent further fetching of transmit data from the Layer 2 device until D-channel access is achieved. As soon as the required number of consecutive E-channel "1"s has been counted, the leading 0 of the opening flag is transmitted in the next D-bit position towards the NT. DEN_X pulses are also re-enabled in order to shift D-channel bits from the Layer 2 device into the SID transmit buffer.

During transmission in the D-channel the TP3421 SID continues to compare each E-bit received from the NT with the D-channel bit previously transmitted before proceeding to send the next D-bit. In the event of a mis-match, a contention for the previous D-bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and "1"s are transmitted in all following D-bit positions. Status Indication type CON is sent in the C/I channel, and DEN_X output pulses are again inhibited.

In order to retransmit the lost packet, the Layer 2 device must begin as before, by priming its Transmit buffer with the packet header. It must also reset the C/I channel by sending the DI code to the TP3421 in at least 2 consecutive GCI frames, prior to sending a new AR8 or AR10 command.

DEN_X pulses stop immediately after receiving the closing flag on the B_X input from the layer 2 device.

Successful completion of a transmit packet is detected by the TP3421 when the closing flag is transmitted in the D channel. '1's are then transmitted in the following D bit positions. Status Indication type EOM is sent, to indicate the End of Message. Also, the Priority Access counters are decremented to the lower priority level within each priority class, in accordance with the I.430 algorithm. Priority is subsequently restored to the higher level when the specified number of consecutive 1's (9 or 11) is detected in the D-echo-bit position.

MULTIFRAME MAINTENANCE CHANNELS (S1 AND Q WORDS)

Each direction of transmission across the S Interface includes a low-speed (800 b/s) channel for loop maintenance, accessed via the control interface of the TP3421. A multiframe structure, consisting of 20 frames on the S Interface, is used to synchronize these channels and convey messages coded into 4-bit words, see Table VII. One word is transmitted downstream (NT-to-TE) in the S1 channel, and one word is transmitted upstream (TE-to-NT) in the Q channel every multiframe.

When the device is in NT mode, the MIE command enables both the transmission of the Multiframe identification algorithm (reversal of the FA/N bits every 5th frame and M bit set = 1 every 20th frame) and the generation of the MFR indication in the Monitor Channel. The algorithm is present during INFO 2 and INFO 4 frames. In TE modes this command only enables the MFR indication, since the device will always search for and synchronize to the multiframing identification bits if the NT is sending them. In all modes there is an option to enable or disable an automatic checking circuit to validate received S or Q channel words. If this circuit is enabled by the EN3X instruction, at the end of each multiframe the received 4-bit word is decoded to determine if it should generate an MFR indication immediately, or be stored until 3 consecutive multiframes have contained the same 4-bit word before an indication is generated. Table VII lists the codes which are 3-times checked. Note, however, that no other action is taken by the TP3421 in response to received codes (e.g. loopbacks are not automatically implemented); the external controller must take the necessary action. This provides the freedom to implement maintenance functions without constraints from the device, and to utilize the unassigned codes for other functions.

If the 3 times checking circuit is disabled by the DIS3X instruction, each received S or Q word generates an MFR indication once per multiframe.

The MCD command disables the transmission of the Multiframe identification algorithm in NT mode and disables the MFR indication in both NT and TE modes. Both the MCE and MCD commands can only be written to the device when it is deactivated (either powered-up or powered-down). The Multiframe Transmit Register should also be loaded with the appropriate "Idle" messages, by means of an MFT command, prior to activation.

Functional Description (Continued)

TABLE VII. Codes for Q-Channel and S1-Channel Messages with 3x Checking Enabled

Message	NT-to-TE					TE-to-NT				
	Received at TE				Number of Repetitions before MFR Message	Received at NT				Number of Repetitions before MFR Message
	S11	S12	S13	S14		Q1	Q2	Q3	Q4	
Idle (NORMAL)	0	0	0	0	3	1	1	1	1	3
Loss-of-Power Indication	1	1	1	1	1	0	0	0	0	1
STP Pass	0	0	1	0	3	—	—	—	—	—
STF Fail	0	0	0	1	3	—	—	—	—	—
ST Request (Note 1)	—	—	—	—	—	0	0	0	1	3
STI Indication	0	1	1	1	3	—	—	—	—	—
DTSE-IN	1	0	0	0	1	—	—	—	—	—
DTSE-OUT	0	1	0	0	1	—	—	—	—	—
DTSE-IN&OUT	1	1	0	0	1	—	—	—	—	—
LB1 Request	—	—	—	—	—	0	1	1	1	3
LB1 Indication	1	1	0	1	3	—	—	—	—	—
LB2 Request	—	—	—	—	—	1	0	1	1	3
LB2 Indication	1	0	1	1	3	—	—	—	—	—
LB1/2 Request (Note 2)	—	—	—	—	—	0	0	1	1	3
LB1/2 Indication	1	0	0	1	3	—	—	—	—	—
Loss-of-Received-Signal Indication	1	0	1	0	3	—	—	—	—	—
Unassigned	All Other Codes				1	All Other Codes				1

Note 1: The code "0001" will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a Passive Bus.

Note 2: The code "0011" will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a Passive Bus.

Applications Information

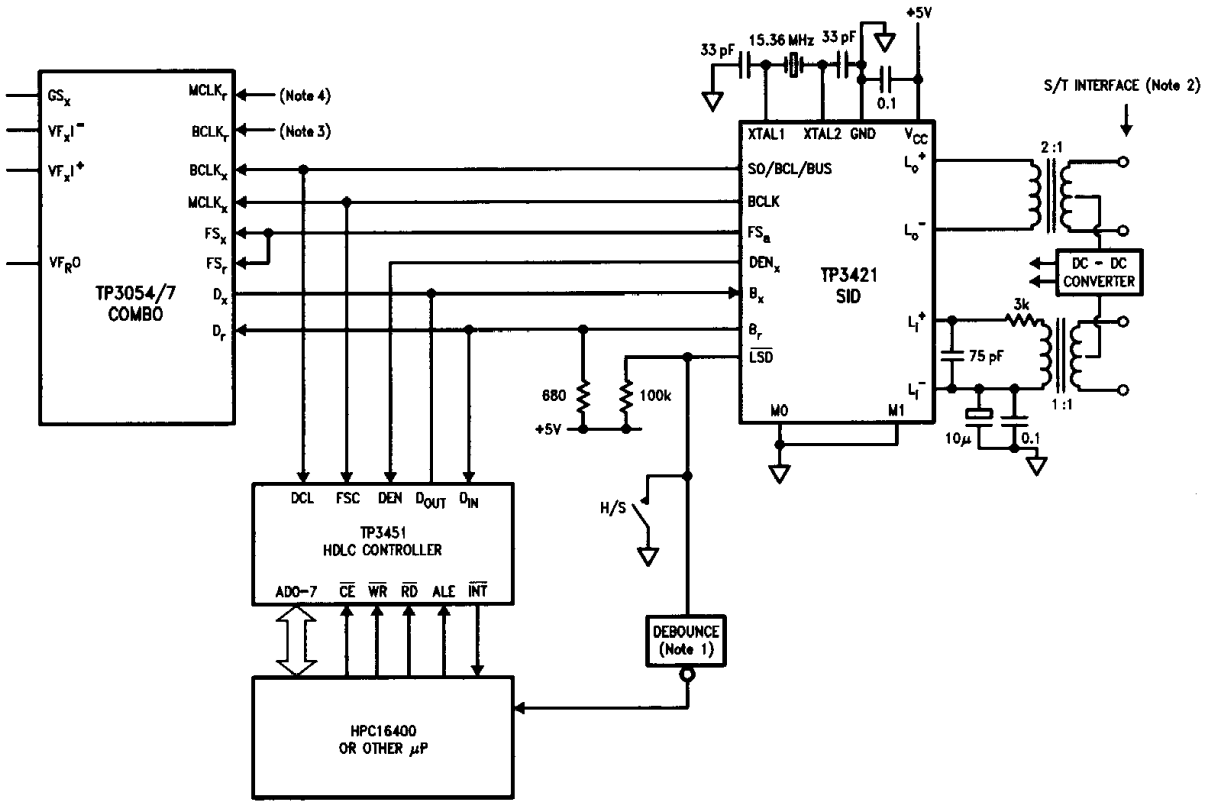
While the pins of the TP3421 SID are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A decoupling capacitor of 0.1 μF should be connected from this common point to V_{CC}. Taking care with the pcb layout in the following ways will help prevent noise injection into the receiver front-end and maximize the transmission performance:

1. keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components.
2. keep the connections between the device and the components on the $L_i\pm$ inputs short; the L_i- capacitors should be connected close to the device pins.
3. keep the connections between the device and the transformers short.

Figure 5 shows a typical application of the TP3421 in an ISDN Terminal. To provide a voice channel, the TP3054/7 Combo I Codec/filter is shown. Although these Combos clock PCM data at a rate of 1 CLK cycle per bit, direct compatibility with the GCI is provided by connecting the BCL output of the TP3421 (in TEM mode) to the $BCLK_X$ input of the Combo. Data is shifted between devices in the B1 channel at 768 kHz, with the 1.536 MHz GCI clock (BCLK) providing the MCLK for the Combo. If the network assigns the B2 channel to a voice call, the BEX command is used to exchange the B1 and B2 slots between the GCI and S/T interfaces.

For more in-depth information on a variety of applications, the TP3421 Users Manual is a comprehensive guide to the hardware and software required to meet the I.430 interface specification. Performance measurements, demonstrating compliance with I.430 and ANSI transmission requirements, are also included.



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Note 1: Only necessary if a mechanical hook switch is connected to the NMI input of the HPC.

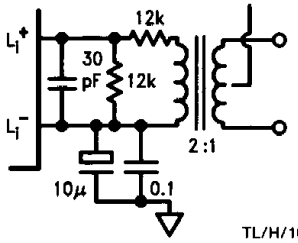
Note 2: See TP3421 User's Manual for Line Interface Protection.

Note 3: For TP3054 (μ-law) leave $BCLK_r$ open-circuit. For TP3057 (A-law) connect $BCLK_r$ low for 1-536 MHz MCLK operation. $BCLK_x$ operates at 768 kHz.

Note 4: To power-up the Combo, $MCLK_r$/PDN must be pulled low.

FIGURE 5. Typical Application in a TE and/or TA

Alternative Receive Input Using 2:1 Transformer



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at L_i, L_o Pins	V_{CC} + 1V to GND − 1V
Voltage at any Digital Input	V_{CC} + 1V to GND − 1V
Storage Temperature Range	−65°C to + 150°C
Current at L_o Pins	± 100 mA
Current at any Digital Output	± 50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are electrical testing limits at V_{CC} = 5.0V and T_A = 25°C. All other limits are design goals for V_{CC} = 5.0V ±5% and T_A = 0 to 70°C. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL Input			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL Input	V_{CC} − 0.5			V
V_{OL}	Output Low Voltage	B_r, I_L = 3.2 mA All Other Digital Outputs, I_L = 1 mA			0.4	V
V_{OH}	Output High Voltage	B_r, I_L = −3.2 mA All Other Digital Outputs, I_L = −1 mA All Outputs, I_L = −100 μA	2.4 2.4 V_{CC} − 0.5			V V V
I_I	Input Current	Any Digital Input, GND < V_{IN} < V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	B_r, $\overline{LSD}$ GND < V_{OUT} < V_{CC}	−10		10	μA
LINE INTERFACES						
R_{Li}	Differential Input Resistance	GND < L_i+, L_i− < V_{CC}	200			kΩ
CL_{Lo}	Load Capacitance	Between L_o+ and L_o−			200	pF
VOS	Differential Output Offset Voltage at L_o+, L_o−	Driving Binary 1s, 220Ω between L_o+ and L_o−	−20		+20	mV
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	All Outputs Open-Circuit		1.0		mA
$I_{CC}1$	Power Up Current	As Above, Device Deactivated (Note 1)		18.0		mA
TRANSMISSION PERFORMANCE						
	Transmit Pulse Amplitude	R_L = 220Ω Between L_o+ and L_o− (Note 2)	±1.55		±1.75	Vpk
	Transmit Pulse Unbalance	0+ Relative to 0−			±5	%
	Input Pulse Amplitude	Differential Between L_i+ and L_i−	±175			mVpk

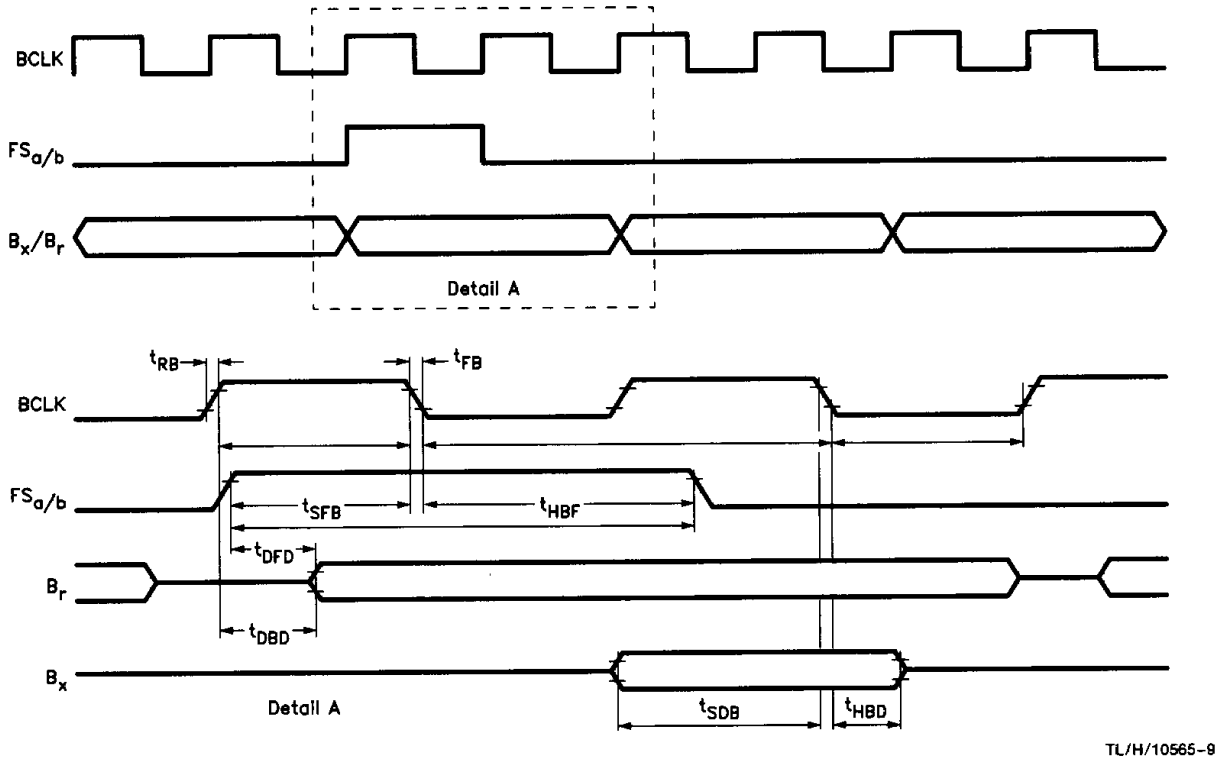
Note 1: When the device is activated and driving a correctly terminated line, I_{CC1} increases by several mA. A worst-case data pattern, consisting of all binary 0's, increases I_{CC1} by approximately 8 mA.

Note 2: The pulse amplitude at the L_o± pins allows for approximately 1 dB tranformer insertion loss to meet the 0.75V pulse mask test when the line is terminated in 50Ω.

Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FMCK	Master Clock Frequency Master Clock Tolerance		 −100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
tMH, tML	Clock Pulse Width Hi & Low for MCLK	$V_{IH} = V_{CC} - 0.5V$ $V_{IL} = 0.5V$	20			ns
tMR, tMF	Rise and Fall Time of MCLK	Used as a Logic Input			10	ns
DIGITAL INTERFACE *(Figure 6)*						
tWBH	Period of BCLK High	Measured from V_{IH} to V_{IH}	25			ns
tWBL	Period of BCLK Low	Measured from V_{IL} to V_{IL}	25			ns
tRB	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			15	ns
tFB	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			15	ns
tHBF	Hold Time, BCLK Low to FS, High or Low		25			ns
tSFB	Setup Time, FS High to BCLK Low		50			ns
tDBD	Delay Time, BCLK High to Data Valid	Load = 150 pF Plus 2 LSTTL Loads			80	ns
tDBZ	Delay Time, BCLK High to Br, Dr Disabled				50	ns
tDFD	Delay Time, FS High to Data Valid	Load = 150 pF Plus 2 LSTTL Loads, Applies if FS Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only			80	ns
tSDB	Setup Time, Data Valid to BCLK Low		0			ns
tHDB	Hold Time, BCLK Low to Data Invalid		25			ns

Timing Characteristics (Continued)



TL/H/10565–9

FIGURE 6. GCI Timing