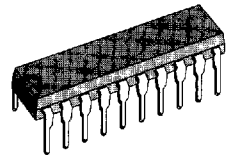
SGS-THOMSON MICROELECTRONICS

ST5420

SID-μW : S/T INTERFACE DEVICE WITH MICROWIRE/DSI

ADVANCE DATA

- SINGLE CHIP 4 WIRES 192 KBIT/S TRANSCEIVER, PROVIDES ALL CCITT I.430 LAYER 1 FUNCTIONS
- ISDN BASIC ACCESS HANDLING 144KBIT/S 2B + D TRANSMISSION
- 4 SELECTABLE DIGITAL SYSTEM INTERFACE (DSI) FORMATS
- MICROWIRE™ μW COMPATIBLE SERIAL CONTROL INTERFACE
- EXCEEDS I.430 RANGE : AT LEAST 1.5KM POINT-TO-POINT AND 200M POINT-TO-MULTIPOINT
- ADAPTIVE AND FIXED TIMING OPTIONS FOR NT
- CLOCK RESYNCHRONIZER AND DATA BUFFERS FOR NT2
- PROGRAMMABLE S&Q CHANNELS HANDLING ACCORDING TO US ANSI STANDARD FOR LAYER 1 MAINTENANCE
- OPERATING POWER CONSUMPTION < 75mW
- STAND-BY POWER CONSUMPTION < 3mW
- EASILY INTERFACEABLE WITH ST5075/6, ST5451



DIP20

DESCRIPTION

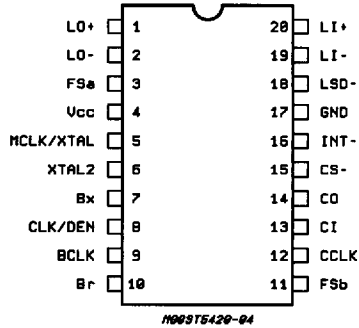
The ST5420 (SID-μW) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on SGS-THOMSON Microelectronics double metal advanced HCMOS3A process, and requires only a single + 5V supply. All functions specified in CCITT recommendation I.430 for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in TE (Terminal Equipment), in NT1 or NT2 (Network Termination) or in PABX line-card device.

As specified in I.430, full-duplex transmission at 192kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192kb/s aggregate rate, including 2 'B' channels, each of 64kb/s, and 1 'D' channel at 16kb/s. In addition, the ST5420 provides the 800b/s S & Q multiframe channels for Layer 1 maintenance.

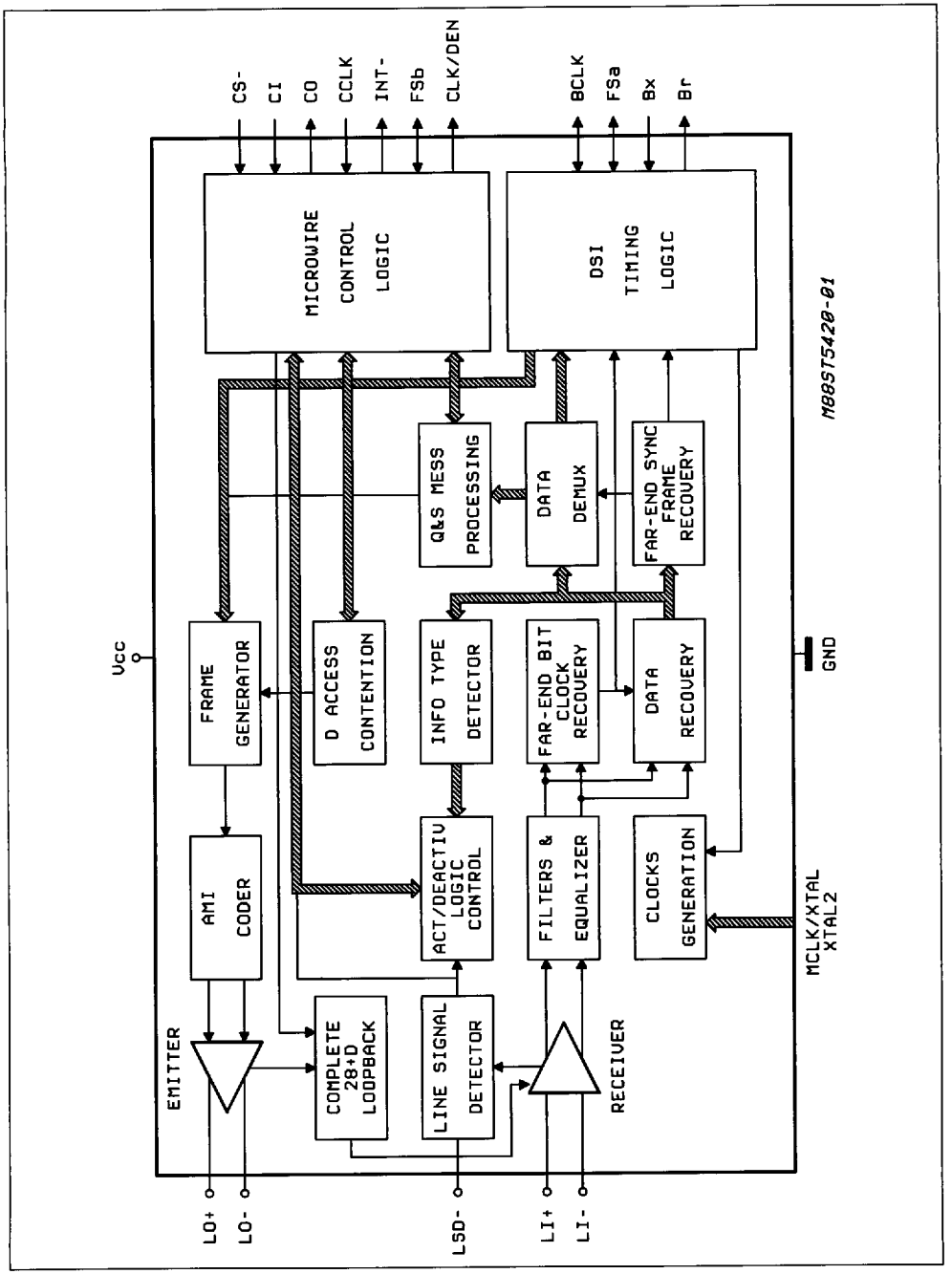
All I.430 wiring configurations are supported by ST5420, including the "passive bus" for up to 8 TE's distributed within 200 meters of low capacitance cable, and point-to-point and point-to-star connections up to at least 1500 meters. Adaptive receive signal processing enables the device to operate with low bit error rates on any of the standard types of cable pairs commonly found in premise wiring installations.

Far-end Clock Resynchronizer and data buffer allow design of NT2 equipment connected to several T interfaces with a minimum external circuitry. Several different Digital Interface formats provide maximum flexibility for 2 B + D basic access data transfer with a minimum pin count. The SID μW programmable functions can be set and controlled via a serial control channel MICROWIRE compatible. The Digital System Interface (DSI) is used for the transfer of "B1", "B2" and "D" channels data.

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Name		Description
LO+, LO-	1, 2	ransmit AMI signal differential outputs to the S line transformer. When used with a 2:1 step-down transformer, the line signal conforms to the output pulse masks in CCITT I.430.
FSa	3	In NT modes and TE mode DSI Slave, this pin is the Transmit Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data into Bx. In TE mode DSI Master only, this pin is a digital output pulse which indicates the start of the 'B' channel data transfer at both Rx and Br.
V_{CC}	4	Positive power supply: must be +5V ±5%
MCLK/XTAL	5	Master Clock or Crystal Oscillator Input: this pin requires either a 15.36MHz crystal (parallel resonant with $R_S < 100\Omega$) to be tied between this pin and XTAL2 or a logic CMOS level 15.36MHz clock from a stable source. When using a crystal, a total of 33pF load capacitance to GND must also be connected. In NT configurations. MCLK clock input doesn't need to be synchronous with the Network Reference Clock (FSa).
XTAL2	6	Crystal Oscillator Output: should be connected to one of the crystal, if used.
Bx	7	Digital input for 'B' and 'D' channel data to be transmitted to the line; must be synchronous with BCLK.
CLK/DEN-	8	**CLK** TE mode DSI slave selected: This pin is a clock signal output phased-locked to the received line signal and can be considred as the far-end clock reference. CLK is a clock signal compatible with the bit clock timing of the DSI format selected: 2.048MHz, 256KHz, 1536KHz or 2.56MHz. **DEN** TE mode DSI master selected: This pin is a normally low output which pulses high to indicate the active bit times for D channel data transmitted at the Bx input. It is intended to be gated with BCLK bit clock to control the shifting of D channel data from a Layer 2 device to the ST5420 transmit buffer. By use of the ST5451 HDLC controller, no external circuitry is needed.
BCLK	9	Bit Clock: set the data shift rate for 'B' and 'D' channel on the digital interface side. When NT mode or TE mode Digital System Intrface (DSI) Slave is selected, BCLK is an input which may be anymultiple of 8KHz from 256KHz to 4.096MHz. It need not be synchronous with MCLK. In TE mode DSI Master this pin an output clock with the frequency depending on the interface format selected. It is synchronous with the data on Bx and Br pins and is phase-locked to the received line signals. Depending on the DSI format choosen BCLK can assume 4 different values: DSI format 1: 2048KHz DSI format 2: 256KHz DSI format 3: 512KHz DSI format 4: 2560KHz
Br	10	Digital output: data is shifted out from the Tri-state Br during the assigned time slots. Elsewhere, Br is high impedance, 2B + D data is shifted out at the BCLK frequency on the transmit rising edges of BCLK except in format 3 wich has a timing GCI compatible. In format 3, data is shifted out at half the BCLK frequency on the transmit rising edges of BCLK.
FSb	11	In NT modes and TE mode DSI Slave, this pin is the Receive Frame Sync. pulse input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data out from Br. In TE mode DSI Master only this pin is an 8 bit wide pulse which indicates the active slot for the B2 channel on the digital interface.
CCLK	12	Clock input for the MICROWIRE control channel.
CI	13	MICROWIRE control channel serial data input.
CO	14	MICROWIRE channel serial data output for status information. When not enabled by CS-, this output is Tri-state.
CS-	15	Chip Select Input: When pulled low enables the control channel data to be shifted in and out. When high, this pin inhibits the control interface.
INT-	16	Interrupt output: A latched output signal, normally Tri-state, that goes low to indicate a change of status of the loop transmission system.

PIN DESCRIPTION (continued)

Name		Description
GND	17	Negative power supply: normally 0V (ground). All analog and digital signals are referred to this pin.
LSD-	18	The line signal detect output, normally Tri-state pulls low when the device is powered down and a received line signal is detected. It is intended to be used to "wake-up" a microprocessor from a low-power idle mode. This output is disabled when the device is powered up.
LI-, LI+	19, 20	Receive AMI signal inputs from the S line transformer: A 1:2 step-up transformer should be used identical to the transmit side. The LI- pin is connected to the intrnal voltage reference at 2.5V and must be decoupled to GND with a 10µF capacitor in parallel with a 0.1µF ceramic capacitor. To ensure the receive input impedance I.430 spec even if power is lost, it is necessary to add 3 external resistors between the transformer and the LI+, LI- pins.

FUNCTIONAL DESCRIPTION

POWER-ON INITIALIZATION

Following the initial application of power, ST5420 enters the power down de-activated state, where all the internal I.430 circuits, including the master oscillator, are inactive and in a low power state except for the line signal detect (LSD-) circuit.

When the SID is powered down and a line signal is detected LSD- pin pulls low.

Configuration mode programming of the SID has to be completed before a power up (PUP) instruction.

POWER UP

An instruction PUP on the MICROWIRE control interface is required to power up the SID.

Power up transition enables all analog and I.430 circuitry, starts the crystal oscillator and reset the state machine to the de-activated state inhibiting the LDS- output as well.

In TE mode DSI master selected, BCLK and FSa clocks are provided according to the format selected.

POWER DOWN

An instruction PDN on the MICROWIRE control interface is required to power down the SID.

PDN forces the device to the low power state without sequencing through any of the de-activation states. It should therefore only be used after the SID has been put in a known state, eg in the line de-activated state.

The power down transition disables analog and "I.430" circuitry, stops the crystal oscillator and all the clocks internally generated.

During power down, Configuration Registers remain in their current state and can be changed by the MICROWIRE control interface.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate Mark Inversion (AMI) coding with inverted binary is used, as illustrated in figure 1.
This coding rule requires that a binary ONE is represented by a 0V high impedance output, whereas a binary ZERO is represented by a positive or negative 100% duty cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c. balanced line signal.

The line frame format used in the SID follows the CCITT recommendation specified in I.430 and illustrated in figure 2. Each complete frame consists of 48 bits, with a line bit rate of 192kbit/s, giving a frame repetition rate of 4kHz. A violation of the AMI coding rule is used to indicate a frame boundary by using a 0+ bit followed by a 0- balance bit to indicate the start of a frame, and by forcing the first binary zero following the balance bit to be of the same polarity.

In Network Termination (NT) to Terminal Equipment (TE) transmission direction, the frame contains in addition to the 2B + D 144kbit/s basic access data, an echo channel, the E bit, which is used to retransmit back the D bits received from the TE (s), and three extra bits : FA, M and S.

In the TE to NT direction, the frame contains in addition to the 2B + D data, of an extra bit : FA.

FA, M and S bits are used to set up a Q multiframe channel in the TE to NT direction, and a S multiframe channel from NT to TE. These 800 bit/s message oriented channels are structured on the base of the United State ANSI standard specification for layer 1 maintenance.

Figure 1 : Inverted AMI Line-coding Rule.

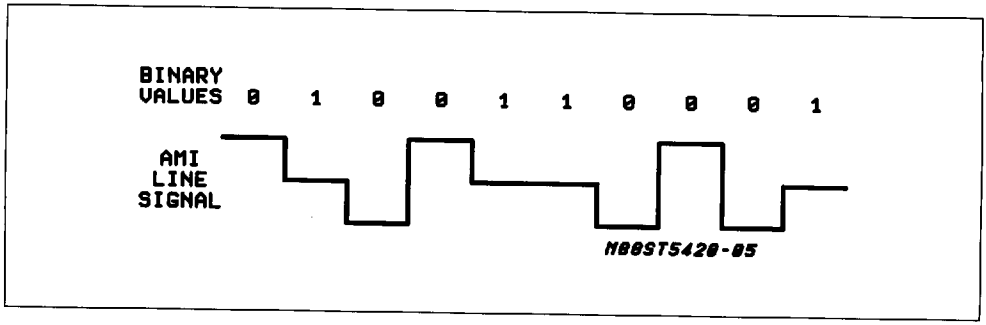
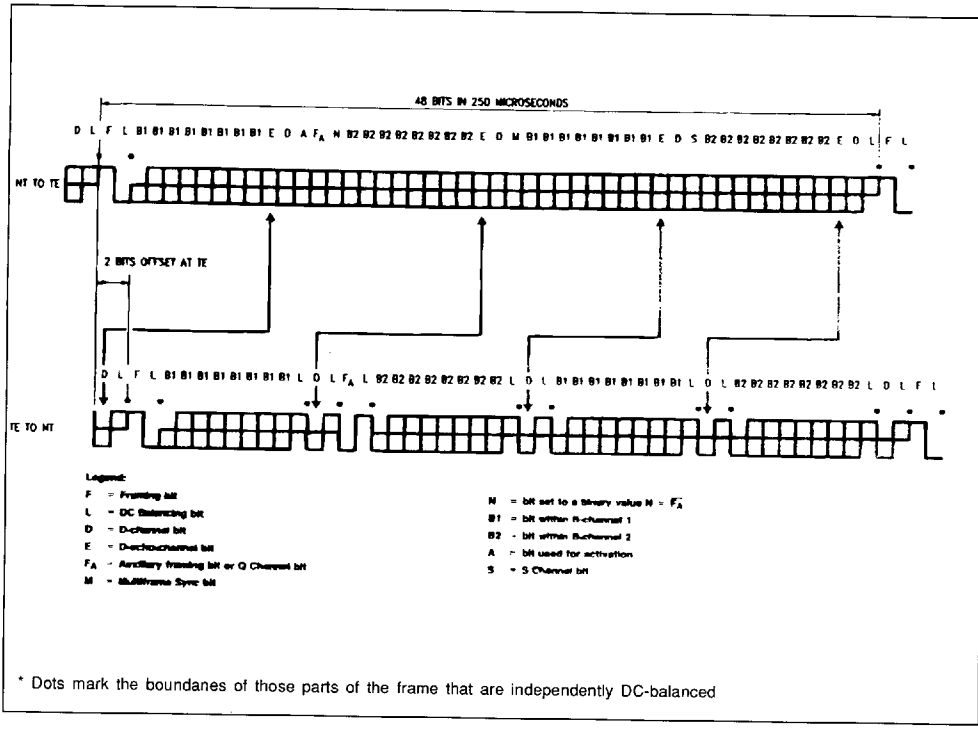


Figure 2 : Frame Format.



* Dots mark the boundanes of those parts of the frame that are independently DC-balanced

LINE TRANSMIT SECTION

The differential line driver outputs LO+ and LO– are designed to drive a transformer with an external termination resistor. A 2: 1 transformer, terminated in a 50Ω load, results in a signal amplitude of 750mV pK on the line and meets the I.430 pulse shape specification.

When driving 400Ω or 5.6Ω load, I.430 requirements are also respected.

When driving a binary 1 symbol, the output presents a high impedance in accordance with I.430.
When driving a O+ or O– symbol, a voltage limited current source is turned on. Short protection is included in the output stage.

Overvoltage protection is required externally.

Depending on TE or NT selected configuration, 192kbit/s data is transmitted on LO+/ LO– by means of clocks respectively locked on the far-end received

bit and frame clocks recovered from the line with two bit delay between transmit and receive frame, or locked with a fixed delay on the Frame Sync signal received from the FSa input.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1 : 2 transformer which may be of the same type used for the transmit direction.

At the front end of the receive section is a continuous filter which limits the noise bandwith. To improve the protection of the line interface and to comply with the receive input impedance spec even if power is lost, it is necessary to add 3 external resistors between the receive transformer and the LI+/LI– pins. Alternatively, a 1 : 1 transformer and 2 external resistors may be used. To correct pulse attenuation and distorsion caused by the transmission line in point to point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics.

This equalizer is always enabled when either TE mode or NT mode adaptive sampling is selected, but is disabled for NT short passive bus applications, when NT mode fixed sampling is selected.

An adaptive threshold circuit maximizes the Signal to Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 15.36MHz.

When the device is powered down, a Line Signal Detect circuit, which can discriminate a valid line signal from noise, is enabled to detect the presence of incoming data if the far-end starts activation of the loop. LSD– output pulls low to wake up the equipment.

DIGITAL INTERFACES

The SID provides two digital interface for both control and basic access data transfer named MICROWIRE and DSI.

Digital System Interface (DSI): The Digital System Interface (DSI) combines B and D channel data onto common pins Bx and Br. Several multiplexed formats are available as shown figure 3. Selection is made via MICROWIRE. Direct connection among different ISDN devices can be provided.

At this interface, phase skew between Transmit and Receive directions may be accomodated at the Line Card or NT2 end since separate Frame Sync inputs FSa and FSb are provided. Each of these synchronizes a counter which gates the transfer of B1, B2 and D channels in the allocated Time-slots.

In NT2 or PBX equipments, the serial shift rate is determined by the BCLK input and may be any value from 256kHz to 4096kHz. Thus, the B and D channel slots can be interfaced to a TDM bus and assigned to the first 4 bytes wide Time Slots of the frame. Unused channels are high impedance.

In TE mode DSI master selected, FSa is an output indicating the start of both Transmit and Receive B and D channel data transfers. BCLK is also an output at the frequency of which is dependent on the Format selected :

in Format 1, BCLK = 2048KHz
in Format 2, BCLK = 256kHz
in Format 3, BCLK = 512kHz
in Format 4, BCLK = 2560KHz

Format 3 is GCI compatible excluding C/I and M channel transfer.

Except for Format 3, data is transmitted in both direction at the BCLK frequency. Data is shifted out from Br on the rising edges of BCLK and is shifted in on Bx on the falling edges of BCLK.

Control Interface (MICROWIRE) : A serial interface, which can be clocked independently from DSI, is provided for microprocessor control of various functions in the SID. All data transfers consist of a single byte shifted into the Control Register via the CI pin simultaneous with a single byte shifted out from the Status Register via the CO pin. Data shifts into CI on rising edges of CCLK and out from CO on falling edges when CS– is pulled low for 8 cycles of CCLK.

An interrupt output, INT– goes low to alert the microprocessor whenever a change occurs in one or more of the conditions indicated in the Status Register. This latched output is cleared to a high impedance state by the first rising CCLK edge after CS– goes low.

Tables 1 and 2 list the control functions and status indicators.

Status read. Whenever a change occurs in one or more of the conditions indicated in the SID Status Register, the INT– pin is pulled low. The "controller" device must service the interrupt before attempting to send a new command to the SID device. On the first rising edge of the CCLK after CS– goes low, the INT– pin from SID is cleared to the high impedance state.

The status bits are output on the CO pin. If the in-

terrupts for EOM status and MER status have been disabled then, these status are assumed not necessary and cannot be accessed.

Command write. If the "controller" needs to send a command to SID, it pulls CS– pin of SID low and transmits 8 bits of command on the 8 rising edges of CCLK. While the command bits are being transmitted, a SID status change could occur, but the resulting interrupt (if selected) will be inhibited until the CS– is cleared to the high state. The INT– will then go low, forcing an interrupt. The controller then forces a low level on the CS– input to access the status as described above.

When a command is being received on the CI pin, the CO pin outputs a "00000000" byte indicating a NOC "no change" status. It is possible to write in the SID on the CI pin while shifting out the status register onto CO.

Table 1 : Microwire Control Register Functions.

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Activatiotion/deactivation									
*Power Down	PDN	0	0	0	0	0	0	0	0
Power Up	PUP	0	0	1	0	0	0	0	0
Deactivation Request	DR	0	0	0	0	0	0	0	1
Info2 Transmit Request	FI2	0	0	0	0	0	0	0	1
Activation Request	AR	0	0	0	0	0	0	1	1
Device Mode:									
*NT Mode Adaptive Sampling	NTA	0	0	0	0	0	1	0	0
NT Mode Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Mode DSI slave	TES	0	0	0	0	0	1	1	0
TE Mode DSI Master	TEM	0	0	0	0	0	1	1	1
Monitoring Mode Activation	MMA	0	0	0	1	1	1	1	1
Digital Interface Format:									
* DSI Format 1	DIF1	0	0	0	0	1	0	0	0
DSI Format 2	DIF2	0	0	0	0	1	0	0	1
DSI Format 3	DIF3	0	0	0	0	1	0	1	0
DSI Format 4	DIF4	0	0	0	0	1	0	1	1
B channel Configuration:									
*B Channel Mapped Direct	BDIR	0	0	0	0	1	1	0	0
B Channel Exchanged	BEX	0	0	0	0	1	1	0	1
B1 Channel Enabled	B1E	0	0	0	1	0	1	0	0
*B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enabled	B2E	0	0	0	1	0	1	1	0
*B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
D Channel Access:									
D Channel Request Class 1	DREQ1	0	0	0	0	1	1	1	0
D Channel Request Class 2	DREQ2	0	0	0	0	1	1	1	1

(*) indicates initial state following power on initialization.

Table 1 : Microwire Control Register Functions (continued).

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
End of Message Indication:									
*EOM Indication Enabled	EIE	0	0	0	1	0	0	0	0
EOM Indication Disabled	EID	0	0	0	1	0	0	0	1
Multiframe Processing:									
*Multiframe Disabled	MID	0	0	0	1	0	0	1	1
Multiframe Enabled	MIE	0	0	0	1	0	0	1	0
Write Multiframe Message	MFT	0	0	1	1	M1	M2	M3	M4
*Enable 3X Checking	EN3X	0	0	1	0	1	0	0	0
Disable 3X Checking	DIS3X	0	0	1	0	1	0	0	1
Loopback Test Mode:									
*Clear All Loopbacks	CAI	0	0	0	1	1	0	1	1
Loopback B1 on DSI Enabled	LB1E	0	0	0	1	1	0	0	0
Loopback B2 on DSI Enabled	LB2E	0	0	0	1	1	0	0	1
Loopback 2 B + D Enabled	LSB	0	0	0	1	1	0	1	0
Loopback B1 on Line Enabled	LBB1E	0	0	0	1	1	1	0	0
Loopback B2 on Line Enabled	LBB2E	0	0	0	1	1	1	0	1

(*) indicates initial state following power on initialization.

Table 2 : Microwire Status Register Functions.

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
No Change	NOC	0	0	0	0	0	0	0	0
Line Signal Detected	LSD	0	0	0	0	0	0	1	0
Activation Pending	AP	0	0	0	0	0	0	1	1
End of Message on D Channel	EOM	0	0	0	0	0	1	1	0
Lost Contention	CON	0	0	0	0	0	1	1	1
Multiframe Receive Register	MFR	0	0	1	1	M1	M2	M3	M4
Activation Indication	AI	0	0	0	0	1	1	0	0
Line Error Indication	EI	0	0	0	0	1	1	1	0
Deactivation Indication	DI	0	0	0	0	1	1	1	1

Figure 3a : DSI Formats Master.

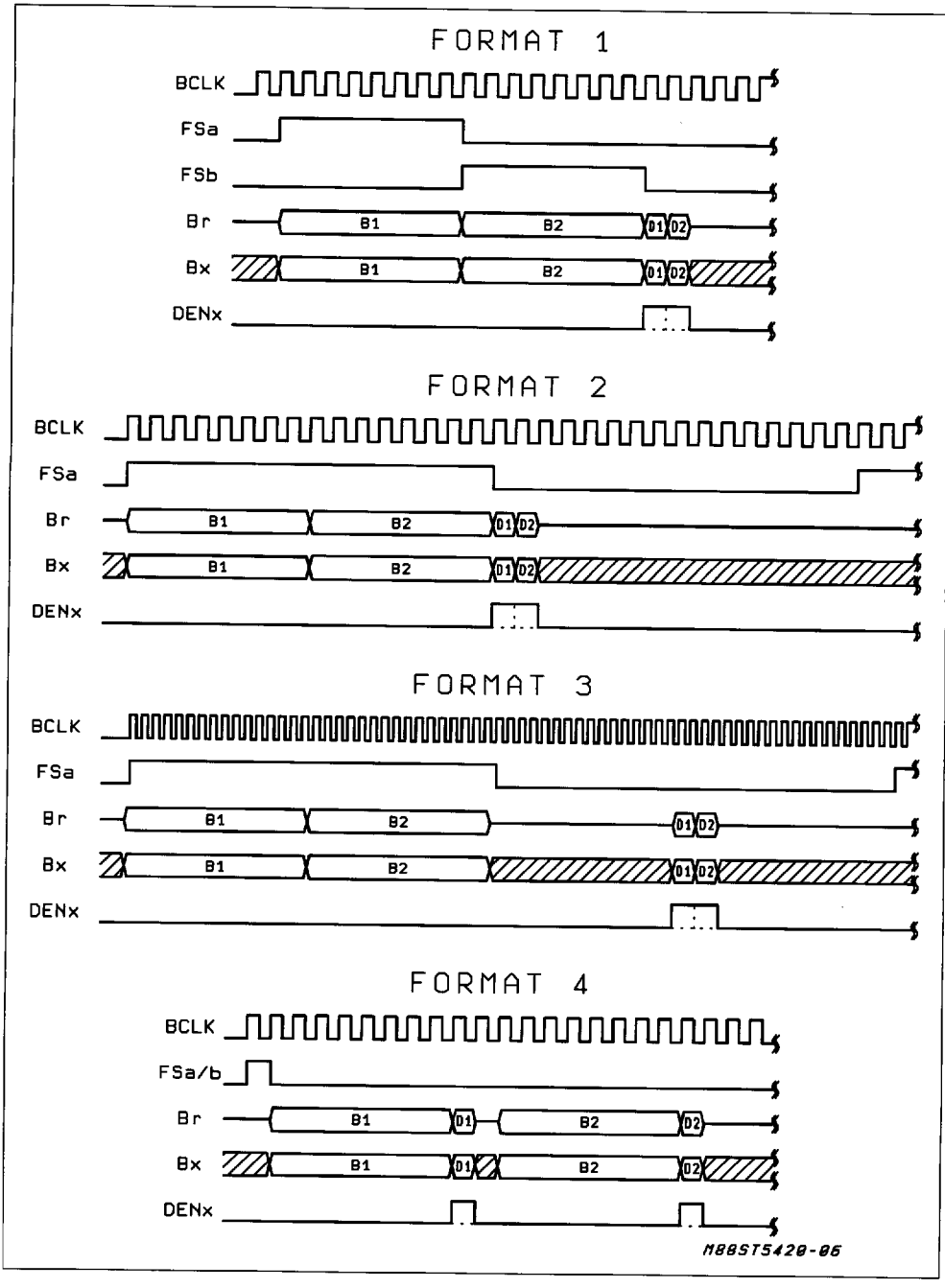
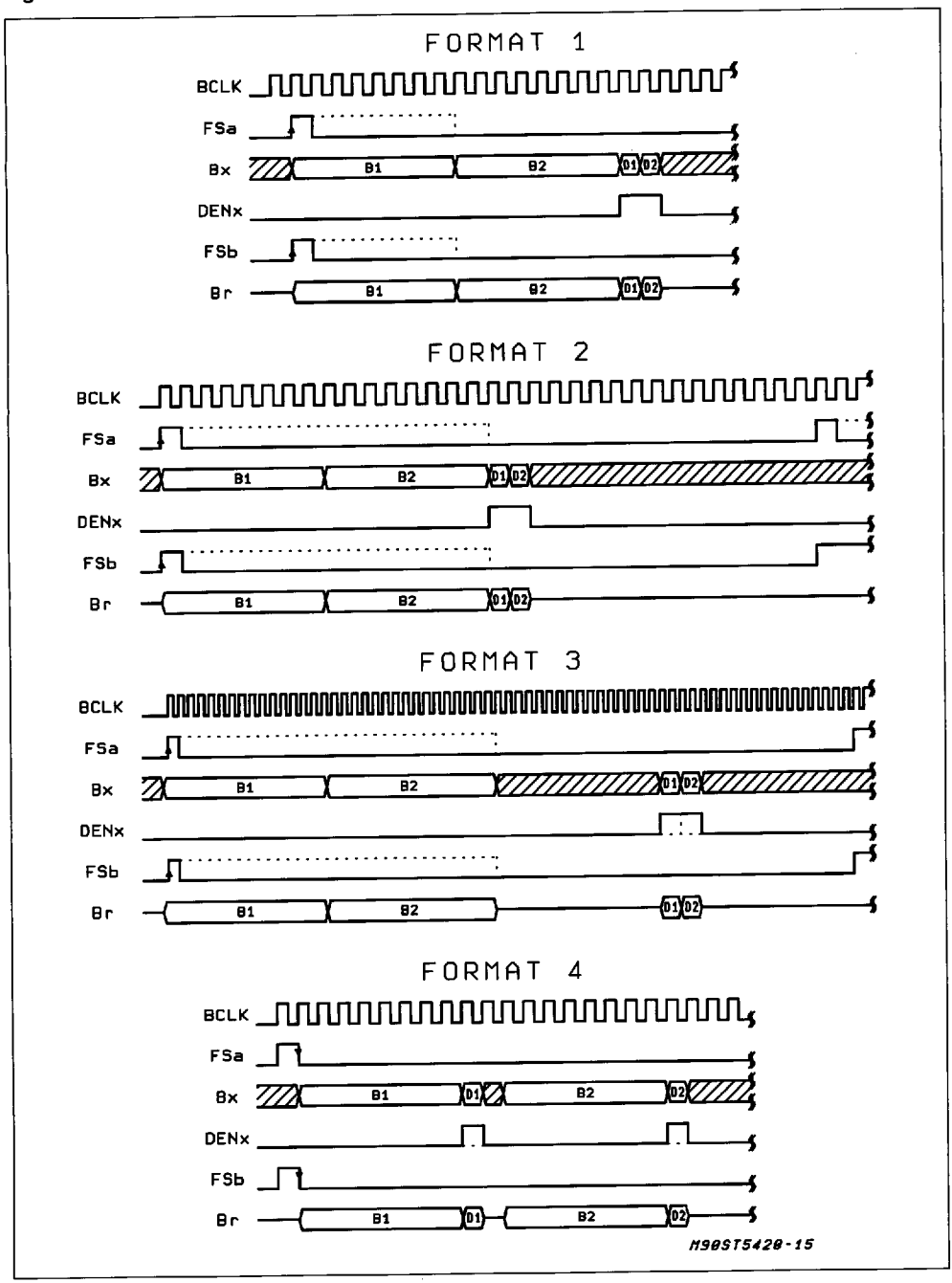


Figure 3b : DSI Formats Slave.



CONTROL FUNCTIONS DESCRIPTION

ACTIVATION/DEACTIVATION

PUP : Power Up. The Power Up command enables all analog circuitry, starts the XTAL and resets the state machine to the deactivated state enabling INFO0 transmission. It also inhibits the LSD–output.

PDN : Power Down. The Power Down command immediately forces the device to a low power state, without sequencing through any of the deactivation states. It should therefore only be used after SID has been put in a known state.

DR : Deactivation Request. The Deactivation Request command forces the device through the appropriate deactivation sequence specified in I.430. In TE mode, is equivalent to a Timer Expiry instruction.

AR : Activation Request. The Activation Request initiates the specified Activation sequence. It is recommended that an AR be delayed at least 2ms after the device is powered up.

FI2 : Force Info2. Being in the activated state G3, the RSY instruction forces the SID through the appropriate sequence to send INFO2 on the line. If the S line is not completely activated, RSY instruction has no effect. Should be used in NT mode only in NT1 equipment. On loss of signal received from the line, the SID sends INFO2 on the line.

Command. An activation being in progress, a second AR command allows the SID through the appropriate sequence to send INFO4 on the line. Should be used in NT mode only in NT1 equipment. In that revision only.

DEVICE MODE

NTA : NT Mode Adaptive Sampling. In NT mode, Adaptive sampling should be selected when the device is an NT equipment connected on any wiring configuration up to the maximum specified length for operation. Multiple Terminals, if required, must be grouped within approximately 50 meters of each other (depending on cable capacitance as indicated in I.430). Transmit section of the SID is phased locked to the DSI FSa signal.

NTF : NT Mode Fixed Sampling. In NT mode, Fixed sampling should be selected when the device is in an NT equipment connected on a passive bus wiring configuration up to approximately 200 meters in length depending on cable type. In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed, to enable multiple Terminals (nominally up to 8) to be connected anywhere along the passive bus. Transmit and Receive section of the SID is phased locked to the DSI FSa signal.

TES : TE Mode DSI slave. This mode should be selected when the device is used on the T side of an NT2 equipment. The I.430 circuitry operates as in the TE mode but the DSI interface is then driven by BCLK and FSa sources in the NT2.
Data buffers and a clock resynchronizer enable the Digital Interface to function with jittering sources for FSa and BCLK.
A clock signal output phased locked to the Receive line signal is delivered on CLK in a mode depending on the reference clock generation configuration selected.
All D channel access control circuitry is disabled.

TEM : TE Mode DSI Master. This mode should be selected when the device is in a Terminal. The SID is then the source of the BCLK and FSa signals. Access to the Transmit D channel, including the priority and contention resolution control, is enabled.

MMA : Monitoring Mode Activation. The SID being selected previously in the TEM mode, the MMA command allows the device to receive and activate on INFO3 frames, while being the master of the Digital System Interface. That mode can be used for applications such as outputs monitoring of TEs on a Passive Bus via a "dummy" NT.
The MMA mode can be disabled by any configuration command : ie TEM.

B CHANNELS CONFIGURATION

BDIR/BEX/B1E/B1D/B2E/B2D. BDIR and BEX instructions provide for the exchange of data between the B1 and B2 channels.

When either or both B channels are disabled by means of the B1D or B2D instruction, binary 1 are transmitted on the line in those B channel bit positions regardless of data at the Bx input, meanwhile being Br output in high impedance state. When enabled by means of the B1E and B2E instructions, B channels are transparently transmitted.

D CHANNEL ACCESS

DREQ1/DREQ2. The instructions DREQ1 and DREQ2 are a request from the layer 2 to the SID selected in TE mode to attempt to access the transmit D channel at the S interface. The correct priority class for the pending message must also be selected : 8 or 9 selected with DREQ1 and 10 or 11 selected with DREQ2.

END OF MESSAGE INDICATION

EIE/EID. In TE configuration, the End of Message Status indicator sending can be enabled by means of the instruction EIE and disabled by means of the instruction EID.

MULTIFRAME PROCESSING

MID/MIE/MFT/MFR. The multiframe channel processing must be enabled by an MIE instruction and an MID instruction must be used to disable. In the Transmit direction, with the device in TEM or TES mode, data entered in bit positions M1, M2, M3 and M4 of instruction MFT is transmitted towards the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT mode, data entered in the M bit positions is transmitted towards the TE in multiframe bit positions S1, S2, S3 and S4 respectively.

In the Receive direction, when the Multiframe receive data buffer requires servicing, the MFR status message is autonomously sent from the SID in which M1, M2, M3 and M4 bits represent the Q1, Q2, Q3 and Q4 or S1, S2, S3 and S4 bits received from the multiframe respectively.

Multiframe Structure and transmission protocol on the line comply with the ANSI US Standard T1.XYZ.198Y. "Basic Access Interface for S and T Reference points - Layer 1 specification".

Multiframe message exchange can be supported by the SID when the line is synchronized : states F6 & F7 in TEM or TES modes and state G3 in NT mode.

DIS3X/EN3X. When EN3X is set, a new Multiframe message received from the line is checked and transferred on the M channel when received three times identical. When DIS3X is set, Multiframe messages are transferred transparently every superframe.

LOOPBACK TEST MODES

LBS/LB1E/LBB1E/LB2E/LBB2E/CAL. Three classes of loopback mode are available on the SID selected by the appropriate Control Instruction. LBS set a the loopback of the 2B + D channels from the Bx input to the Br output. It may be set when the device is either activated, in which case it is transparent or when it is deactivated in which case it is non-transparent.

LB1E and LB2E instructions turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.

LBB1E and LBB2E instructions turn each individual B channel from the Digital Interface received input back to the Digital Interface transmit output. They may be set separately or together.

CAL instruction clears all the loopbacks simultaneously.

STATUS INDICATORS DESCRIPTION

NOC : No Change. The status indicator NOC is transmitted from CO output during a Control Access on MICROWIRE interface when no change has occured.

LSD : Line Signal Detection. If set, indicates that the far-end of the line is attempting to activated the interface. May be used as an alternative to the LSD– pin to wake up a microprocessor.

AP : Activation Pending. If set in NT mode, indicates that INFO1 frames have been identified on the line. The SID is waiting for an Activation Request instruction to send INFO2.

If set in TEM or TES mode, indicates that INFO2 (or INFO4) frames have been identified on the line when the following events occur :

- being in the TE deactivated state, detection of INFO2 or INFO4
- being in the TE loss framing state F8, detection of INFO2

EOM : End Of Message. In TE configuration, set when the closing flag of a D channel message has been transmitted by a TE on the S interface indicating successful completion of a packet. The Interrupt associated with this indicator can be disabled via the Control Instruction EID if desired.

CON : Lost Contention. Set when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit indicating a lost contention. D channel access attempt is deactivated at the S interface. A new DREQ1 or DREQ2 instruction is needed to restart the procedure.

AI : Activate Indication. If set, indicates that the S interface has received INFO3 or INFO4.

EI : Error Indication. If set in the TE mode, indicates

If set in the NT mode, indicates that a loss of frame synchronization is detected on the line.

DI : Deactivate Indication. If set, indicates that the S interface has been deactivated.

ACTIVATION/DEACTIVATION

NT Mode. After power on initialization, the SID can be configured in NT power down mode, depending on register configuration setting. The SID is powered up by means of the PUP instruction.

Activation may be initiated from either end of the loop. To operate an activation from the Network, the device must be first powered up by the appropriate instruction followed at least 2ms later by an AR instruction. Network timing : FSa, BCLK and MCLK if provided must be present at this time.

When the activation is initiated by the far-end, the SID being in the Power Down state, a Line Signal Detector pulls low the LSD– and INT– pins, either of which can be used to wake up the system. A Power Up procedure must then be issued allowing identification of received signal ie INFO1. The appropriate procedure is then followed according to I.430. The detailed description is given in figure 4.

I.430 recommends that 2 Timers should be available in an NT. An Activation Request to the SID should be associated with the start of an external Timer 1 if required. Timer 1 should be stopped when the AI indication is generated following successful activation. If Timer 1 expires before AI is generated, however, Control instruction DR should be written to the device to force de-activation. Timer 2 which is specified to prevent unintentional re-activation, is not required since the SID can uniquely recognize INFO1 frames.

TEM or TES Mode. After Power on initialization, the SID can be configurated in TEM or TES side power down mode, depending on register configuration setting. The SID is powered up by means of the PUP instruction.
Activation may be initiated from either end of the loop. To operate an activation from the Terminal, the device must be first powered up by the appropriate instruction followed at least 2 ms later by an AR instruction. When the activation is initiated by the far-end, the SID being in the Power Down state, a Line Signal Detector pulls low the LSD– and INT– pins, either of which can be used to wake up the system. A Power Up instruction must then be issued allowing identification of received signal ; INFO2. The appropriate procedure is then followed according to I.430. The detailed description is given in figure 5.

I.430 recommends that a Timer should be available in an TE. An Activation Request to the SID should be associated with the start of an external Timer 1 if required. Timer 1 should be stopped when the AI indication is generated following successful activation. If Timer 1 expires before AI is generated, however, Control instruction DR should be written to the device to force deactivation.

Figure 4 : Activation Procedure NT Selected.

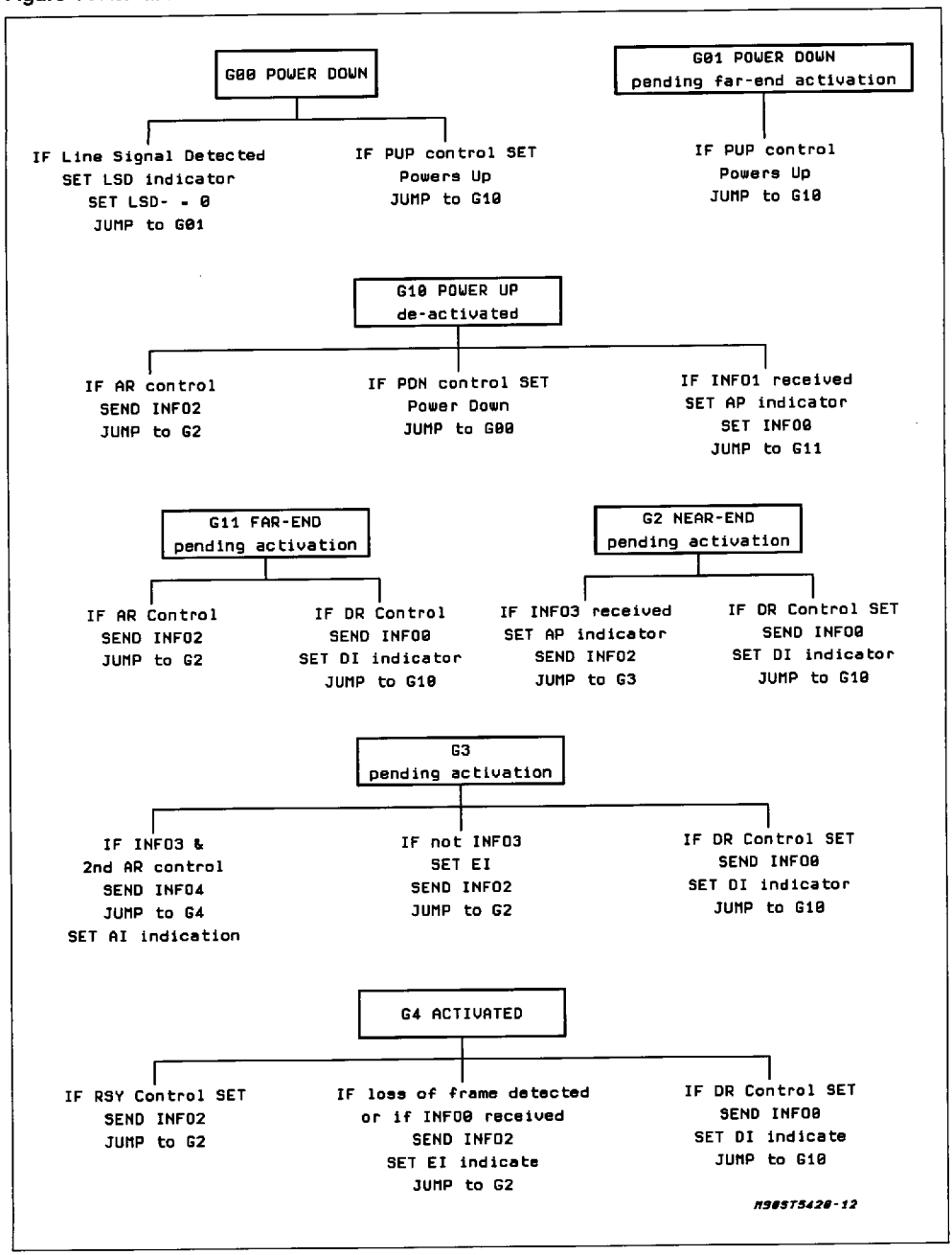


Figure 5 : Activation Procedure TE Selected.

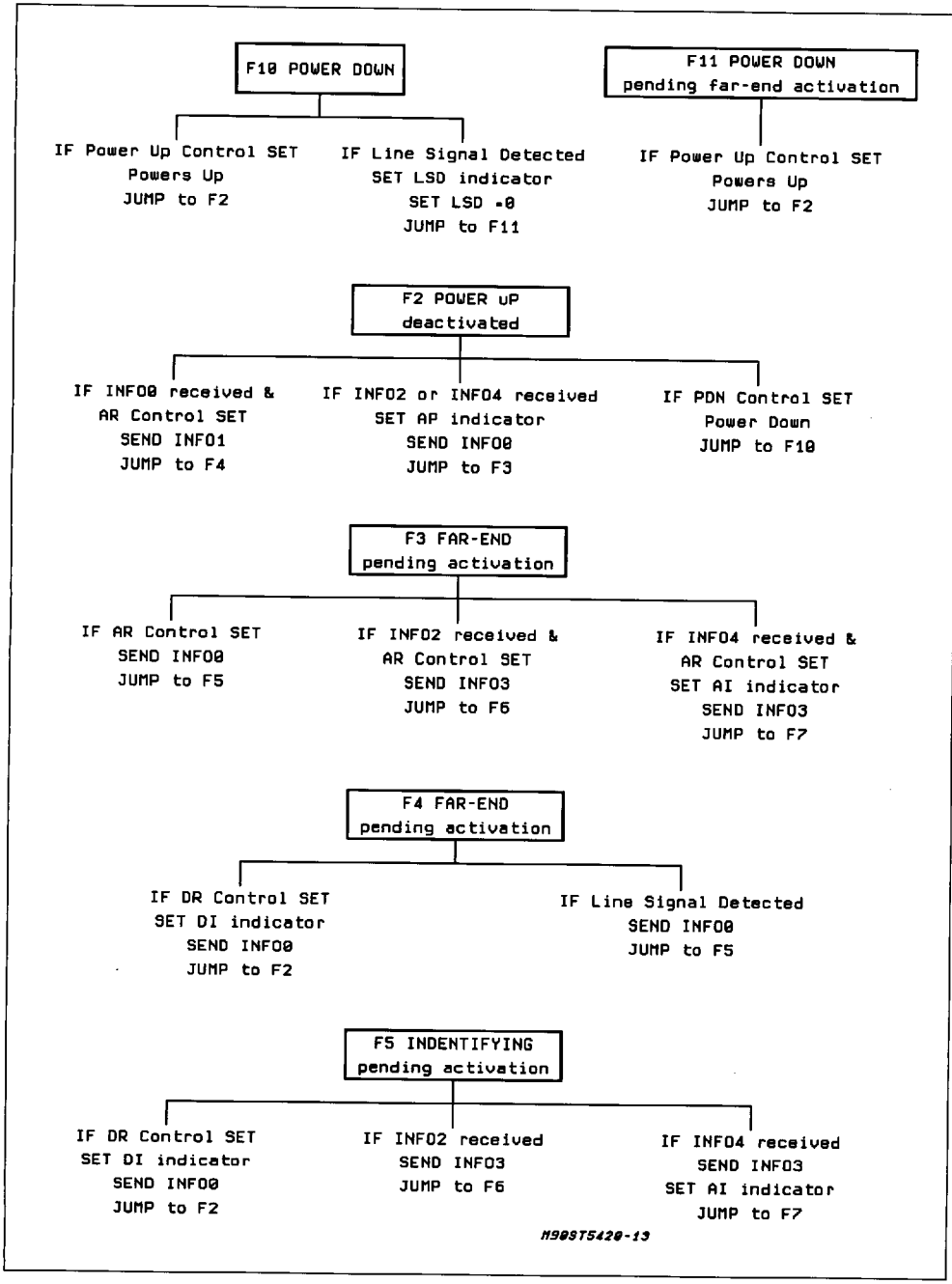
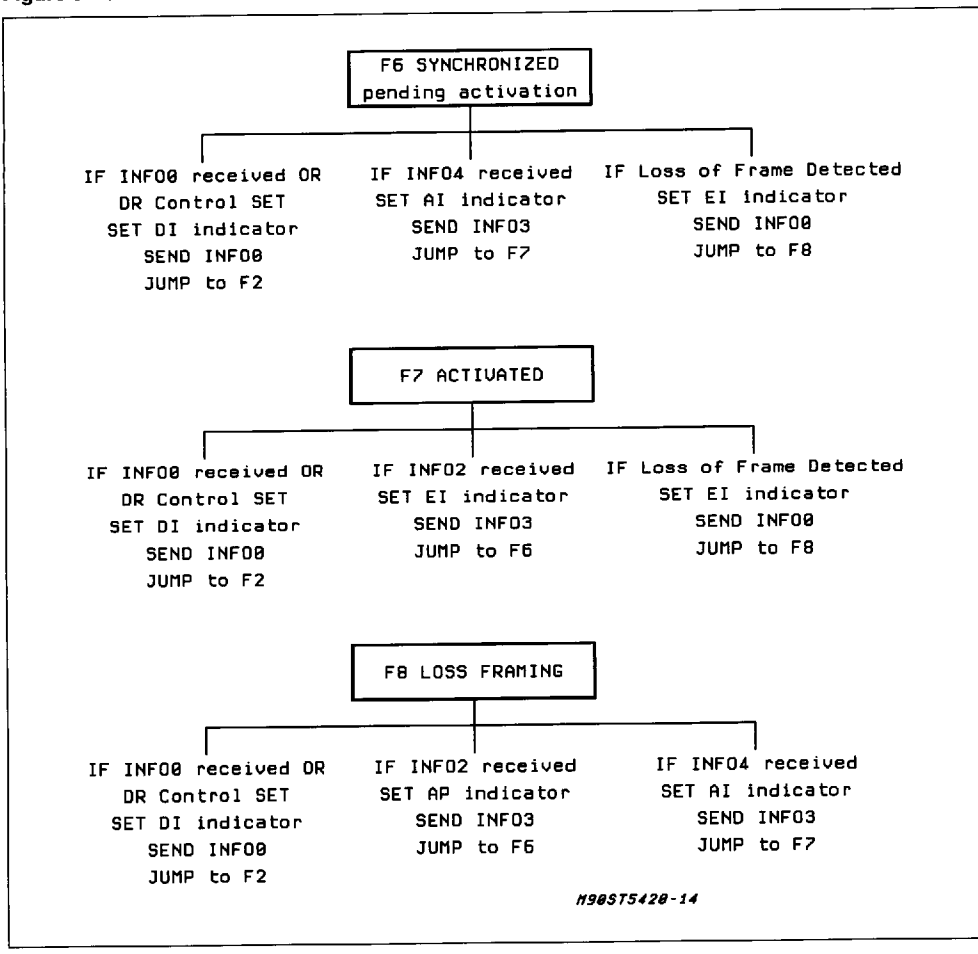


Figure 5 : Cont'd Activation Procedure TE Selected.



D Channel Access in TEM Mode. In TEM mode, the SID arbitrates access for Layer 2 HDLC frames to the D channel bit positions on the line in accordance with the I.430 Priority Mechanism for Signalling and Packet Priority Classes. The shifting of D channel Transmit data from the Controller into the SID buffer is controlled by DEN output which can be gated with the Digital Interface Bit Clock BCLK.

After Power initialization, DEN output pulses are inhibited and no D channel data is shifted into the Bx input.

A Controller device requiring to start transmission of a packet on the line should first activate the line by the appropriate procedure. Then it should prime its Transmit Buffer such that the opening Flag is ready to be shifted accross the Digital interface. Then a Control Instruction DREQ1 or DREQ2 will initiate the D channel access sequence according to Priority Class 1 (signalling) or Priority Class 2 (Data packet) respectively.

In response to the DREQ instruction, the DEN output is immediately enabled to prefetch the opening Flag from the Controller device into the SID D channel Buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S interface is transmitting in the D channel. This is assumed by counting consecutive "1"s in the E bit position of frames received from the NT and comparing the

value with the current priority level as specified by I.430. If another TE is active in the D channel, DEN pulses are inhibited once the Opening Flag is in the Transmit Buffer, to prevent further fetching of Transmit data from the Controller until D channel access is achieved.

As soon as the required number of consecutive E bit "1" has been counted, the leading 0 of the opening flag is transmitted in the next D bit position towards the NT. Then, DEN pulses are also re-enabled in order to shift D channel bits from the Controller into the SID Transmitter buffer. No interrupts are necessary for local flow control between the Controller and the SID.

During transmission in the D channel, the SID continues to compare each E bit received from the NT with the D channel bit previously transmitted before proceeding to send the next D bit. In the event of a mis-match, a contention for the previous D bit is assumed to have been won by another TE. Transmission of the current packet therefore stops and "1"s are transmitted in all following D bit positions. Status indication type CON is set and the INT– output is pulled low to interrupt the Controller. DEN output pulses are again inhibited.

In order to retransmit the lost frame, the Controller must begin as before by priming again its Transmit Buffer with the packet header and writing a new DREQ instruction into the Control Register.

Successful completion of a Transmit frame is detected by the SID when the closing Flag is transmitted in the D channel. "1"s are then transmitted in the following D bit positions, with the DEN output held low to prevent further transfer of Data from the Controller. If enabled by the Control Instruction EIE, the INT output is pulled low with status indicator EOM set to indicate the End of message.

In order to transmit a new frame, the Controller must begin as before.

POWER SUPPLIES

While the pins of the ST5420 SID device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.1µF should be connected from this common point to V_{CC} as close as possible to the device pins.

Figure 6 : Voice Terminal Application Diagram.

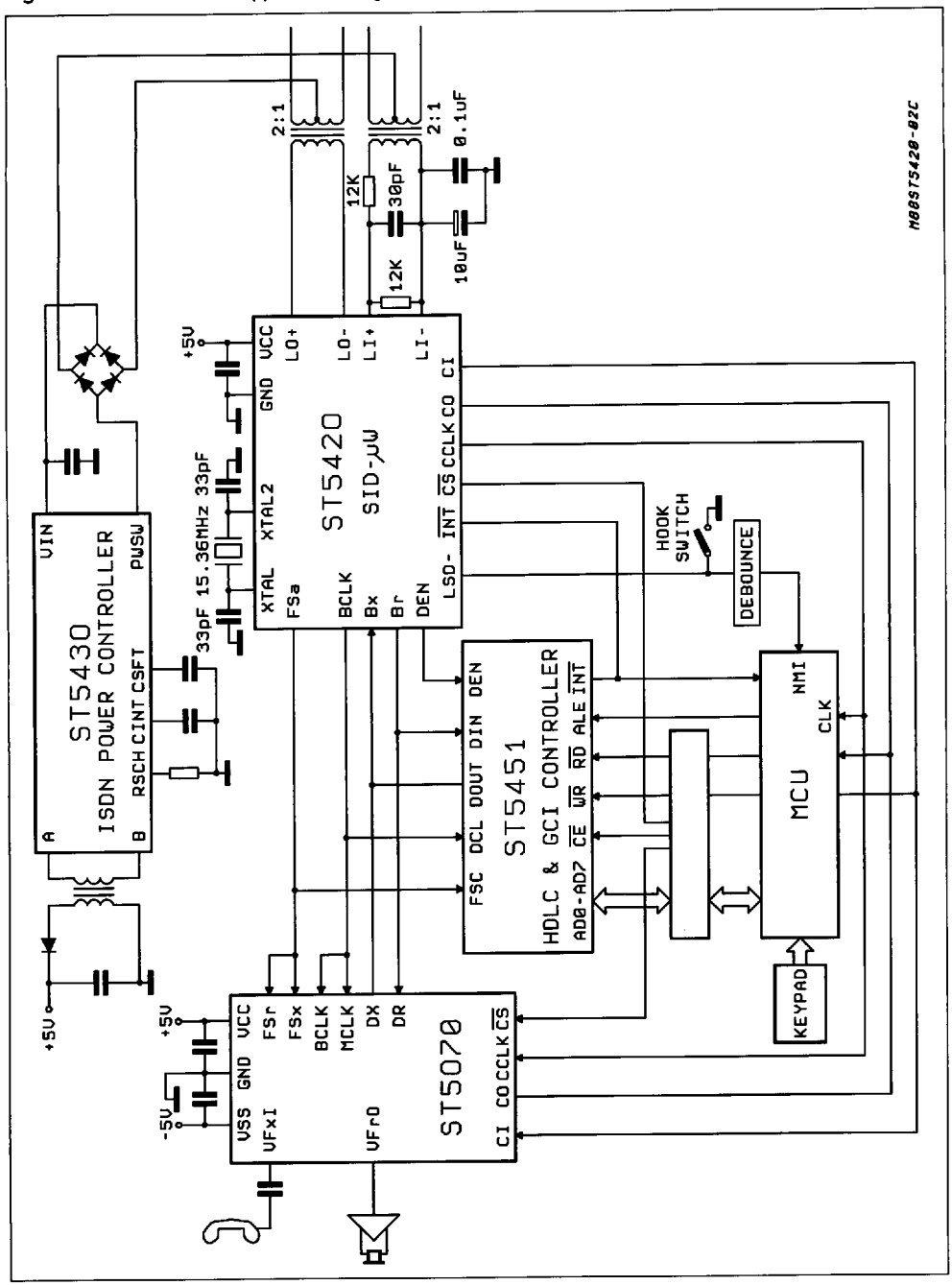
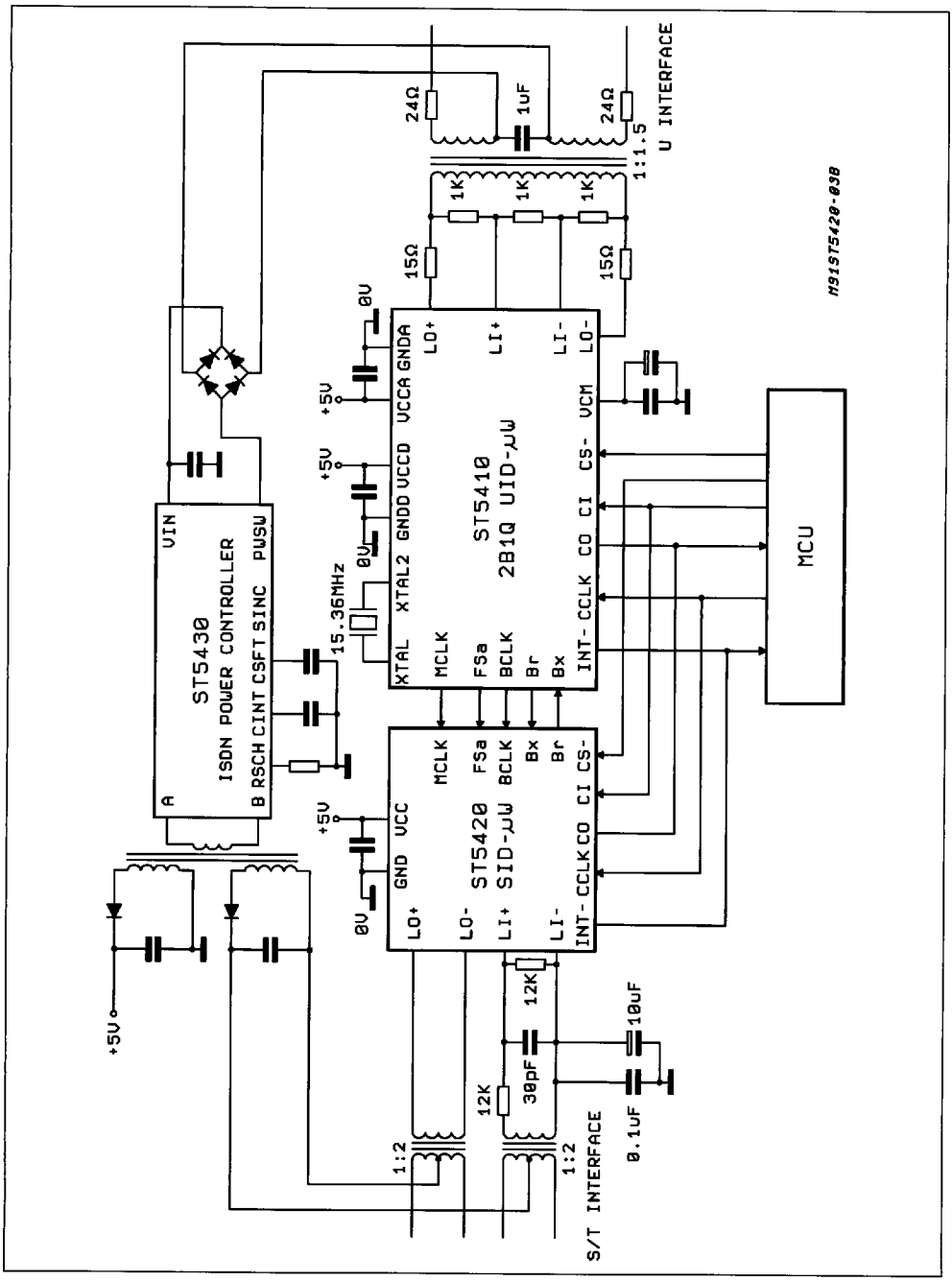


Figure 7 : Network Terminal Application Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
	V_{CC} to GND	7	V
	Voltage at LO, LI	V_{CC} + 1V to GND - 1V	
	Current at LO	±100	mA
	Voltage at any Digital input	V_{CC} + 1V to GND - 1VmA	
	Current at any Digital output	±50	mA
	Storage Temperature Range	-65 to +150	°C
	Lead temperature (soldering, 10 second)	300	°C

ELECTRICAL CHARACTERISTICS (unless specified otherwise : V_{CC} = 5V ± 5%, T_A = 0°C to 70°C ; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C ; all signals are referenced to GND).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2			V
V_{OL}	Output Low Voltage	Br IL =-3.2mA All Other Digital Outputs, IL = 1mA			0.4	V
V_{OH}	Output High Voltage	Br IL = -3.2mA All Other Digital Outputs, IL = +1mA	2.4			V
I_{IL}	Input Low Current	Any Digital Input, GND < V_{IN} < V_{IL}	-10		10	µA
I_{IH}	Input High Current	Any Digital Input, V_{IH} < V_{IN} < V_{CC}	-10		10	µA
I_{OZ}	Output Current in High Impedance (tri-state)	All Digital Tri-state I/Os	-10		10	µA
LINE INTERFACE						
I_{LI}	Input Leakage	0V > LI+, LI- > 5V	-1		1	µA
R_{LI}	Input Resistance	0V > LI+, LI- > 5V	20			KΩ
V_{LI}	Input Voltage Range		-0.5		V_{CC} +0.5	V
R_{LLO}	Load Resistance	from LO+ to LO-		200		Ω
C_{LLO}	Load Capacitance	from LO+ to LO-			200	pF
V_{OS}	Differential Offset Voltage at LO+, LO-		-20		20	mV
POWER DISSIPATION						
I_{CC0}	Power Down Current	All Outputs Open-Circuit			600	µA
I_{CC1}	Power Up Current	(Note 1)			15	mA

Note 1: when the device is activated and driving a correct terminated line, ICC1 increases by several mA. A worst case data pattarn, consisting of all binary O'S increases ICC1 by approximately 8mA.

ELECTRICAL CHARACTERISTICS (continued)
TRANSMISSION PERFORMANCE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Transmit Pulse Amplitude	Conform to all CCITT I430 Requirements Using the Specified Transformer	±1.55		±1.75	
	Input Pulse Amplitude	Differential Between LI+ & LI–	±175			mVpk

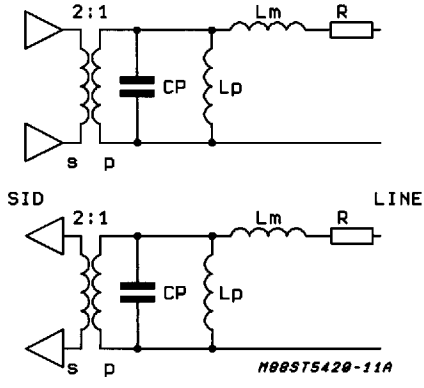
MASTERCLOCK

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	MCLK Frequency			15.36		MHz
	MCLK Input Clock Jitter				50	ns
	Timing Recovery Jitter	BCLK Output Relative to MCLK at NT	– 130		+ 130	ns
t_{MH}, t_{ML}		Clock Pulse Width High and Low of MCLK	20			ns
t_{MR}, t_{MF}		Rise Time and Fall Time of MCLK Used as an Input			10	ns

TRANSFORMER MODEL (all values are to be measured at 10khz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
1 : N	Primary to secondary turn ratio	– 1	2	1	%
R	Primary Total DC Resistance			10	Ohm
Lp	Primary Inductance	20			mH
Lm	Primary Inductance with Secondary Shorted			20	µH
Cp	Primary Capacitance with Secondary Open			25	pF

Figure 8 : Transmit & Receive Transformer Model.



TIMING SPECIFICATIONS (unless specified otherwise : V_{CC} = 5V ± 5%, T_A = 0°C to 70°C ; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C ; all signals are referenced to GND ; see note 5 for timing definition).

SERIAL CONTROL PORT TIMING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK				2.048	MHz
t_{CH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	100			ns
t_{CL}	Period of CCLK Low	Measured from V_{IL} to V_{IL}	100			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCSL}	Hold Time, CCLK High to CS Transition		10			ns
t_{SSC}	Setup Time, CS–Transition to CCLK High		50			ns
t_{SIC}	Setup Time, CI Valid to CCLK High		50			ns
t_{HCI}	Hold Time, CCLK High to CI Invalid		20			ns
t_{DCO}	Delay Time, CCLK Low to CO Data Valid	Load = 100pF. Plus 1 LSTTL Load			20	ns
t_{DSO}	Dealy Time, CS–Low to CO Data Valid	Bit C7 only			50	ns
t_{DCZ}	Delay Time, CCLK Low to CO High				50	ns
t_{HCSH}	Hold Time, 8th CCLK Low to CS High		100			ns
t_{DCI}	Delay Time, CCLK High to INT- High					ns

TIMING SPECIFICATIONS (continued)

DIGITAL INTERFACE TIMING : FORMAT 4

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Transition to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH} t_{WCL}	BCLK Width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		30			ns
t_{DCF}	Delay Time BCLK High to FSa High	TE Mode only			30	ns
t_{DCD}	Delay Time BCLK High to Data Valid		20		80	ns
t_{DZC}	Delay Time BCLK Low to Data Invalid		20		80	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		20			ns
t_{HCD}	Hold Time BCLK Low to Data Invalid		20			ns

Note : 5. A signal is Valid if it is above V_{IH} or below V_{IL} and Invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply :
a) All input signals are defined as : V_{IL} = 0.4V, V_{IH} = 2.7V, t_a < 10ns, t_a < 10ns.
b) Delay times are measured from the Input signal Valid to the output signal Valid.
c) Setup times are measured from the Data input Valid to the clock input Invalid.
d) Hold times are measured from the clock signal Valid to the Data Input Invalid.

TIMING SPECIFICATIONS (continued)

DIGITAL INTERFACE TIMING : FORMAT 1, 2

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Transition to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH} t_{WCL}	BCLK Width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		30			ns
t_{DCF}	Delay Time BCLK Transition to FSa Transition	TE Mode only			30	ns
t_{DCD}	Dealy Time BCLK High to Data Valid		20		80	ns
t_{DFD}	Dealy Time FSa High to Data Valid	Load 100pF. Apply only if FSa Rises Later Than BCLK Rising Edge.			80	ns
t_{DCZ}	Delay Time BCLK Low to Data Invalid		20		80	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		20			ns
t_{HDC}	Hold Time BCLK Low to Data Invalid		20			ns

TIMING SPECIFICATIONS (continued)

DIGITAL INTERFACE TIMING : FORMAT 3

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Transition to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH} t_{WCL}	BCLK Width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		30			ns
t_{DCF}	Delay Time BCLK Transition to FSa Transition	TE Mode only			30	ns
t_{DCD}	Delay Time BCLK High to Data Valid		20		80	ns
t_{DFD}	Delay Tune FSa High to Data Valid	Load 100pF. Apply only if FSa Rises Later Than BCLK Rising Edge.			80	ns
t_{DCZ}	Delay Time BCLK Low to Data Invalid		20		80	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		20			ns
t_{HDC}	Hold Time BCLK Low to Data Invalid		20			ns
t_{DCC}	Delay Time BCLK High to CLK High	TE and NT2 T Side Modes only	0		30	ns

TIMING DIAGRAMS

Figure 9 : Serial Control Interface Timing.

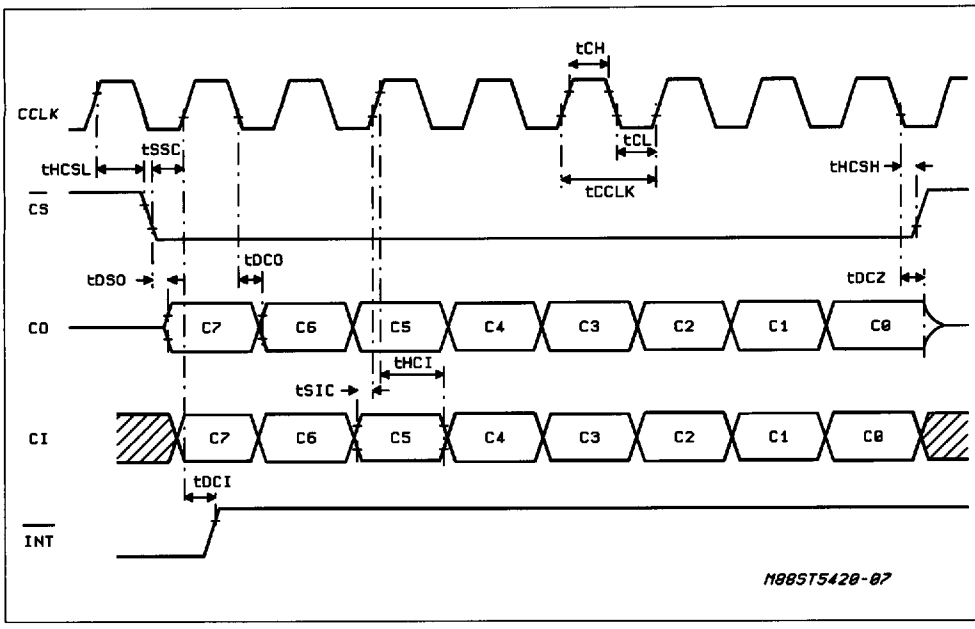


Figure 10 : Digital Interface - Formats 1 & 2 (similar to COMBO I/II non delayed data timing mode).

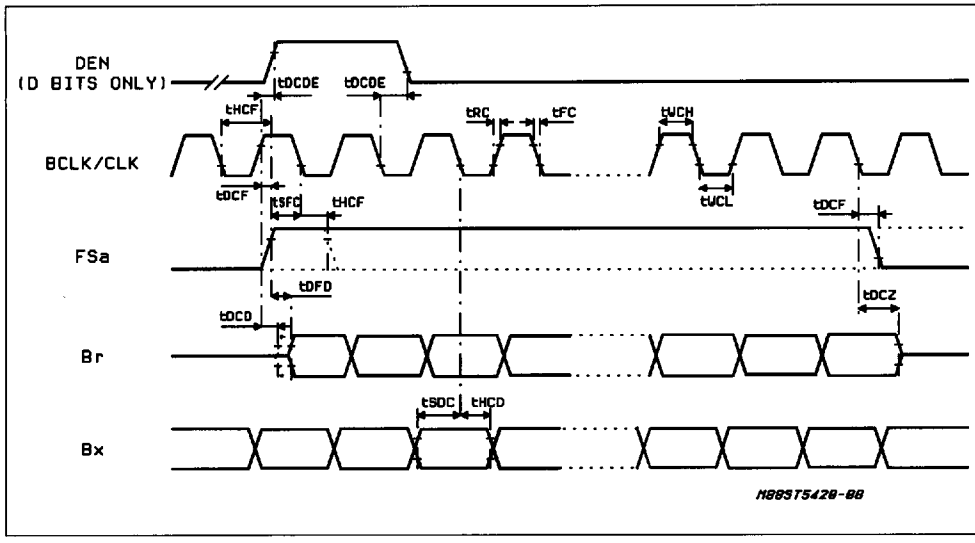


Figure 11 : Digital Interface Timing - Format 3 (GCI compatible).

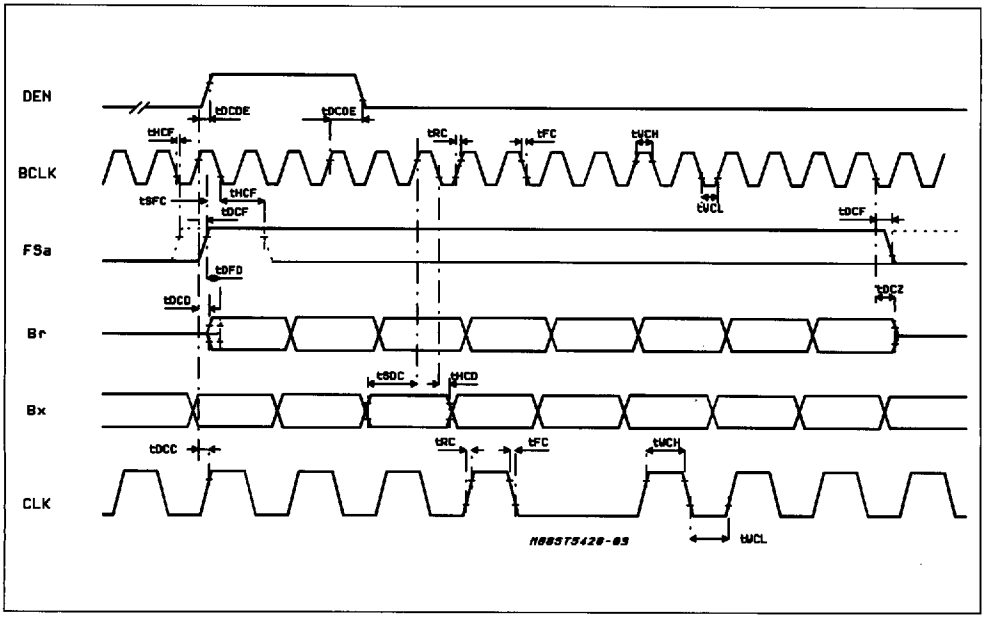


Figure 12 : Digital Interface - Formats 4 (similar to COMBO I/II non delayed data timing mode).