# ISDN Exchange Power Controller (IEPC) PEB 2025

**Preliminary Data** **CMOS IC**

| Type | Ordering Code | Package |
|---|---|---|
| PEB 2025-P | Q67100-H6038 | P-DIP-22 |

The IEPC is an integrated power controller especially designed for feeding two and four wire transmission lines. The IEPC is fully compatible to the CCITT recommendations on power feed at the "S" interface. So the IEPC can be used in PBX/Central Office and in intelligent NTs.

The IEPC supplies power to up to four transmission lines. Each line is individually powered and controlled via a microprocessor interface. An interrupt output signals any malfunction to the microprocessor.

**The High Voltage CMOS Technology (60 V) Ensures a Wide Field of Applications**

- Two and four wire transmission
- Point-to-point configurations
- Point-to-multipoint configurations

Programmable output current and thermal shut down guards the IEPC against overloads.

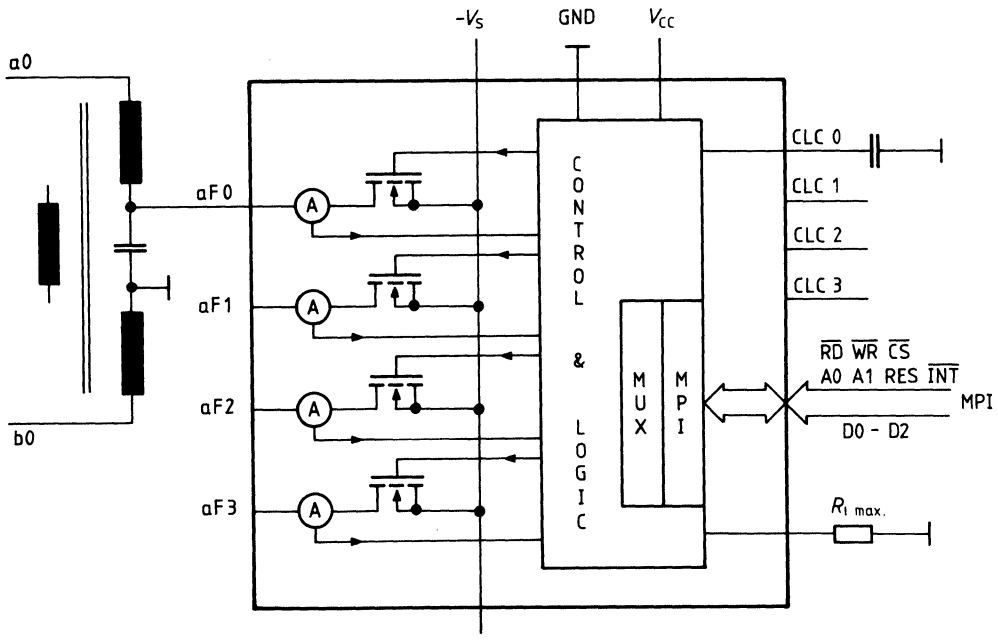
The IEPC offers a special transient permitted overload state. Momentary overloads within a specified range e.g. by connecting a TE to a powered line, will not activate the current limit circuits of the power controller. If overload is detected, the linedriver will turn off according to the time and current dependent turn off characteristic as described in FTZ 1R211.

The IEPC offers an automatic restart mode. In this case, the IEPC tries to power up the line periodically every 10 s, thus the feeding of a line will return automatically after the overload conditions are removed.

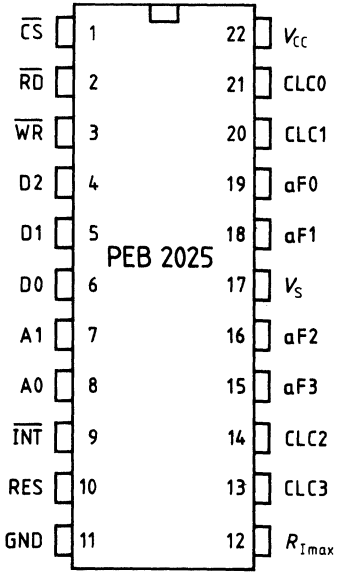
**Features**

- Supplies power to up to four transmission lines.
- CCITT recommendations compatible for power feed at the "S" interface.
- Each line is individually powered and controlled.
- Wide field of applications.
- Maximum output current programmable up to 100 mA.
- Programmable switch-off-characteristic by overcurrent detection.
- Automatic restart after removing overload conditions.
- Status detectors for each linedriver.
- Microprocessor compatible interface.
- Interrupt output for detection of any malfunction.
- High voltage CMOS technology (60 V).

**Figure 1**
**IEPC Functional Diagram**




**Pin configuration**
(top view)



**Pin Definitions and Functions**

| Pin No. | Symbol | Input (I) Output (O) | Function |
|---|---|---|---|
| 17 | $-V_S$ | I | **Supply Voltage:** This pin has to be connected to the negative supply voltage. $-V_S$ supplies power to all linedrivers. |
| 22<br>17 | $V_{CC}$<br>GND | I<br>I | **Digital Supply Voltage:** +5 V<br>**Ground** Digital<br>Note: GND has to be connected to ground battery (positive supply voltage). |
| 19, 18<br>16, 15 | aF0-aF3 | O | **a**-Line **F**eeding: $aF_i$ are the linedriver outputs |
| 12 | $R_{I\ max}$ | I | **Current Limit:** Using an external resistor connected between $R_{I\ max}$ and GND, the maximum line current is programmed. This programmed limit is the same to all linedrivers. |
| 21, 20,<br>14, 13 | CLC0-CLC3 | I | **C**urrent **L**imit **C**haracteristic: By connecting external capacitors between $CLC_i$ and GND, the time-dependent turn off-characteristics of the linedrivers are defined. |
| 1 | $\overline{CS}$ | I | **Chip Select:** A logic low on $\overline{CS}$ enables $\overline{RD}$ and $\overline{WR}$ communication between the processor and the IEPC. |
| 3 | $\overline{WR}$ | I | **Write:** A logic low on this pin when $\overline{CS}$ is low enables the IEPC to accept command words from the processor. |
| 2 | $\overline{RD}$ | I | **Read:** A low on this pin (if $\overline{CS}$ is low) enables the IEPC to release status onto the data bus for the processor. |
| 6, 5, 4 | D0-D2 | I/O | **Data Bus:** Control, status and command information is transfered via this bus between IEPC and processor. |
| 8, 7 | A0, A1 | I | **Address Bus:** These inputs select the internal registers while chip select is active. |
| 10 | RES | I | **Reset:** A logic high on the RES input sets the device into the initial state. |
| 9 | INT | O | **Interrupt:** Open-drain output. If any malfunction is detected by the IEPC, this interrupt-pin is activ low. |

**Figure 2**
**IEPC Architecture**

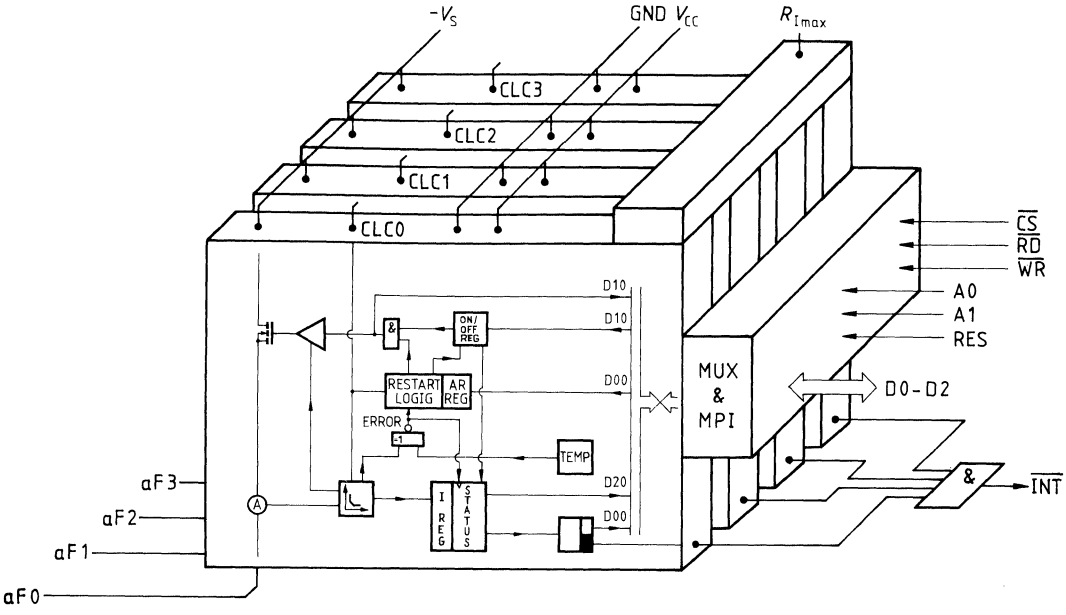
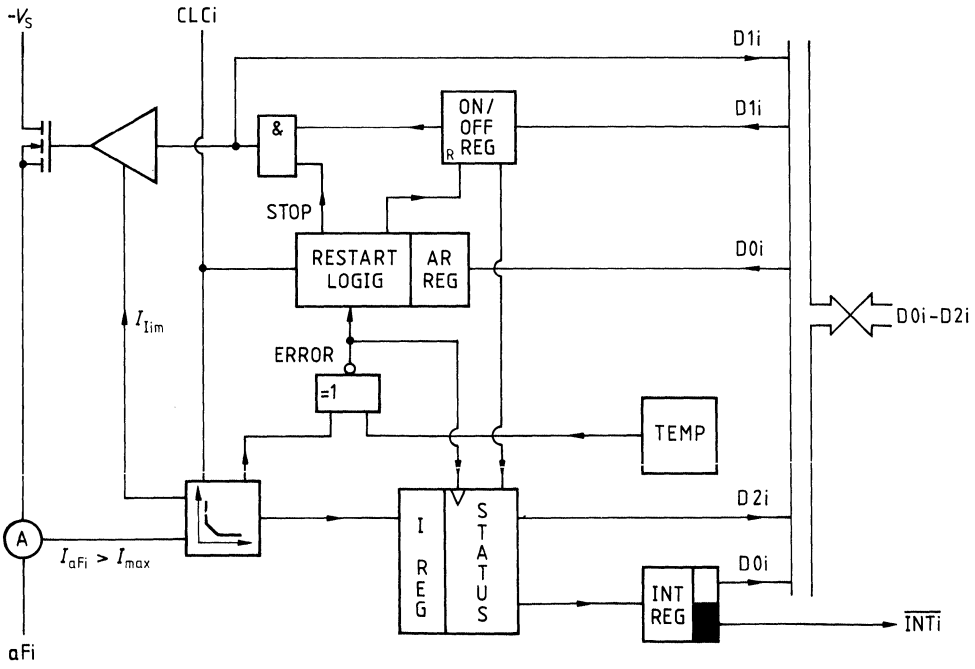


**Figure 3**
**Functional Diagram of One Linedriver i**




**Functional Description**

**Figure 2** shows the IEPC organization. The exchange power controller contains one linedriver for each of the four transmission lines. A line oriented register architecture allows very simple software control. **Figure 3** shows the functional diagram of one of the four linedrivers. The IEPC consists of a high voltage analog part and a low voltage digital part. The ground battery (positive supply voltage) has to be connected to GND (Pin 11).

When powering up the IEPC, the linedrivers are switched off and all registers are cleared. The same initialized state can be achieved by an external high signal applied to the reset RES.

## Analog Part

### Power Switches

The negative pole of the supply, e.g. an exchange battery, has to be connected to the pin $-V_S$. After an ON-command to line i, a high voltage MOS-FET will connect the negative supply voltage from $-V_S$ to $aF_i$. The ON-resistance of each transistor is less than 10 Ω.

### Current Control

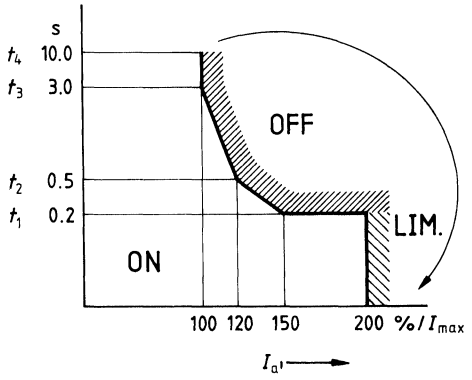
The current of each negative wire ($aF_i$) is controlled individually. The maximum feeding current is programmed by an external resistor $R_I$ connected between pin $R_{I\ max}$ and GND **(figure 1)** and is the same to all four lines.

$$R_I\ [k\Omega] \approx 700/I_{max}\ [mA]$$

**$aF_i$ line control:** Connecting an external capacitor between CLC and GND **(figure 1)**, the IEPC offers a special time and current dependent turn off characteristic. To meet the FTZ 1R211 recommendations, the value of the capacitor should be 10 µF. Additionally, the IEPC will limit the $aF_i$ line current to 2.0 $I_{max}$, in order to protect the IEPC against over currents and to avoid discharging of the feeding source. **Figure 4** shows this **t**ransient **p**ermitted **o**verload (TPO) state.

During the first 200 ms since overload of the negative wire $aF_i$ was detected ($IaF_i \geq I_{max}$), the current will be limited to 2.0 $I_{max}$. Within the next 300, ms the current must drop from 1.5 $I_{max}$ to 1.2 $I_{max}$, otherwise the linedriver turns off. After 3 s, any current above $I_{max}$ results in turn off the linedriver. 10 s after overload is detected, if no turn off of the linedriver has accured, the current limiting characteristic becomes active again and will be prepared for detection of further overload conditions.

**Figure 4**
**Diagram of the Transient Permitted Overload (TPO) State**



The time dependence of the turn-off characteristic is based on the value of the external capacitor $C_t$ at pin CLC:

$$t_1 \text{ [sec]} \approx C_t \text{ [µF]}/50$$
$$t_2 \approx 2.5\, t_1;\ t_3 \approx 15\, t_1;\ t_4 \approx 50\, t_1.$$

If pin CLC is connected to GND, the time and current dependent turn off characteristic is disabled and the IEPC limits the driver current to 2 $I_{max}$.

**Temperature Shut-Off**

The temperature of each linedriver is monitored separately. If the temperature of one linedriver exceeds shut-off temperature, the transmission line will turn off. The shut-off temperature of the other three linedrivers will be increased.

**Autorestart**

In connection with the time-dependent-current-limitation, the IEPC offers an autorestart mode. If overload was detected and the linedriver has been switched off, an automatic restart can be programmed (see digital part). It should be noticed, however, that autorestart is only possible if the time- and current-dependent-turn off mode is used, i.e. a capacitor is connected between $CLC_i$ and GND. The delay time depends on value of the capacitor.

**Digital Part**

The microprocessor interface (MPI) communicates with a processor which controls the IEPC. This MPI contains a 3-bit data bus, 2-bit address bus, read-, write-, chip select- and reset lines.

If chip select is inactive (logic high) the data bus is in a high impedance state and no communication between the processor and IEPC is possible. The IEPC contains a line oriented register architecture, i.e. one read and one write register for each line. A read or write cycle affects the addressed register, which is related to the corresponding linedriver.

The write register consists of three control bits per line i:

D0: Autorestart-bit (AR)
D1: ON/OFF-bit (ON)
D2: must be 0

The read register consists of three status bits per line i:

D0: Interrupt-bit (INT)
D1: Actual ON/OFF driver status-bit (AO)
D3: Current overload-bit

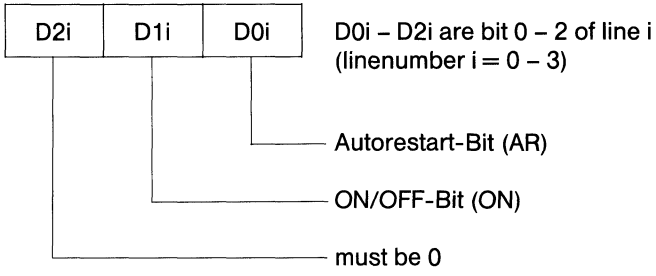
A logic high on the RES pin sets the device into an initial state: all registers of the IEPC are cleared (D0i – D2i are low).

**Address Table**

| $\overline{CS}$ | A1 | A0 | Selected Line |
|---|---|---|---|
| 0 | 0 | 0 | Line 0 |
| 0 | 0 | 1 | Line 1 |
| 0 | 1 | 0 | Line 2 |
| 0 | 1 | 1 | Line 3 |
| 1 | x | x | No Access |

**Write Register**

The write register is organized as shown below:




**Autorestart-Bit:** If autorestart-mode is needed an external capacitor must be connected between pin CLCi and GND. If D0 is high, autorestart mode is enabled.

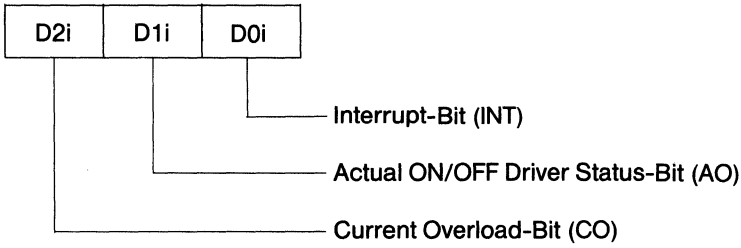
| | D2i | D1i | D0i |
|---|---|---|---|
| AR Enabled | 0 | x | 1 |
| AR Disbaled | 0 | x | 0 |

**ON/OFF-Bit:** To turn on a linedriver, D1i must be set to high, to turn off it must be set to low. An off command resets the time and current dependent turn off characteristic by discharging the external capacitor at pin CLCi.

| | D2i | D1i | D0i |
|---|---|---|---|
| ON | 0 | 1 | x |
| OFF | 0 | 0 | x |

**Read Register**

The read register is organized as shown below:




**Interrupt-Bit:** If malfunctions have been detected (current- or thermal overload) and the linedriver of line i has been turned off the interrupt-bit will be set:

| | D2i | D1i | D0i |
|---|---|---|---|
| Interrupt | x | x | 1 |
| Operational | x | x | 0 |

The interrupts $\overline{INT0}$ – $\overline{INT3}$ are ANDed to the device output-signal $\overline{INT}$. Thus if any malfunction is detected an interrupt signal is sento the the microprocessor.

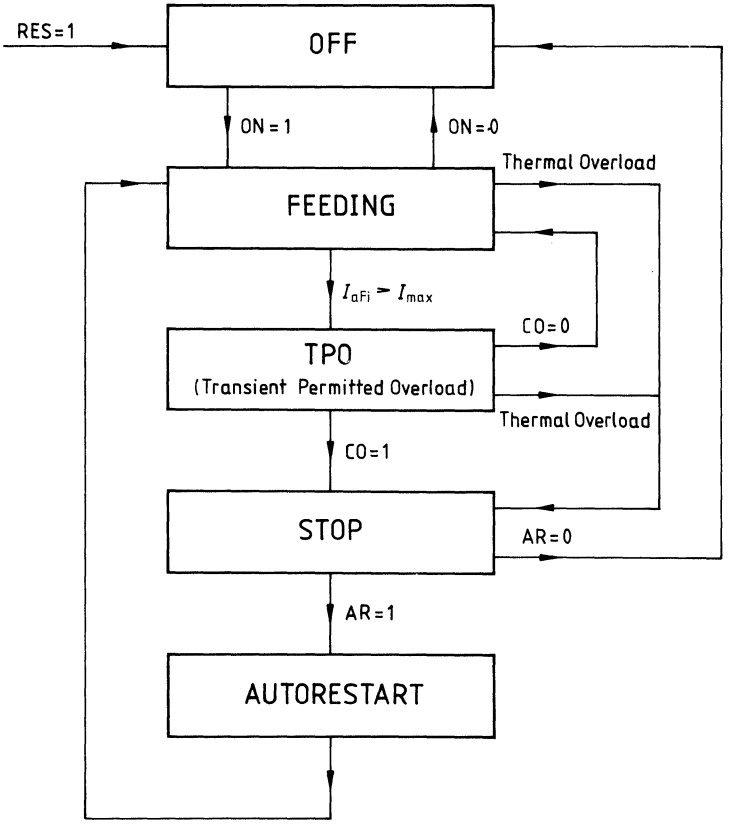
**Actual ON/OFF Driver Status-Bit:** D1i shows the actual status of the linedrive on line i:

| Driver | D2i | D1i | D0i |
|---|---|---|---|
| DRIVER ON | x | 1 | x |
| Driver OFF | x | 0 | x |

**Current Overload-Bit:** If $IaF_i \geq I_{max}$ is detected and the linedriver has been switched off the current overload bit will be set.

| | D2i | D1i | D0i |
|---|---|---|---|
| Current overload | 1 | x | x |
| Operational | 0 | x | x |

**Figure 5**
**Linedriver State Diagram**



**State Diagram**

**Figure 5** shows the diagram of one IEPC linedriver.

A logic high on the RES input sets the device into the initial state. The linedriver is switched off and all registers are cleared. The same initialized state is achieved by powering up the IEPC. After an ON-command (ON = 1), the linedrivers will turn on and the IEPC is the FEEDING-state. To return to the OFF-state the ON-bit must be cleared (ON = 0).

In the FEEDING-state, the current $IaF_i$ is controlled. If overcurrent is detected, one of the following cases happens:

1. If an external capacitor is connected between $CLC_i$ and GND and $IaF_i \geq I_{max}$ is detected, the IEPC stays in the **Transient P**ermitted **O**verload-state (TPO). Exceeding the time-current-limit, the linedriver turns off and the IEPC is in the STOP-state. The current overload-bit will be set (CO = 1). If no exceeding happens, the linedriver returns to the FEEDING-state.

2. If $IaF_i \geq I_{max}$ is detected and $CLC_i$ is connected to GND, the IEPC limits the driver current to 2 $I_{max}$. The current overload bit will not be set.

The temperature of each linedriver is controlled separately. If the temperature of one linedriver exceeds the shut-off temperature, the transmission line will turn off and the linedriver is in the STOP-state. In this case, the shut-off temperature of the other three linedrivers will be increased.

There are two different ways to leave the STOP-state:

1. If the autorestart bit is set (AR = 1), the IEPC returns after a delay time to the FEEDING-state automatically. The ON/OFF register will not be cleared.
2. If no autorestart mode is selected (AR = 0), the IEPC returns to the OFF-state. In this case, the ON/OFF register will be cleared.

As soon as the STOP-state is reached the IEPC sends an interrupt signal to the microprocessor (interrupt-pin is active low).

If the linedriver i is not in the thermal overload state, every rising edge of the read signal resets the interrupt bit $INT_i$ (DOi) of the selected line i. The current overload-bit COi (D2i) is reset too.

If the linedriver i is in the thermal overload state, the rising edge of the read signal has no effect on the interrupt bit.

The internal interrupts $\overline{INT0}$ - $\overline{INT3}$ are ANDed to the open drain output pin $\overline{INT}$. So the interrupt pin stays active low until all interrupt bits $INT_i$ are reseted.

## Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | Unit |
|---|---|---|---|
| Supply voltage referred to GND | $-V_S$ | −70 | V |
| $V_{CC}$ referred to GND | $V_{CC}$ | 6 | V |
| On any other pins referred to GND | $V_S$ | −0.5 to 6 | V |
| Reverse current on pins aF0 – aF3 | $I_S$ | 0 | mA |
| Power dissipation | $P_D$ | 1 | W |
| Ambient temperature under bias | $T_A$ | −25 to 85 | °C |
| Storage temperature | $T_{stg}$ | −40 to 125 | °C |
| Thermal resistance junction to ambient | $T_j$ | 50 | K/W |

## Operating Range

$T_A = 0$ to 70 °C, $V_S = -60$ V, $V_{CC} = 5$ V ± 5%, GND = 0 V

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| **Linedrivers** | | | | |
| Operating voltage ($-V_S$ – GND) | $-V_S$ | −12 | −60 | V |
| Feeding current ($aF_i$) | $I_F$ | | 100 | mA |
| Current limiting ($aF_i$) | $I_{LIM}$ | | 200 | mA |
| Turn-on resistance ($-V_S$ – $aF_i$) | $R_{DSON}$ | | 10 | Ω |
| Delay: ON-Command to turn on linedriver[1]) | $t_{ON}$ | | 0.5 | ms |
| Delay: OFF-Command to turn off linedriver | $t_{OFF}$ | | 2 | ms |

[1]) for res. loads

**Operating Range** (cont'd)
$T_A = 0$ to 70 °C, $V_S = -60$ V, $V_{CC} = 5$ V ± 5%, GND = 0 V

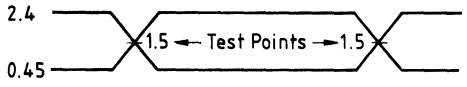
| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| **Control & Logic** | | | | |
| Autorestart period $I_O = 2$ mA | $t_{ar}$ | 10 | | s |
| **MPI** | | | | |
| L-input voltage | $V_{IL}$ | −0.5 | 0.8 | V |
| H-input voltage | $V_{IH}$ | 2.0 | $V_{CC}$ | V |
| L-output voltage $I_O = 2$ mA | $V_{OL}$ | | 0.45 | V |
| H-output voltage $I_O = 1$ mA | $V_{OH}$ | 2.4 | | V |
| Reset pulse width | $t_{RES}$ | 5 | | µs |

**Switching Times**

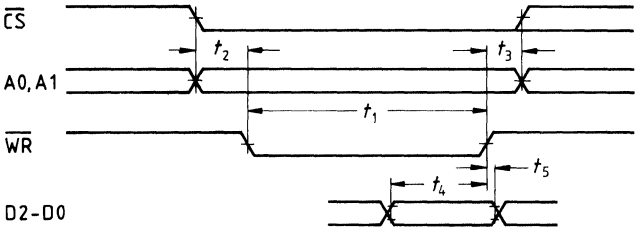
| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| $\overline{RD}$ or $\overline{WR}$ pulse width | $t_1$ | | | ns |
| Address and $\overline{CS}$ setup time to $\overline{RD}\downarrow$ or $\overline{WR}\downarrow$ | $t_2$ | | | ns |
| Address and $\overline{CS}$ hold timer after $\overline{RD}\uparrow$ or $\overline{WR}\uparrow$ | $t_3$ | | | ns |
| Data setup time to $\overline{WR}\uparrow$ | $t_4$ | | | ns |
| Data hold time after $\overline{WR}\uparrow$ | $t_5$ | | | ns |
| Data valid after $\overline{RD}\downarrow$ | $t_6$ | | | ns |
| Data valid after $\overline{RD}\uparrow$ | $t_7$ | | | ns |
| Data bus inactive after $\overline{RD}\uparrow$ | $t_8$ | | | ns |

## Waveforms

AC Testing Input, Output Waveform




Write Timing




Read Timing