SIEMENS

ISDN D-Channel Exchange Controller (IDEC) PEB 2075

Preliminary Data **ACMOS IC**

Type	Ordering code	Package
PEB 2075-P	Q67100-H8682	P-DIP-28
PEB 2075-N	Q67100-H8683	PL-CC-44 (SMD)

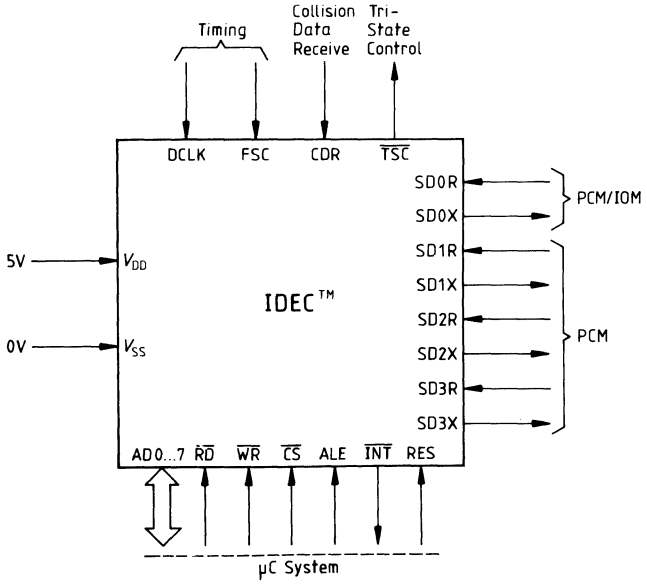
The ISDN Digital Exchange Controller PEB 2075 (IDEC™) is a serial HDLC data communication circuit with four independent channels. Its telecommunication specific features make it especially suited for use in variable data rate PCM systems. In addition, the device contains spohisticated switching functions and it implements automatic contention resolution between packet data from different sources.

Its applications include: communication multiplexers, peripheral ISDN line cards, packet handlers, X.25 packet switching devices. The IDEC is a fundamental building block for networks with either centralized, de-centralized or mixed signaling/ packet data handling architectures.

Features

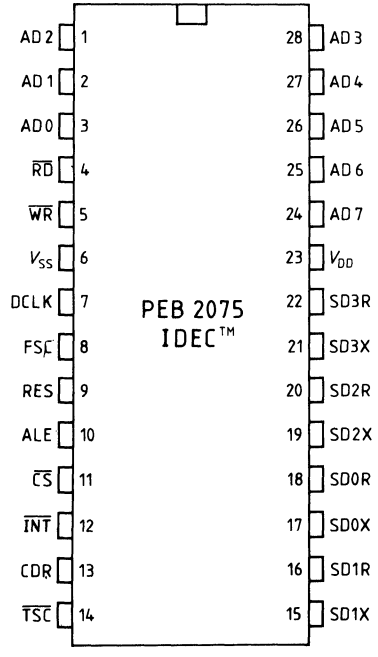
- Four independent HDLC channels
- 64 byte FIFO storage per channel and direction
- Handling of basic HDLC functions
  Flag detection/generation
  Zero deletion/insertion
  CRC checking/generation
  Check for abort
- Single connection and quad connection modes
- IOM® interface or PCM interface
- Programmable time slots and channel data rates (up to 4 Mbit/s)
- Different methods of contention resolution
- 8-bit parallel microcontroller interface with vectored interrupt
- Advanced CMOS technology
- Power consumption less than 50 mW.

Logic Symbol



Pin Configuration

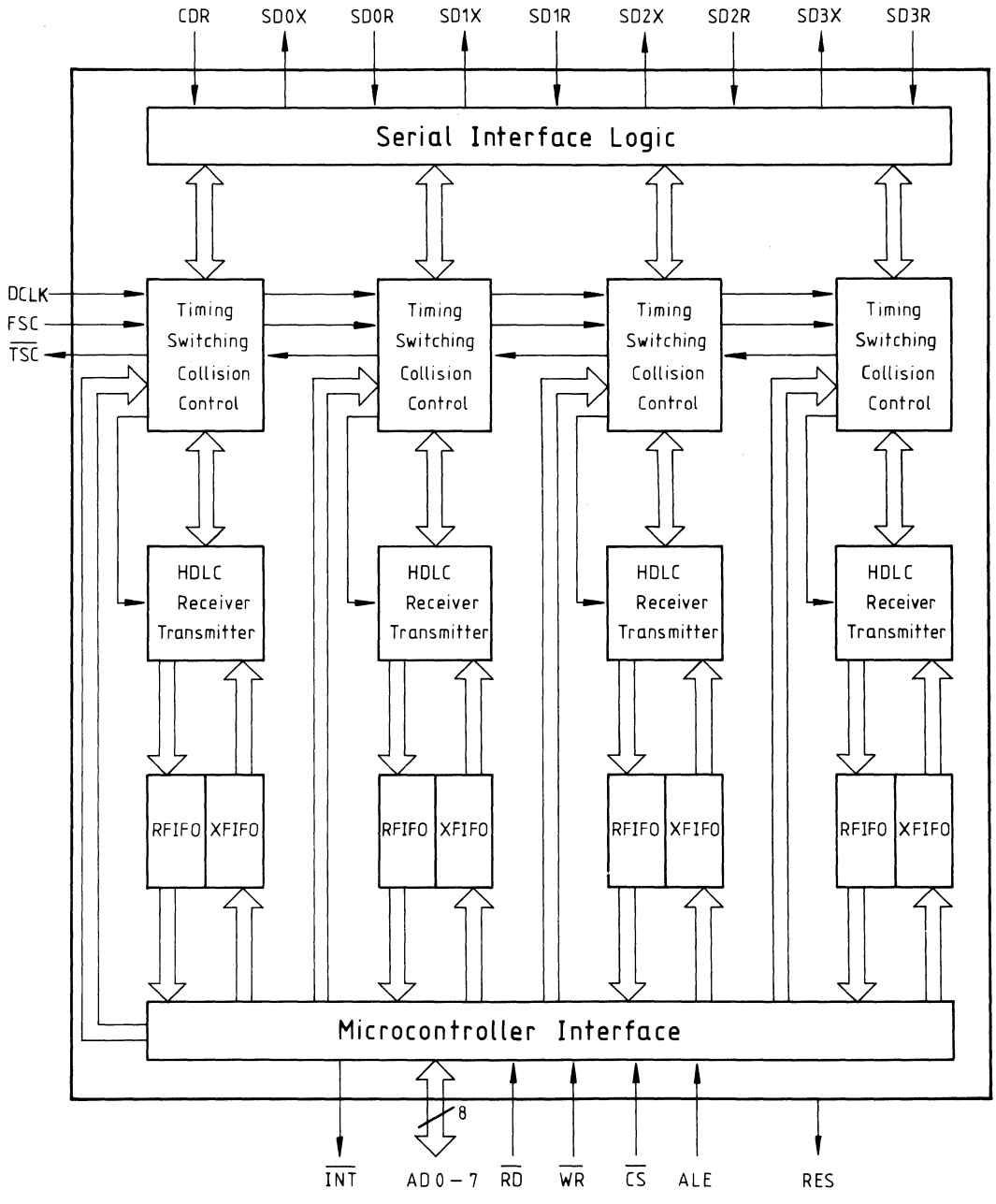
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Functions
3 2 1 28 27 26 25 24	AD 0 AD 1 AD 2 AD 3 AD 4 AD 5 AD 6 AD 7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address-Data Bus.** The multiplexed address-data bus transfers data and commands between the µP system and the IDEC.
11	$\overline{CS}$	I	**Chip Select.** A low on this line selects the IDEC for a read/write operation.
5	$\overline{WR}$	I	**Write.** A low on this line indicates a write operation.
4	$\overline{RD}$	I	**Read.** A low on this line indicates a read operation.
12	$\overline{INT}$	OD	**Interrupt Request.** This line is activated when the IDEC requests an interrupt. It is an open drain output.
10	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address-data bus, selecting one of the internal sources or destinations.
18 16 20 22	SD0R SD1R SD2R SD3R	I	Serial Data Receive
17 15 19 21	SD0X SD1X SD2X SD3X	O	Serial Data transmit Serial Data transmit Serial Data transmit Serial Data transmit Serial Data transmit Serial Data transmit Collision output
7	DCLK	I	**Data Clock;** supplies a clock signal either equal to or twice the data rate.
8	FSC	I	Frame Synchronization or data strobe signal
14	$\overline{TSC}$	O	**Time-Slot Control.** Supplies a control signal for an external driver.
13	CDR	I	**Collision Data Receive.**
9	RES	I	Reset
6	V_{SS}	I	Ground
23	V_{DD}	I	Supply voltage +5 V

Figure 1
Block Diagram



1. System Integration

Communication Multiplexers

The four independent serial HDLC communication channels implemented in the IDEC make the circuit suitable for use in communication multiplexers.

The collision detection/resolution capability of the circuit allows statistical multiplexing of packets in one or several physical data communication channels, for example in DMI (mode 3) applications.

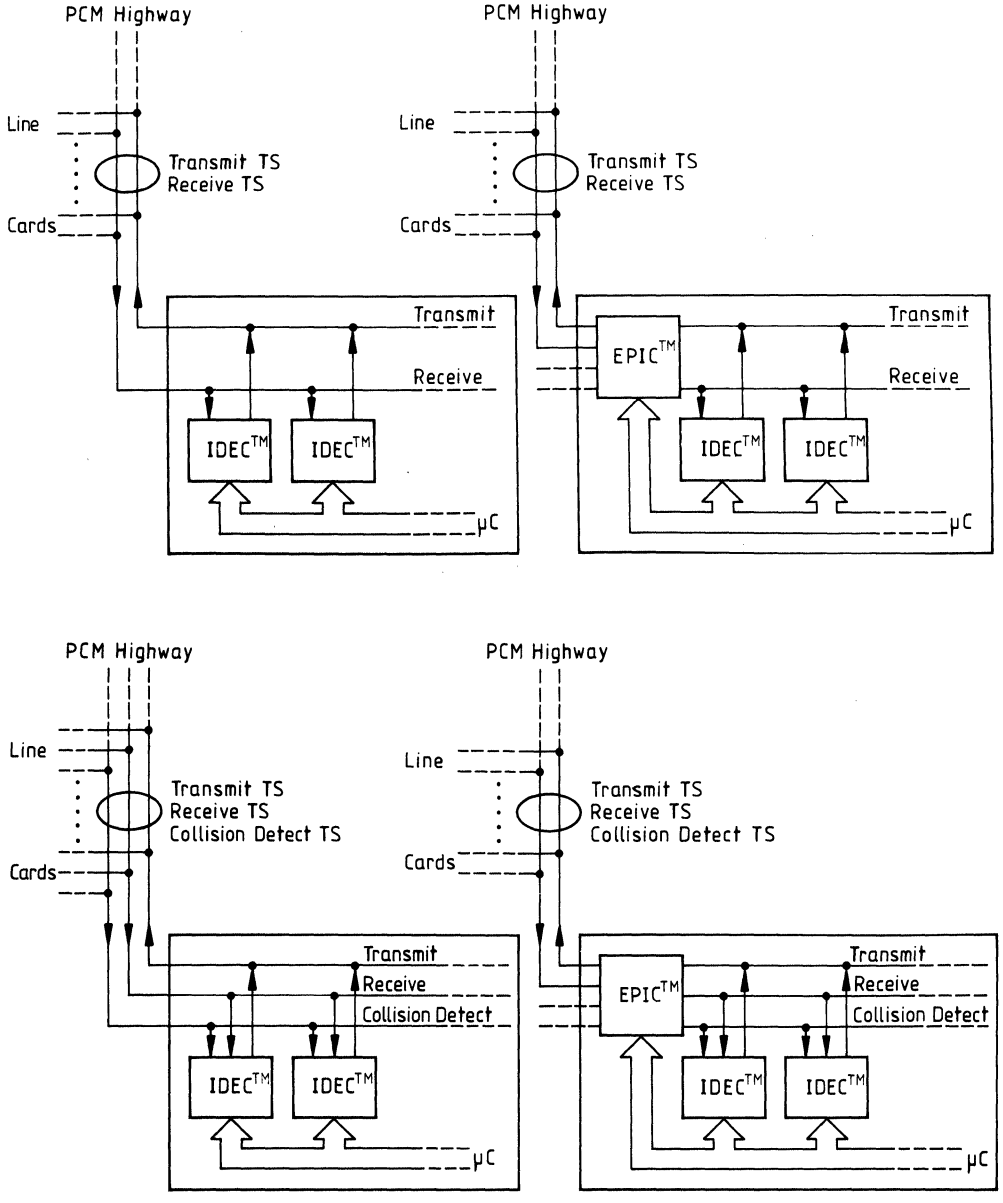
Centralized Signaling Data Packet Handlers

The IDEC can be used in central packet handlers of ISDN networks to process signaling or packet data of four ISDN subscribers. In this application, it may be used with or without the Extended PCM Interface Controller (EPIC) PEB 2055.

The IDEC can be connected to the IOM interface of the EPIC, which is itself connected to the PCM system highway. The EPIC implements concentration and time-slot assignment functions. As an alternative, the IDEC may be directly connected to PCM highways **(figure 2)**.

The size (from 1 to 8 bits) and the position of the time slot associated with each HDLC controller are software programmable. In addition to the receive and transmit data highways, the IDEC accepts a third input connection for collision detection purposes. The mode of collision detection is programmable. A "collision highway" (or time slot) can be used for remote collision control, as a "clear to send" lead, or for local contention resolution among several IDECs.

Figure 2
Use of IDEC in Central Signaling Data Packet Handlers



Line Cards De-Centralized or Mixed Signaling/Data Packet Handling Architectures

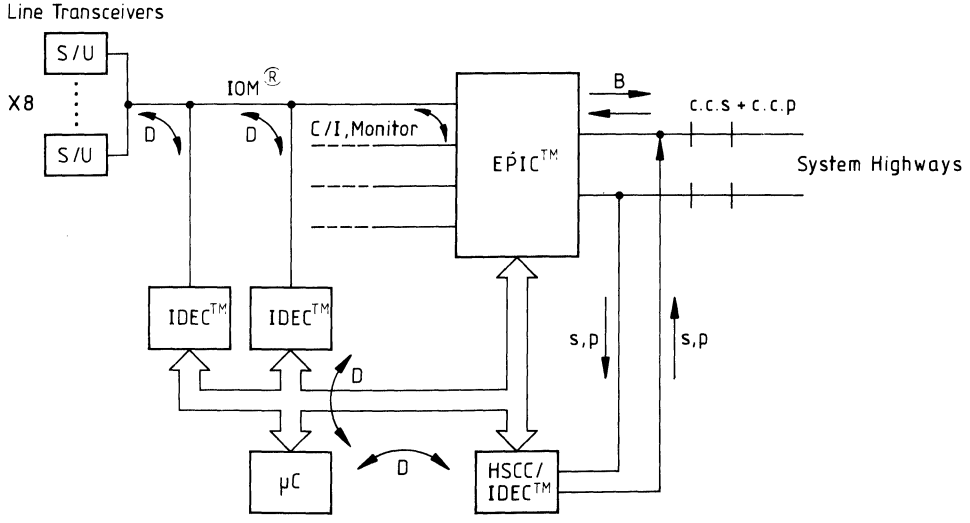
The IDEC can be used on peripheral line cards to process D-channel packets for ISDN subscribers. An Extended PCM Interface Controller PEB 2055 has the layer 1 controlling capacity and a B and D channel switching capacity for a total of 32 subscribers. The B and D channels and the control information for eight subscribers are carried over one IOM interface. Thus a line card dimensioned for 32 ISDN subscribers may employ up to eight IDECs, two for each IOM connection **(figure 3)**. A High Level Serial Communication Controller (HSCC) SAB 82520 with two HDLC channels, or another IDEC may be used to transmit and receive signaling over the system highway in a common channel. Again, such a common channel may be shared among several line cards, due to the statistical multiplexing capability of these controllers.

In completely de-centralized D-channel processing architectures, the processing capacity of a line card is usually dimensioned to avoid blocking situations even under maximum conceivable D-channel traffic conditions. It may sometimes be more advantageous to perform p-packet handling in a centralized manner while keeping s-packet handling on the line cards. A statistical increase in p-packet traffic has then no effect on the line card, and can be easily dealt with by one of the modular architectures for a central packet handler shown in the previous section. A more effective sharing of the total p-packet handling capacity is the result, especially in a situation where p-packet traffic patterns vary widely from one subscriber group to another.

The use of IDEC in the mixed D-channel processing architecture is illustrated in **figure 4)**.

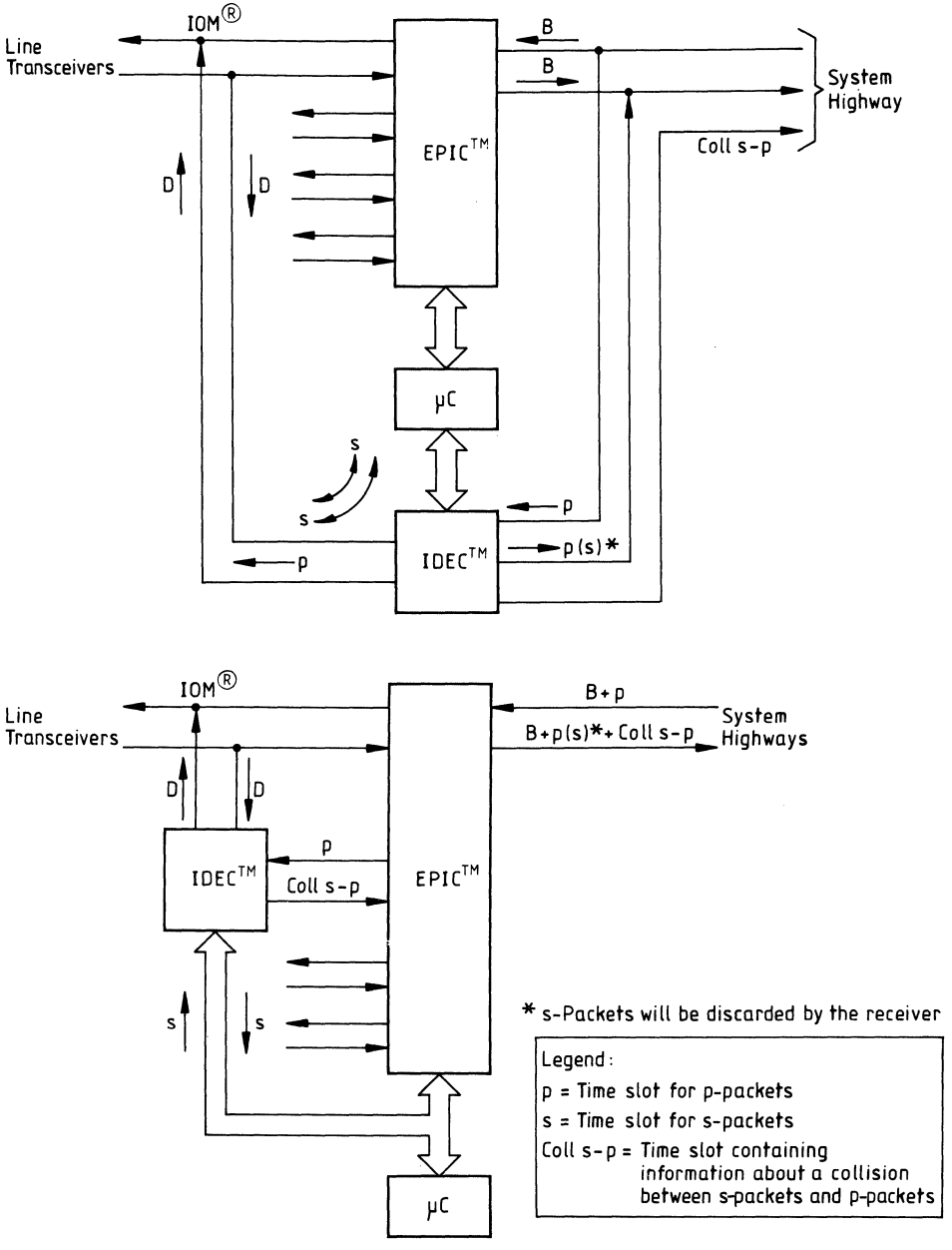
The additional "transparent data" connections supported by the IDEC enable a merging of p- and s-packets into one D-channel. Possible collision situations are dealt with by the IDEC which uses either the additional collision detect line **(figure 4a)** or a time slot on the system highway **(figure 4b)** from the line card to the central packet handler.

Figure 3
Line Card in a De-Centralized D-Channel Handling Architecture



Legend:
c.c.s/p = Common channel for signaling and for packed data, respectively
C/I,Mon = Control/Indication and Monitor channels of the IOM interface

Figure 4a; 4b
IDEC on a Line Card in a Mixed D-Channel Processing Architecture



2. Functional Description

General Functions and Device Architecture

The IDEC is an HDLC controller which handles four HDLC communication channels, each channel fully independent and programmable by its own register set. The circuit performs the following functions:

- Extraction (reception) and insertion (transmission) of the HDLC data packets in a time division multiplex bit stream.
- Implementation of the basic HDLC functions of the layer-2 protocol.
- Interfacing of the data packets to the microprocessor bus. For the temporary storage of data packets overlapping FIFO structures are used per channel and direction.
- Switching of data between serial interfaces.
- Implementation of different types of collision resolution.
- Test functions.

Operating Modes

Each HDLC controller of the IDEC is assigned to one time channel governed either by time slot assignment or by an external strobe signal.

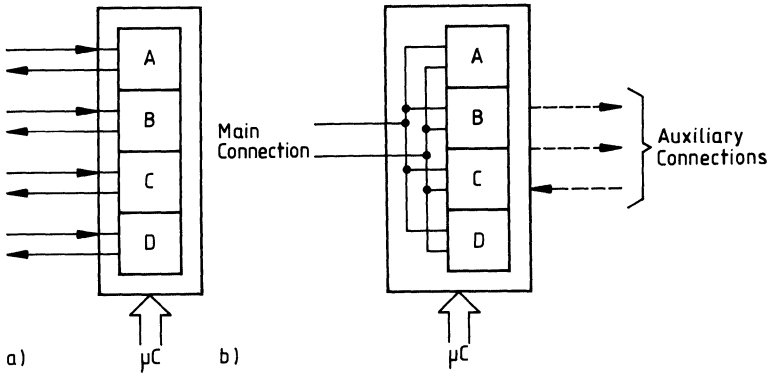
Two basic configurations are distinguished **(figure 5):**

- In the quad connection configuration the four HDLC controllers (A-D) are connected to individual time multiplexed communication lines;
- In the single connection configuration the four HDLC channels are all connected to one time multiplexed communication line.

Figure 5

(a) Quad Connection and

(b) Single Connection Configuration.



In the quad connection configuration two modes are distinguished as follows:

- Each connection is a time slotted highway, the lengths and positions of the time slot are programmable (quad connection time-slot mode);
- Each connection is a communication line, the time channels are marked by an external strobe signal (quad connection common control mode).

Two modes are distinguished in turn for the single connection configuration as follows:

- The connection is a standard IOM interface with predefined channel positions (single connection IOM mode);
- The connection is a time slotted highway (single connection time-slot mode).

For simplicity, a time slotted highway will sometimes be referred to as a "PCM highway", or PCM for short.

Table 1

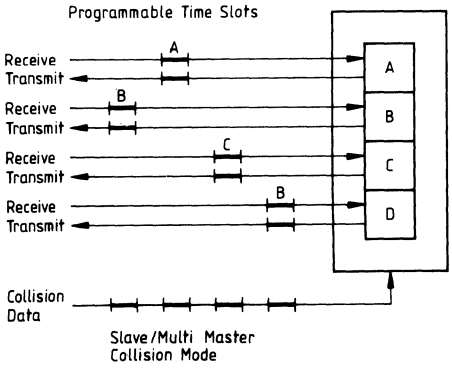
Four Basic Operating Modes of the IDEC

MDS1	MDS0	Mode Description
0	0	Single connection time-slot mode
0	1	Quad connection common control mode
1	0	Single connection IOM mode
1	1	Quad connection time-slot mode

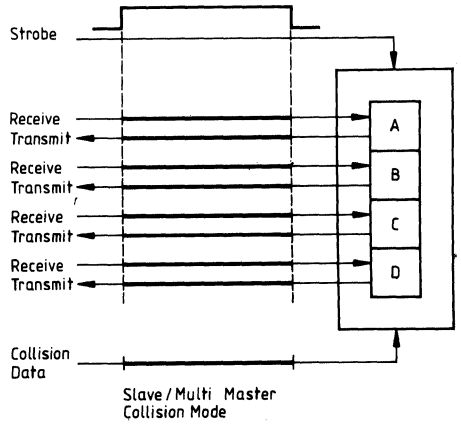
The four modes of operation are illustrated in **figure 6**. Via channel-by-channel programming, one of a number of collision detection modes may be selected in each of the basic modes of operation. For future reference, they are also depicted in **figure 6**.

Figure 6
Operating modes of the IDEC

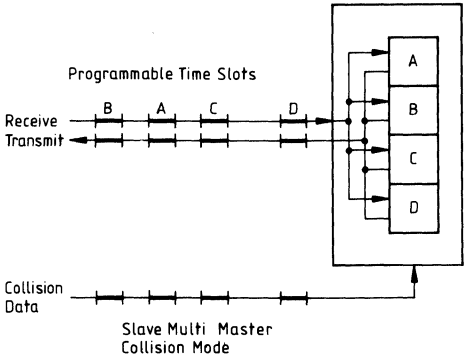
a. Quad Connection TS Mode



b. Quad Connection Common Control Mode



c. Single Connection TS Mode



d. Single Connection IOM Mode

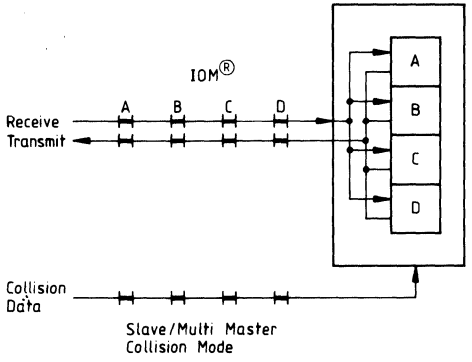
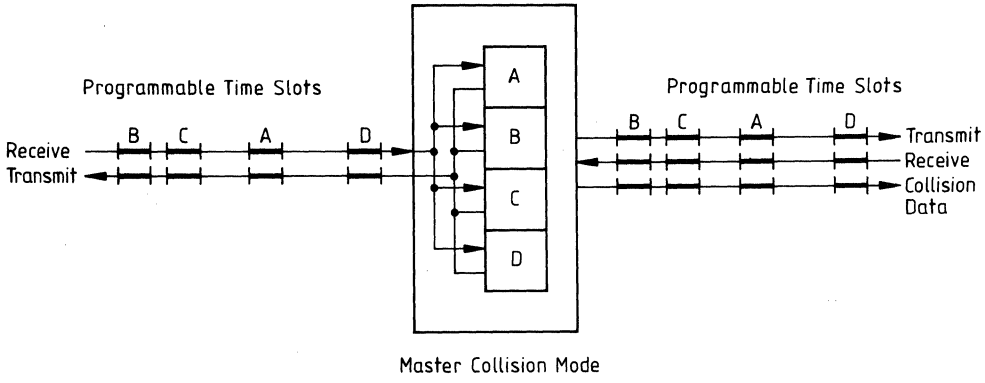


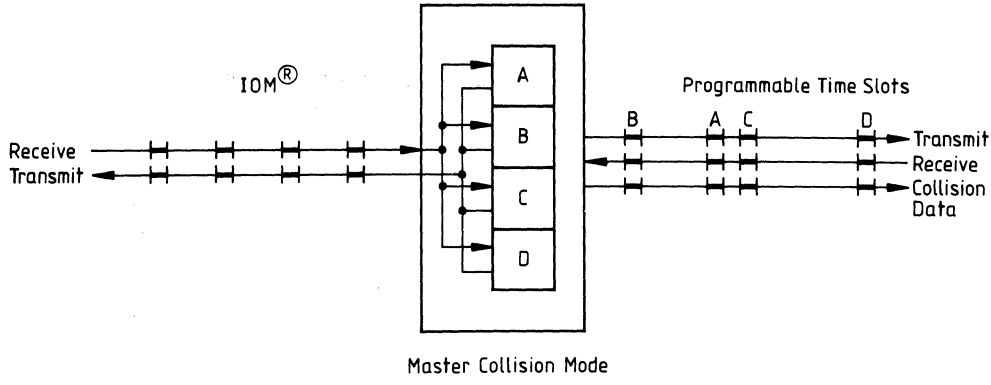
Figure 6 (continued overleat)

e. Single Connection TS Mode



Master Collision Mode

f. Single Connection IOM Mode



Master Collision Mode

Interfaces

Microcontroller Interface

The IDEC is programmable over an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 lines and is directly compatible with processors of the multiplexed address/ data bus type.

Table 2
Microcontroller Interface Signals of the IDEC

Symbol	Type	Name and Functions
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address-Data bus.** The multiplexed address/data bus transfers data and commands between the µC system and the IDEC.
$\overline{CS}$	I	**Chip Select.** A low on this signal selects the IDEC for a read/write operation.
$\overline{WR}$	I	**Write.** This signal indicates a write operation.
$\overline{RD}$	I	**Read.** This signal indicates a read operation.
$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the IDEC requests an interrupt. It is an open drain output.
ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address/data bus.

In addition to 8-bit processors, the IDEC supports a direct connection to 16-bit processors. Thus, through an internal address transformation, it is possible to access all IDEC registers using either even microprocessor addresses only or odd microprocessor only.

Note: The IDEC is now also available in a PL-CC-44 package with a demultiplexed address-data bus. For more information, see the latest IDEC Technical Manual.

Serial Interface

Depending on the selected mode, the IDEC supports four physically separate, full duplex serial interfaces, or one full duplex interface.

In addition to the data input and data output lines, the serial interface requires a common data clock (input DCLK) and a frame synchronization signal (input FSC). Input data is latched on the falling edge of DCLK and output data is clocked off on the rising edge of DCLK. The IDEC may be programmed so that the data clock rate is either equal to data rate, or twice the data rate.

Register Description

Register Address Layout

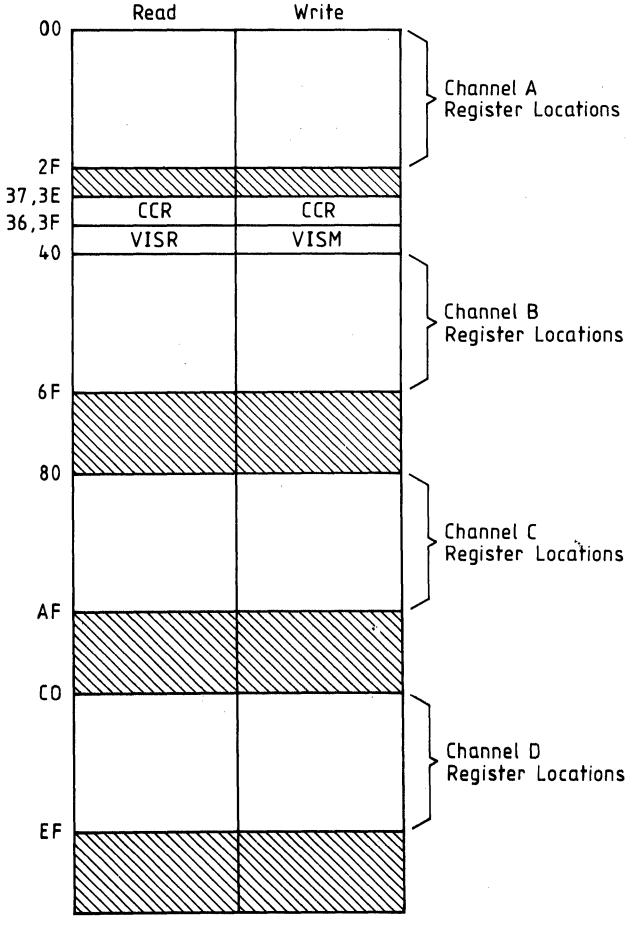
The register set consists of:

- one configuration register common to all four channels (CCR)
- a maskable vectored interrupt status register (VISR, VISM)

and, for each of the four channels, a set of individual registers **(figure 7)**.

In order to support the use of a 16-bit microcontroller, each register can be accessed with an even and an odd address value.

Figure 7
IDEC Register Map



The address map of the individual registers of each channel is shown in **table 2.** In order to obtain the actual address of a register, a "base" has to be added to the address given in the table, as follows:

Base = 00 for channel A
40 for channel B
80 for channel C
C0 for channel D.

Table 2

Address				
Even		**Odd**	**Read**	**Write**
00	to	1F	RFIFO	XFIFO
20		29	ISTA	ISM
28		21	STAR	CMDR
22		2B	MODE	MODE
2C		25	RFBC	TSR

For a detailed register description, see the IDEC data sheet.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
L-input voltage		V_{IL}	−0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{CC}+0.4	V	
L-output voltage		V_{OL}		0.45	V	$I_{OL} = 2$ mA
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD}−0.5		V V	$I_{OH} = -400$ µA $I_{OH} = -100$ µA
Power supply current	operational	I_{CC}			mA	$V_{DD} = 5$ V, input at 0 V/V_{DD}, no output loads
	power down				mA	
Input leakage current Output leakage current		I_{LI} I_{LO}		±10 µA		0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

$T_A = 25$ °C, $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Input capacitance	C_{IN}		7	pF	
I/O	C_{IO}		7	pF	

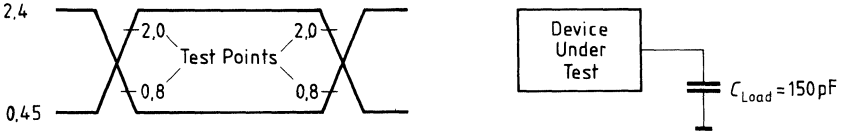
AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

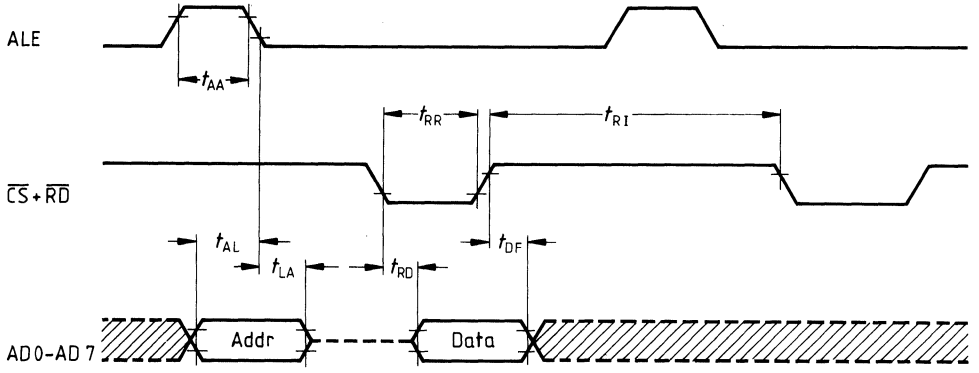
The AC testing input/output waveforms are shown below.

Figure 8
Input/Output Waveform for AC Tests

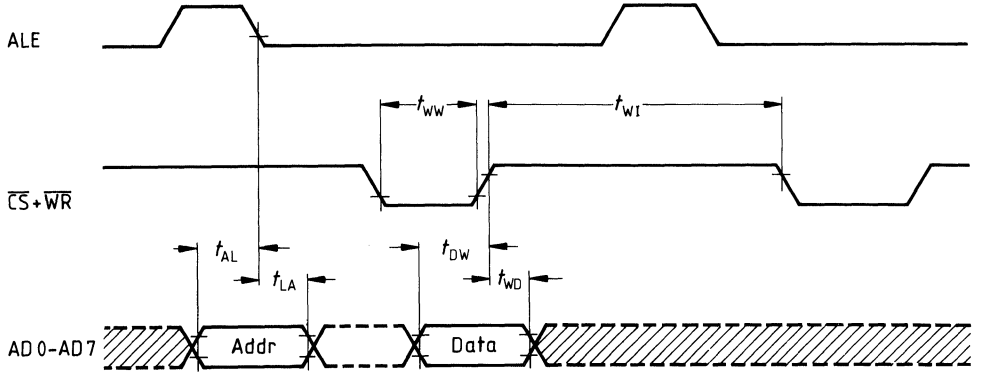


Microcontroller Interface Timing

µP Read Cycle



µP Write Cycle



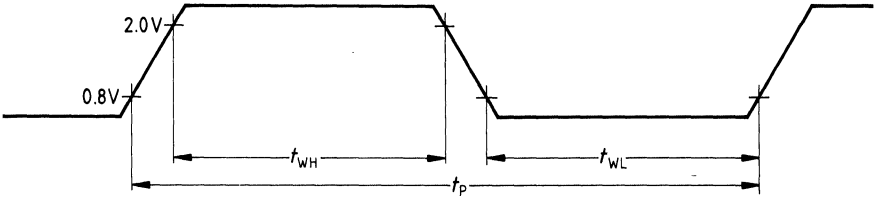
Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	20		ns
Address hold time from ALE	t_{LA}	10		ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		120	ns
Data float delay from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	75		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ + $\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}$ + $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

Serial Interface Timing

DCLK Characteristics

Definition of DCLK Period and Width



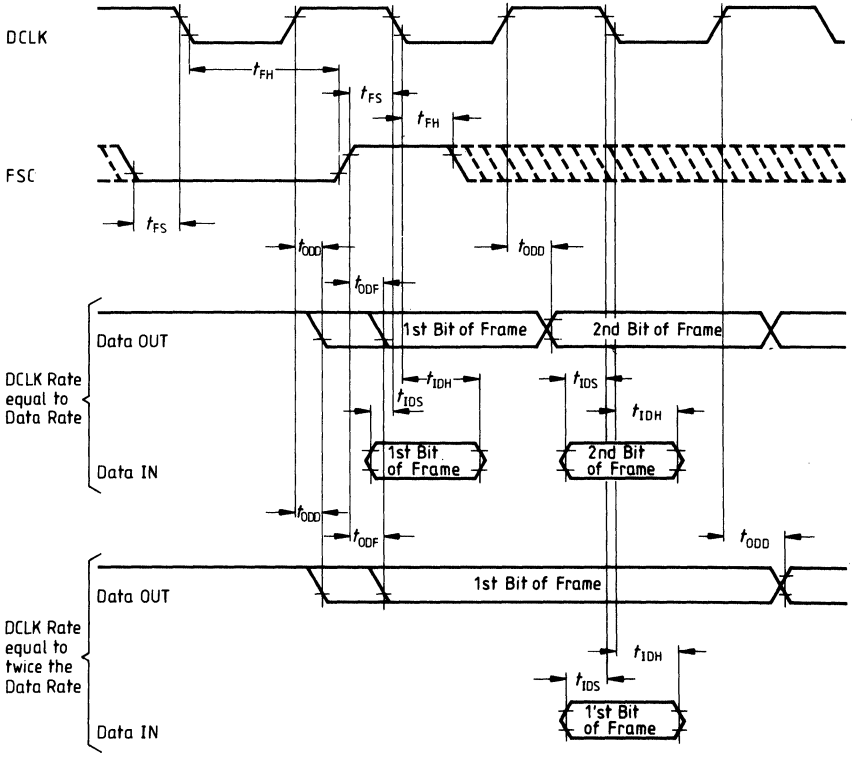
DCLK Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
DCL period	t_P	230 160			ns ns	single clock rate double clock rate
DCL high	t_{WH}	90 50			ns ns	single clock rate double clock rate
DCL low	t_{WL}	70			ns	

Input/Output Characteristics

FSC in Single Connection Modes and Quad Connection TS Mode.

FSC Timing Characteristics



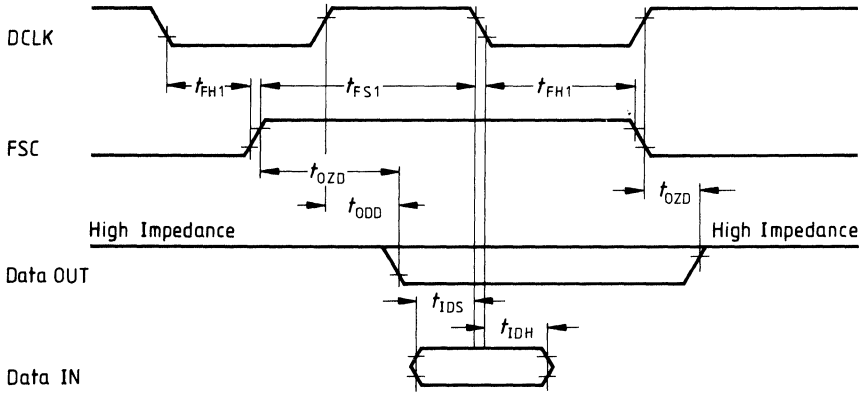
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
FSC set-up time	t_{FS}	60			ns
FSC hold time	t_{FH}	30			ns
Output data delay from DCLK	t_{ODD}			60	ns
Input data set-up	t_{IDS}	25			ns
Input data hold	t_{IDH}	20			ns
Output data delay from FSC*	t_{ODF}			150	ns

* This delay is applicable in two cases only:

1) When FSC appears for the first time, e.g. at system power-up.
2) When the number of bits in the PCM frame is not equal to either 256 or 512

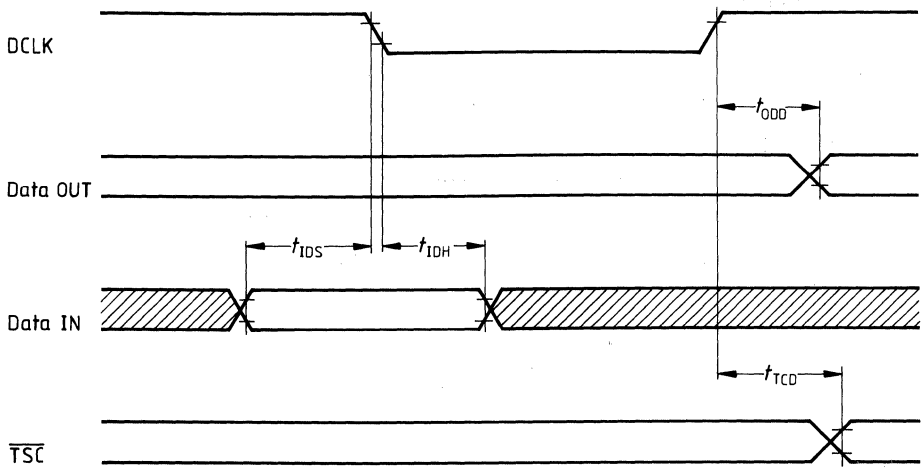
FSC in Quad Connection Common Control Mode

FSC (strobe) Characteristics



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
FSC set-up time	$t_{FS\,1}$	60			ns
FSC hold time	$t_{HF\,1}$	30			ns
Output data from high impedance to active	t_{OZD}			80	ns
Output data from active to high impedance	t_{ODZ}			40	ns
Output data delay from DCL	t_{ODD}			60	ns
Input data set-up	t_{IDS}	25			ns
Input data hold	t_{IDH}	20			ns

Data I/O Characteristics



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Output data delay from DCLK	t_{ODD}			60	ns
Input data set-up	t_{IDS}	25			ns
Input data hold	t_{IDH}	20			ns
TSC delay from DCLK	t_{TCD}			60	ns

Data OUT: SD0X in single connection modes
SD0X, SD1X, SD2X, SD3X in quad connection modes
SD1X, SD2X in master mode

Data IN: SD0R in single connection mode
SD0R, SD1X, SD2R, SD3R in quad connection modes

CDR in slave, multi-master and master modes

RES Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
RES high	t_{RWL}	4 x t_P			ns