ISDN Layer-1 Transceivers

S-Bus Interface Circuit (SBC)

General Description

The four-wire S-interface between subscriber terminals and network termination has been standardized by CCITT recommendation I.430. Making use of a passive bus which provides separate receiver and transmit loops operating at 192-kbit/s, up to eight terminals can be connected to the network termination. In case more than one terminal want to access the bus at the same time, a procedure is provided for resolving the collision problem. Since all layer-1 functions such as frame structure, data rate, power feeding, transceiver characteristics, activation/deactivation and subscriber access procedure are well defined, the S-bus can be considered an important tool for standardization of data communication equipment. It supports connections with a maximum length of 1 km in a point to-point and 150 m in a point-to-multipoint bus configuration.

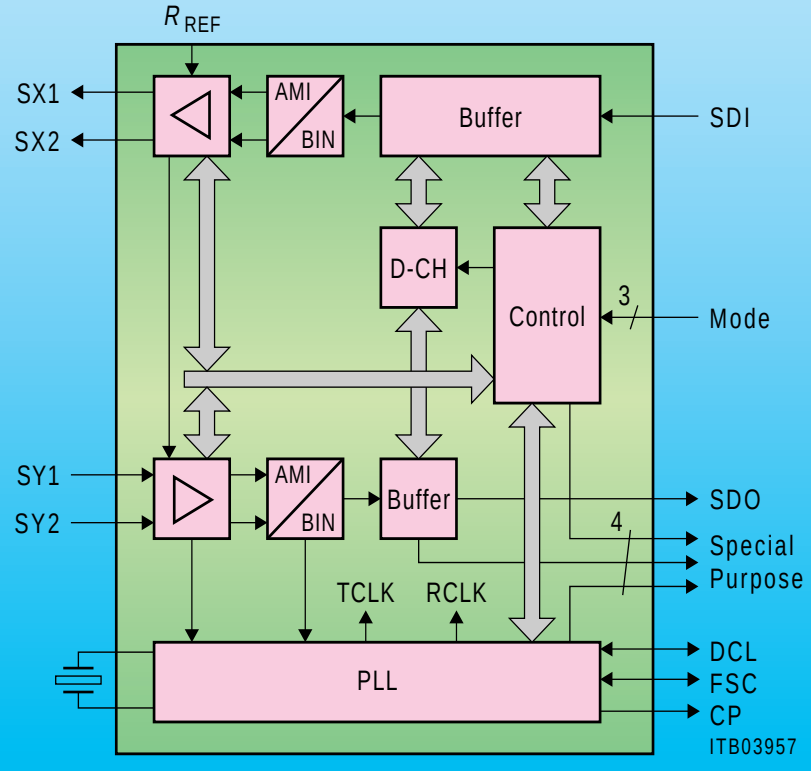
The SBC is designed to meet all CCITT requirements, and, moreover, implements additional features necessary in specific applications. The device contains the transceiver function, timing recovery for the different modes of operation, circuitry for the collision resolution function and a state control block to handle the activation/deactivation procedures autonomously without the support of a microprocessor. A flexible buffer structure performs the frame-alignment function in PBX-trunk applications, where the system clock deviates from the central office clock derived from the line. Matching of the actual line attenuation is supported by receiver circuitry which contains adaptively adjustable thresholds.

Type	Package
PEB 2080-N	P-LCC-28-1 (SMD)
PEB 2080-P	P-DIP-22-1 (not for new designs)
PEF 2080-N	P-LCC-28-1 (SMD)

Not for new development.
For new development use the SBCX (PEB 2081)

Features

- S-bus transceiver according to CCITT I.430
- Recovery of clock and frame signals in different modes of application.
- Frame alignment for trunk module application
- IOM interface compatible (IOM-1)
- Handling of command/indication information during the activation/deactivation procedure
- Switching of test loops
- Control of bus access by echo-bit handling
- Wake-up unit for activation from power-down state
- Several operating modes including trunk applications with frame alignment
- 2-µm CMOS technology and low power consumption:
  Standby: 4 mW
  Active: max. 60 mW at 512 kHz



Block Diagram