SIEMENS

ISDN Subscriber Access Controller (ISAC-S) PEB 2085

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2085-N	Q67100-H8399	PL-CC-44 (SMD)
PEB 2085-P	Q67100-H8401	P-DIP-40

The PEB 2085 ISAC™-S implements the four-wire S/T interface used to link voice/data terminals to an ISDN.

The PEB 2085 combines the functions of the S-Bus Interface Circuit (SBC: PEB 2080) and the ISDN Communications Controller (ICC: PEB 2070) on one chip.

The component switches B and D channels between the S/T and the ISDN Oriented Modular (IOM®) interfaces, the latter being a standard backplane interface for ISDN basic access.

The device provides all electrical and logical functions of the S/T interface, such as: activation/deactivation, mode dependent timing recovery and D-channel access and priority control.

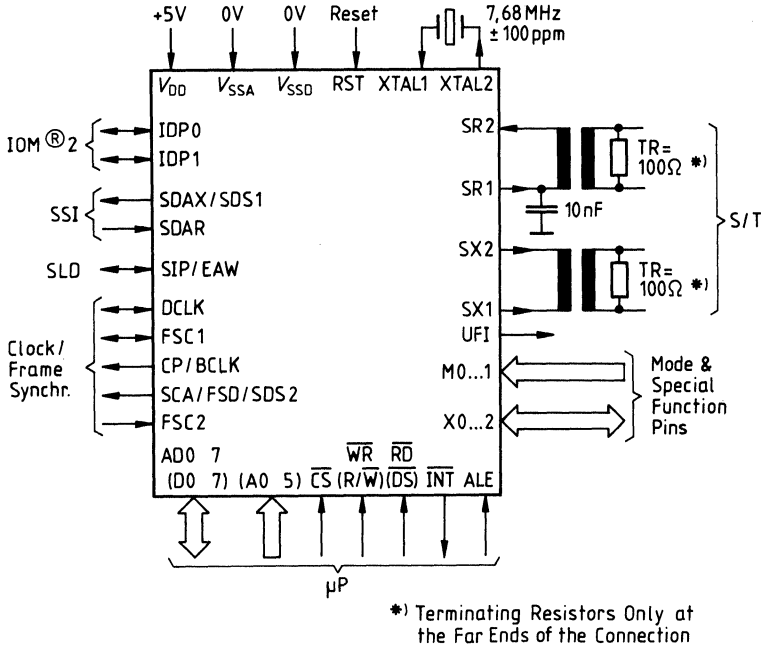
The HDLC packets of the ISDN D channel are handled by the ISAC-S which interfaces them to the associated microcontroller. In one of its operating modes the device offers high level support of layer-2 functions of the LAPD protocol.

The ISAC-S is a CMOS device, available in a P-DIP-40 or PL-CC-44 package. It operates from a single +5 V supply and features a power-down state with very low power consumption.

Features

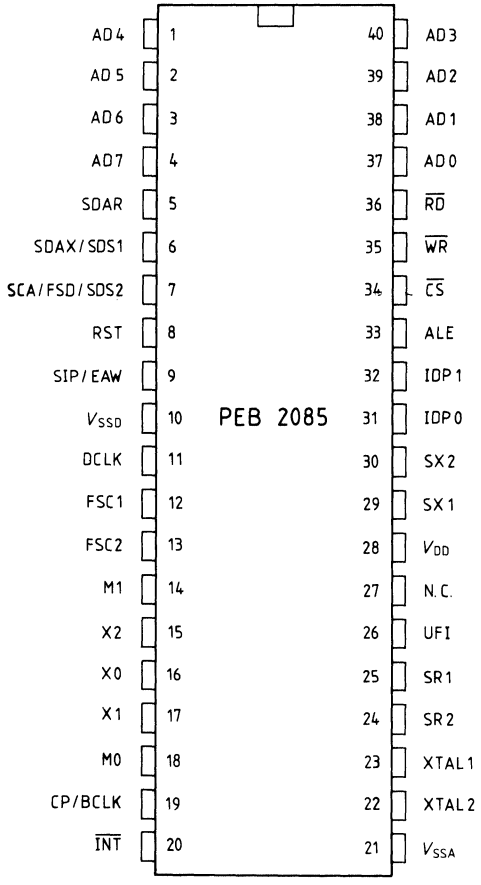
- Full duplex 2B + D S/T interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T interface and IOM
- Receive timing recovery according to selected operating mode
- D-channel access control
- Activation and deactivation procedures, with automatic wake-up from power-down state
- Access to S and Q bits of S/T interface
- Adaptively switched receive thresholds
- Frame alignment with absorption of phase wander in NT2 network side applications
- Support of LAPD protocol
- FIFO buffer (2x64 bytes) for efficient transfer of D-channel packets
- 8-bit microprocessor interface, multiplexed or non-multiplexed
- Serial interfaces: IOM-1, SLD, SSI
  IOM-2
- Implementation of IOM-1/IOM-2 monitor and C/I channel protocol to control peripheral devices
- µP access to B channels and intercommunication channels
- B-channel switching
- Watchdog timer
- Test loops
- Advanced CMOS technology
- Low power consumption

Figure 1
Logic Symbol

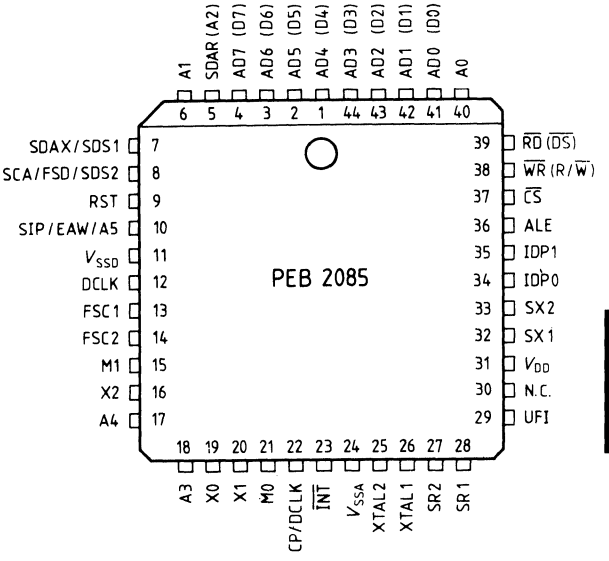


Pin Configuration
(top view)

P-DIP-40



PL-CC-44



Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin. No. PL-CC	Symbol	Input (I) Output (O)	Function
37 38 39 40 1 2 3 4	41 42 43 44 1 2 3 4	AD0/D0 AD1/D1 AD2/D2 AD3/D3 AD4/D4 AD5/D5 AD6/D6 AD7/D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Multiplexed Bus Mode:** Address/Data bus Transfers addresses from the µP system to the ISAC-S and data between the µP system and the ISAC-S. Non-multiplexed bus mode: Data bus. Transfers data between the µP system and the ISAC-S.
34	37	$\overline{CS}$	I	**Chip Select.** A "Low" on this selects the ISAC-S for a read/write operation.
–	36	R/$\overline{W}$	I	**Read/Write.** When "High", identifies a valid µP access as a read operation. When "Low", identifies a valid µP access as a write operation (Motorola bus mode).
35	36	$\overline{WR}$	I	**Write.** This signal indicates a write operation (Intel bus mode).
–	39	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
36	39	$\overline{RD}$	I	**Read.** This signal indicates a read operation (Intel bus mode).
20	23	$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the ISAC-S requests an interrupt. It is an open drain output.
33	36	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address bus (multiplexed bus type only).
10	11	V_{SSD}	–	Digital ground
21	24	V_{SSA}	–	Analog ground
28	31	V_{DD}	–	Power supply (5 V ± 5%)
23 22	26 25	XTAL1 XTAL2	I O	Connection for crystal or external clock input. Connection for external crystal. Left unconnected if external clock is used.
24 25	27 28	SR2 SR1	I O	**S Bus Receiver Input** **S Bus receiver Output** (2.5 V reference)
26	29	UFI	O	Connection for external pre-filter for S bus receiver, if used.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Functions
29 30	32 33	SX1 SX2	O O	**S Bus Transmitter** output (positive) **S Bus Transmitter** output (negative)
31 32	34 25	IDP0 IDP1	I/O I/O	**IOM Data Port 0, 1**
7	8	SCA	O	**Serial Clock Port A,** IOM-1 timing mode 0. A 128-kHz data clock signal for serial port A (SSI).
7	8	FSD	O	**Frame Sync Delayed,** IOM-1 timing mode 1. An 8-kHz synchronization signal, delayed by 1/8 of a frame, for IOM-1 is supplied. In this mode a minimal round trip delay for B1 and Bs channels is guaranteed.
7	8	SDS2	O	**Serial Data Strobe 2,** IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 takes on the function of SDS2 until a write access to SPCR is made.
8	9	RST	I/O	**Reset.** A "High" on this input forces the ISAC-S into reset state. The minimum pulse length is four clock periods. If the terminal specific functions are enabled. The ISAC-S may also supply a reset signal.
12	13	FSC1	I/O	**Frame Sync. 1** LT-S/NT/LT-T: input synchronization signal, IOM-1 and IOM-2 mode. TE: a programmable strobe output, selecting either one or two B channels on IOM-1 interface, IOM-1 mode. TE: frame sync output, "High" during channel 0 on IOM-2 interface, IOM-2 mode.
13	14	FSC2	I/O	**Frame Sync 2,** IOM-1 mode. LT-S/LT-T/NT: input synchronization signal TE: programmable strobe output, selecting either one or two B channels in IOM-1 interface.

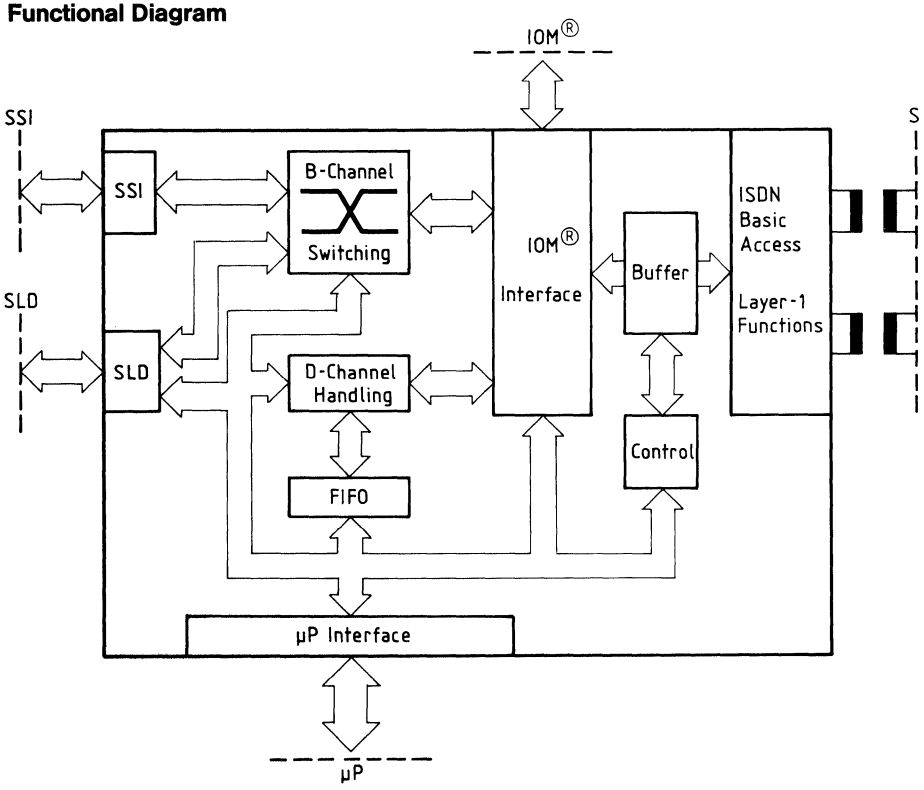
Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
11	12	DCLK	I/O	**Data Clock.** Clock of frequency equal to twice the data rate on the IOM interface. LT-S/LT-T: clock input 512-kHz IOM-1 mode max 4096-kHz IOM-2 mode TE: clock output 512-kHz IOM-1 mode 1536-kHz IOM-2 mode NT: clock input 512 kHz
–	40	A0	I	**Address Bit 0** (non-multiplexed bus type).
–	6	A1	I	**Address Bit 1** (non-multiplexed bus type).
– 5	5 5	A2 SDAR	I I	**Address Bit 2** (non-multiplexed bus type). **Serial Data Port A Receive.** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open-drain/ open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
–	18	A3	I	**Address Bit 3** (non-multiplexed bus type).
–	17	A4	I	**Address Bit 4** (non-multiplexed bus type).
– 9 9	10 10 10	A5 SIP EAW	I I/O I	**Address Bit 5** (non-multiplexed bus type). **SLD Interface Port,** IOM-1 mode. This line transmits and receives serial data at standard TTL or CMOS levels. **External Awake** (terminal specific function). If a falling edge on this input is detected, the ISAC-S generates an interrupt and, if enabled, a reset pulse.
6 6	7 7	SDAX SDS1	0 0	**Serial Data Port A Transmit,** IOM-1 mode. Transmit data is shifted out via this pin at standard TTL or CMOS levels. **Serial Data Strobe 1,** IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SDAX/SDS1 takes on the function of SDS1 until a write access to SPCR is made.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
14 18	15 21	M1 M0	I I	Setting of operating mode
15 17 16	16 20 19	X2 X1 X0	I/O I/O I	Mode specific function pins
19	22	CP	I/O	**Clock Pulses.** Special purpose pin, IOM-1 mode and IOM-2 (except TE) mode.
19	22	BCLK	O	**Bit Clock.** Clock of frequency 768 kHz, IOM-2 mode in TE.

Figure 2
Functional Diagram



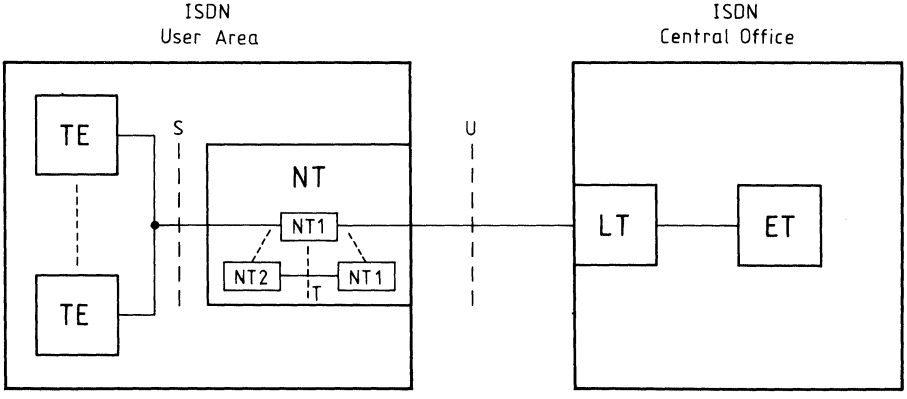
System Integration

ISDN Applications

The reference model for the ISDN basic access according to CCITT I series recommendations consists of

- an exchange and trunk line termination in the central office (ET, LT)
- a remote network termination in the user area (NT)
- a two-wire loop (U interface) between NT and LT
- a four-wire link (S interface) which connects subscriber terminals and the NT in the user area as depicted in **figure 3**.

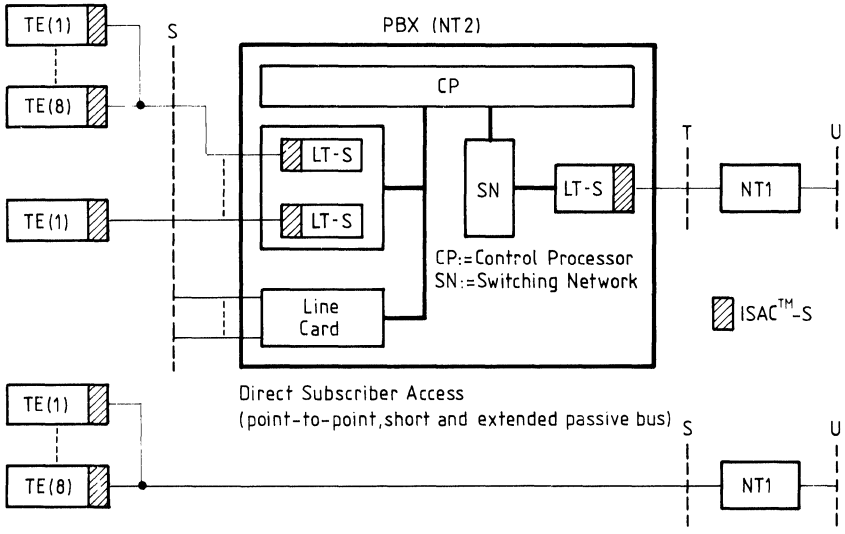
Figure 3
ISDN Basic Subscriber Access Architecture



The NT equipment serves as a converter between the U interface at the exchange and the S interface at the user premises. The NT may consist of either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. The NT1 is a direct transfomation between layer 1 of S and layer 1 of U. NT2 may include higher level functions like multiplexing and switching as in a PBX.

The ISAC-S designed for the user area of the ISDN basic access, especially for subscriber terminal equipment and for exchange equipment with S interfaces. **Figure 4** illustrates the general application of the ISAC-S.

Figure 4
Applications of ISAC-S (ISDN Basic Access)



Terminal Applications

The concept of the ISDN basic access is based on two circuit-switched 64 kbit/s B channels and a message oriented 16 kbit/s D channel for packetized data, signaling and telemetry information.

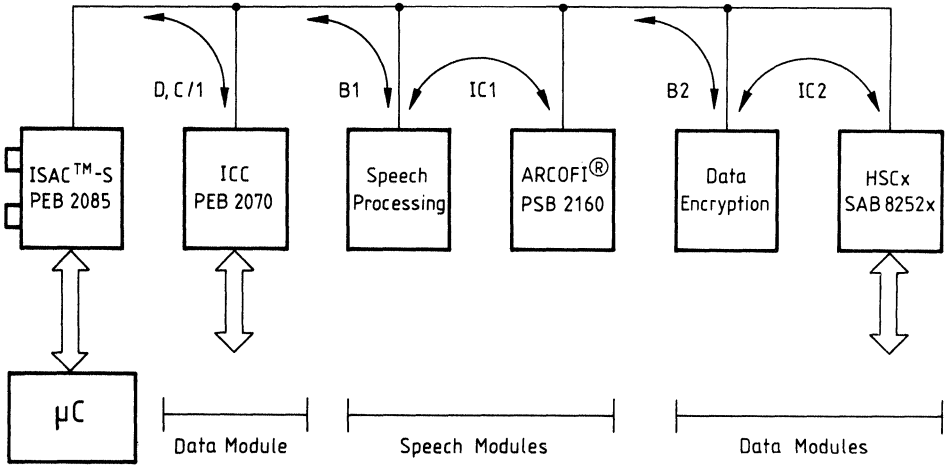
Figure 5 shows an example of an integrated multifunctional ISDN-S terminal using the ISAC-S. The ISAC-S provides the interface to the bus and separates the B and D channels.

The D channel, containing signaling data and packet switched data, is processed by the LAPD controller contained in the ISAC-S and routed via a parallel µP interface to the terminal processor. The high level support of the LAPD protocol is implemented by the ISAC-S allows the use of a low cost processor in cost sensitive applications.

The IOM interface generated by the ISAC-S is used to connect diverse voice/data application modules:

- sources/sinks for the D channel
- sources/sinks for the B1 and B2 channels.

Figure 5
Example of ISDN-S Voice/Data Terminal



Up to eight D channel components (ICC: ISDN Communication Controller PEB 2070) may be connected to the D and C/I (Command/Indication) channels. The ISAC-S and ICC handle contention autonomously.

Data transfers between the ISAC-S and the voice/data modules are done with the help of the IOM monitor channel protocol. Each V/D module can be accessed by an individual address. The same protocol enables the control of IOM terminal modules and the programming of intercommunication inside the terminal. Two intercommunication channels IC1 and IC2 allow a 2 x 64 kbit/s transfer rate between voice/data modules.

In the example above **(figure 5)**, one ICC is used for data packets in the D channel. A voice processor is connected to a programmable digital signal processing codec filter via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication, B2 for data communication.

The ISAC-S ensures full upward compatibility with IOM-1 devices. It provides the additional strobe, clock and data lines for connecting standard combos or data devices via IOM, or serial SLD and SSI interfaces. The strobe signals and the switching of B channels is programmable. **Figure 6** shows the implementation of a basic ISDN feature telephone using the ISAC-S and the Audio Ringing Codec Filter (ARCOFI®: PSB 2160).

Line Card Applications

An example of the use of the ISAC-S on an ISDN PBX line card (decentralized architecture) is shown in **figure 7**.

The ISAC-S is connected to an Extended PCM Interface Controller (EPIC PEB 2055) via an IOM interface.

This interface carries the control and data for up to eight subscribers using time division multiplexing. The ISAC-S's are connected in parallel on IOM (IDP0 output; IDP1, DCLK, FSC1 as inputs), one ISAC-S per subscriber.

The EPIC performs dynamic B and D channel assignment on the PCM highways. Since this component supports four IOM interfaces, up to 32 subscribers may be accomodated.

Microprocessor Environment

The ISAC-S is especially suitable for cost-sensitive applications with single-chip microcontrollers (e. g. 8048, 8031, 8051). However, due to its programmable micro interface and non-critical bus timing, it fits perfectly into almost any 8-bit microprocessor system environment. The microcontroller interface can be selected to be either of the Motorola type (with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$), of the Siemens/Intel non-multiplexed bus type (with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$) or of the Siemens/Intel multiplexed address/data bus type ($\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE).

Figure 6
Basic ISDN Feature Telephone

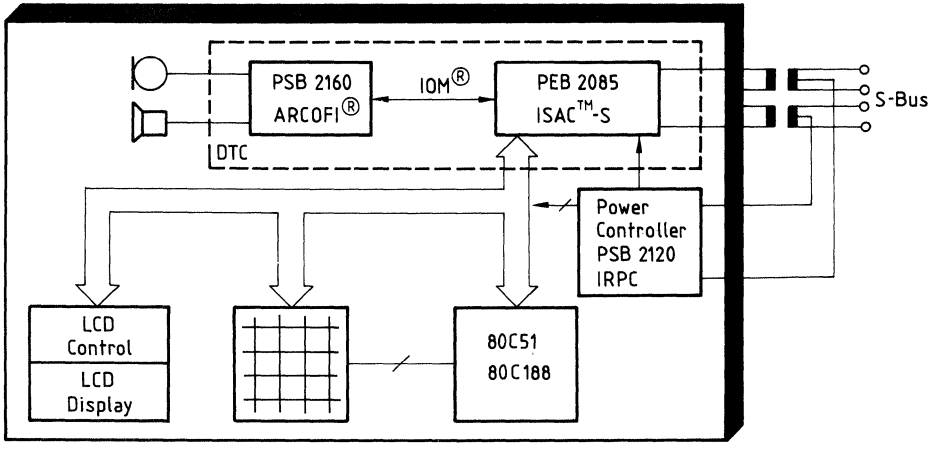


Figure 7
ISDN PBX Line Card Implementation

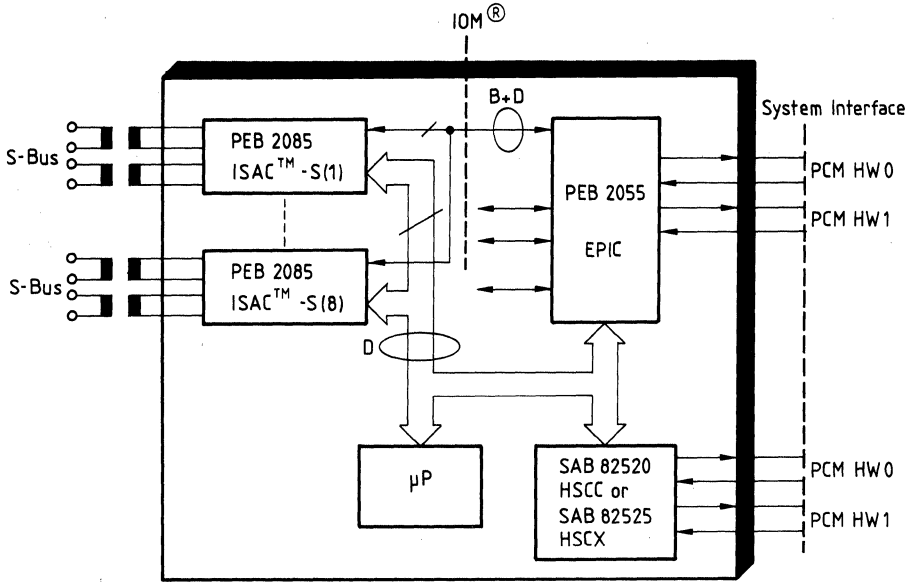
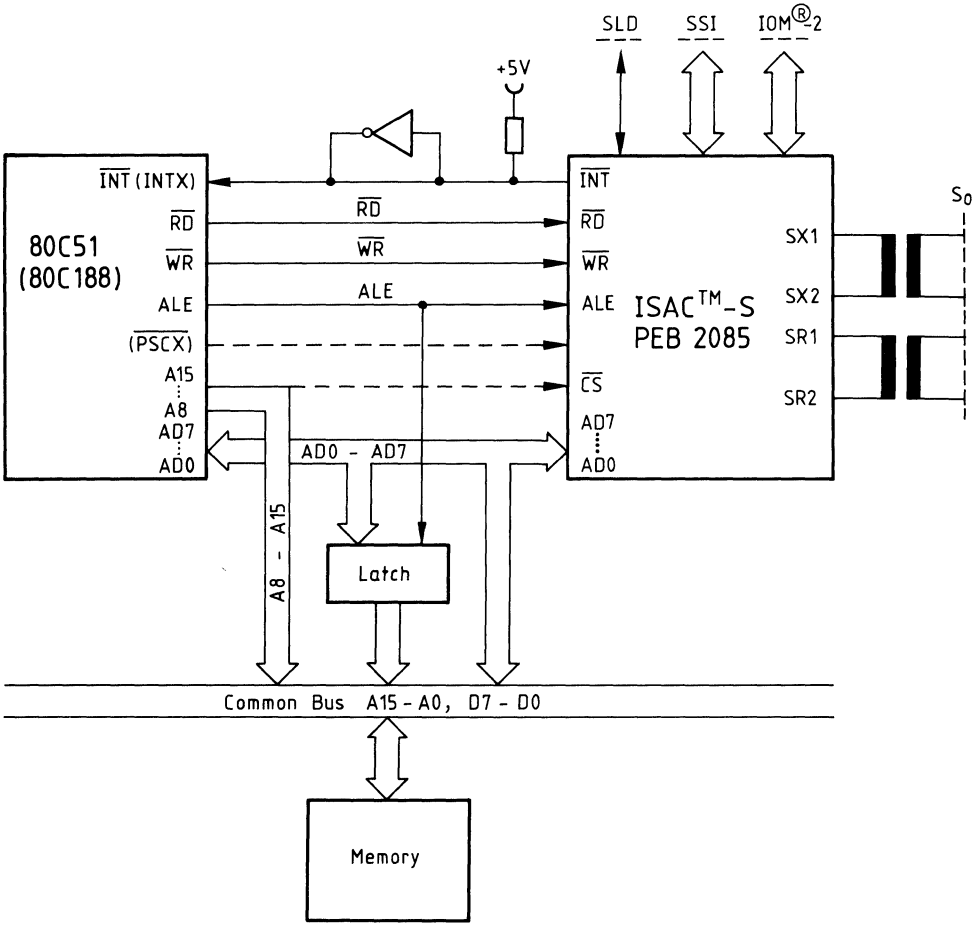


Figure 8


SLD
SSI
IOM®-2
+5V
INT (INTX)
RD
WR
ALE
(PSCX)
A15
A8
AD7
AD0
80C51
(80C188)
INT
RD
WR
ALE
CS
AD7
AD0
ISAC™-S
PEB 2085
SX1
SX2
SR1
SR2
S0
AD0 - AD7
A8 - A15
Latch
Common Bus A15 - A0, D7 - D0
Memory

Functional Description

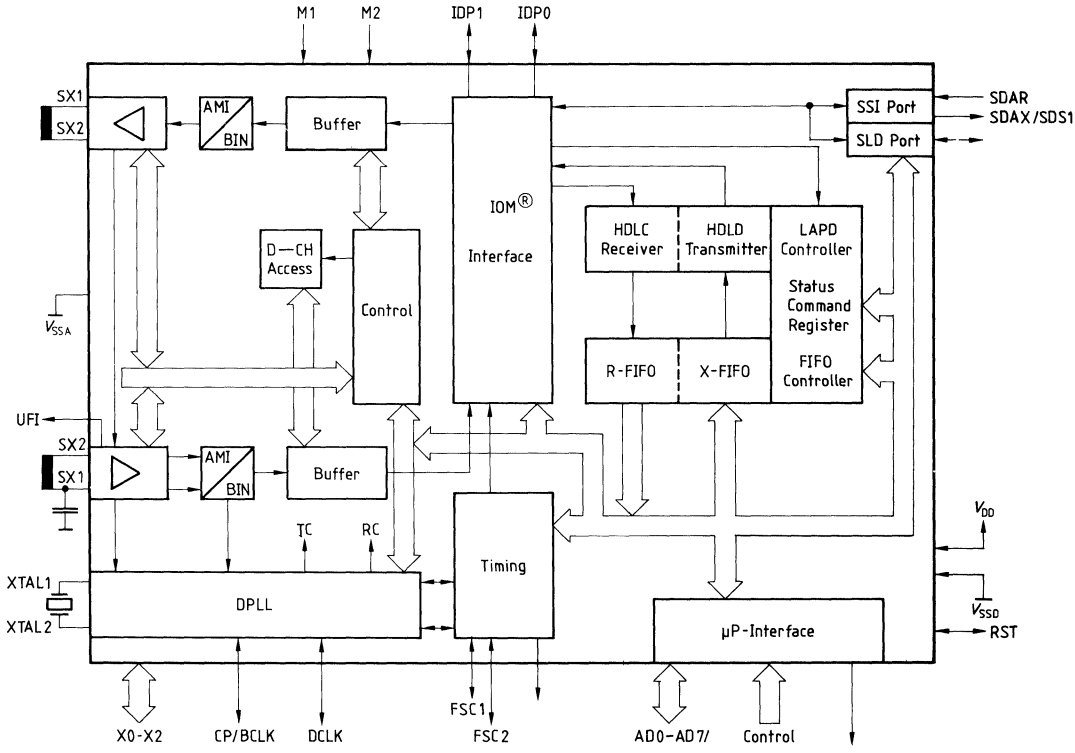
General Functions and Device Architecture

The functional block diagram of the ISAC-S is shown in **figure 9**.

The left-hand side of the diagram contains the layer-1 functions, according to CCITT I series recommendations:

- S-bus transmitter and receiver
- riming recovery and synchronization by means of digital PLL circuitry
- activation/deactivation
- access to S and Q channels
- handling of D channel
- test loops
- send single/continuous AMI pulses (diagnostics).

Figure 9
Architecture of the ISAC-S



The right-hand side consists of:

- the serial interface logic for the IOM and the SLD and SSI interfaces, with B channel switching capabilities
- the logic necessary to handle the D-channel messages (layer 2).

The latter consists of an HDLC receiver and an HDLC transmitter together with 64-byte deep FIFO's for efficient transfer of the messages to/from the user's CPU.

In a special HDLC controller operating mode, the auto mode, the ISAC-S processes protocol handshakes (I- and S-frames) of the LAPD (Link Access Procedure on the D channel) autonomously.

Control and monitor functions as well as data transfers between the user's CPU and the D and B channels are performed by the 8-bit parallel µP interface logic.

The IOM interface allows interaction between layer-1 and layer-2 functions. It implements D-channel collision resolution for connecting other layer-2 devices to the IOM interface, and the C/I and monitor channel protocols (IOM-1/IOM-2) to control peripheral devices.

The timing unit is responsible for the system clock and frame synchronization.

Interface Modes

Two basic modes are distinguished, according to whether the ISAC-S is programmed to operate with IOM-1 or with IOM-2 interface. This programming is performed via bit IMS in ADF2 register.

IOM-1 Interface Mode (IMS = 0)

The ISAC-S is configurable for the following applications:

- ISDN Terminals → TE Mode
- ISDN subscriber line termination → LT-S mode
- ISDN trunk line termination (PBX connection to Central Office) → LT-T mode
- ISDN network termination → NT mode

Configuration is performed by pin-strapping (pins M1, M0), yielding different meanings to the multifunctional pins (X0, X1, X2) as well as the clock and framing signal pins (DCLK, FSC1, FSC2, CP) **see table 1**.

Table 1
Operating Modes and Functions of Mode Specific Pins of ISAC-S PEB 2085 (IOM-1)

Application	M1	M0	DCLK	FSC1/2	CP	X2	X1	X0
TE	0	0	o: 512 kHz*	o: 8 kHz*	o: 1536 kHz*	o: ECHO	o: 3840 kHz	I: CON
LT-S	1	0	i: 512 kHz	i: 8 kHz	i: fixed at 0	i: fixed at 0	o: 7680 kHz	i: fixed at 0
LT-T	0	1	i: 512 kHz	i: 8 kHz	o: 512 kHz*	i: fixed	i: fixed at 0	I: CON
NT	1	1	i: 512 kHz	i: 8 kHz	i: $\overline{SCZ}$	i: $\overline{SSZ}$	i: fixed at 0	–

* synchronized to S i: input o: output

ECHO Reproduces the E-bits received from the S interface synchronously to IOM frame "D"-bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary 1.

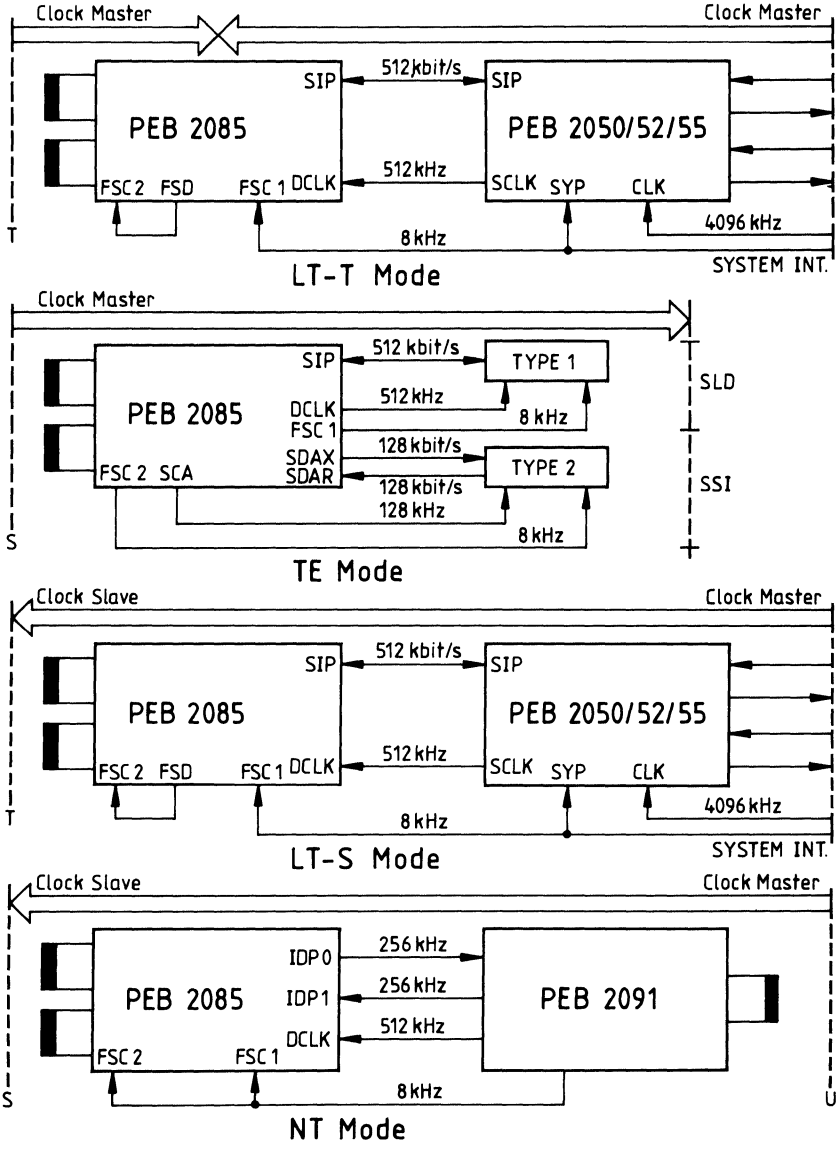
CON Connected to S bus.

$\overline{SCZ}$ Send continuous binary zeros (96 kHz)

$\overline{SSZ}$ Send single binary zeros (2 kHz)

Figure 10
Operating Modes of ISAC-S (IOM-1)

The different operating modes in relation to the timing recovery are illustrated in **figure 10.**



IOM-2 Interface Mode (IMS = 1)

In this mode the IOM interface has the enhanced functionally of IOM-2. Moreover, the auxiliary serial SSI and SLD interfaces are not longer available (as in IOM-1 mode), since they are functionally replaced by the general purpose IOM-2 interface.

Table 2

Operating Modes and Functions of Mode Specific Pins of ISAC-S PEB 2085 (IOM-2)

Application	M1	M0	DCLK	FSC1	CP/BCLK	X2	X1	X0
TE	0	0	o: 1536 kHz*	o: 8 kHz*	o: 768 kHz*	o: ECHO	o: 3840 kHz	i: CON
LT-S	1	0	i: 4096 kHz	i: 8 kHz	i: fixed at 0	i: fixed at 0	o: 7680 kHz	i: fixed at 0
LT-T	0	1	i: 4096 kHz	i: 8 kHz	o: 512 kHz*	i: fixed at 0	i: fixed at 0	i: CON
NT	1	1	i: 512 kHz	i: 8 kHz	i: SCZ	i: $\overline{SSZ}$	i: fixed at 0	–

* synchronized to S i: input o: output

ECHO: Reproduces the E-bits received from the S interface synchronously to IOM frame "D"-bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary 1.

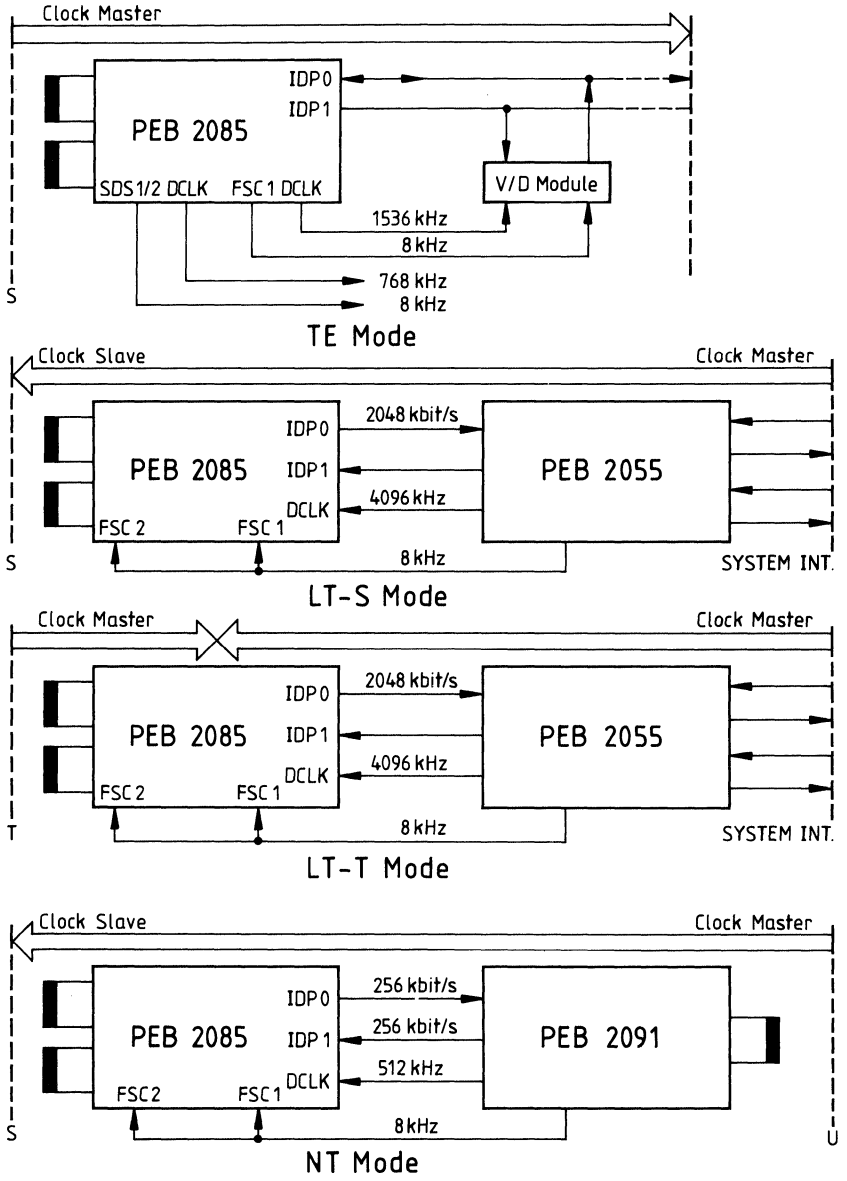
CON Connected to S bus.

$\overline{SCZ}$ Send continuous binary zeros (96 kHz)

$\overline{SSZ}$ Send single binary zeros (2 kHz)

Figure 11
Operating Modes of ISAC-S (IOM-2)

The different operating modes in relation to the timing recovery are illustrated in **figure 11.**



Interfaces

The ISAC-S serves three different user-oriented interface types:

- parallel processor interface to higher layer functions
- IOM interface: between layer 1 and layer 2, and as a universal backplane for terminals
- SSI and SLD interfaces for B channel sources and destinations (in IOM-1 mode only).

µP Interface

The ISAC-S is programmed via an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 (18) lines and is directly compatible with multiplexed and non-multiplexed microcontroller interfaces (Intel or Motorola type buses). The microprocessor interface signals are summarized in **table 3.**

Table 3

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
37	41	AD0/D0	I/O	**Multiplexed Bus Mode: Address/Data Bus.**
38	42	AD1/D1	I/O	Transfers addresses from the µP system to
39	43	AD2/D2	I/O	the ISAC-S and data between the µP system
40	44	AD3/D3	I/O	and the ISAC-S.
1	1	AD4/D4	I/O	**Non-Multiplexed Bus Mode: Data Bus.**
2	2	AD5/D5	I/O	Transfers data between the µP system and
3	3	AD6/D6	I/O	the ISAC-S.
4	4	AD7/D7	I/O	
34	37	$\overline{CS}$	I	**Chip Select.** A 0 ("low") on this line selects the ISAC-S for a read/write operation.
–	36	R/$\overline{W}$	I	**Read/Write.** At 1 ("high"), identifies a valid µP access as a read operation. At 0, identifies a valid µP access as a write operation (Motorola bus mode).
35	36	$\overline{WR}$	I	**Write.** This signal indicates a write operation (Intel bus mode).
–	39	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
36	39	$\overline{RD}$	I	**Read.** This signal indicates a read operation (Intel bus mode).

Table 3 (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
20	23	$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the ISAC-S requests an interrupt. It is an open drain output.
33	36	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address bus (Multiplexed bus type only).
–	40	A0	I	Address bit 0 (non-multiplexed bus type).
–	6	A1	I	Address bit 1 (non-multiplexed bus type).
–	5	A2	I	Address bit 2 (non-multiplexed bus type).
–	18	A3	I	Address bit 3 (non-multiplexed bus type).
–	17	A4	I	Address bit 4 (non-multiplexed bus type).
–	10	A5	I	Address bit 5 (non-multiplexed bus type).

ISDN Oriented Modular (IOM) Interface

IOM-1

This interface consists of one data line per direction (IOM Data Ports 0 and 1: IDP0,1). Two additional signals define the data clock (DCLK) and the frame synchronization (FSC1/2) at this interface. The data clock has a frequency of 512 kHz (twice the data rate) and the frame sync clock has a repetition rate of 8 kHz.

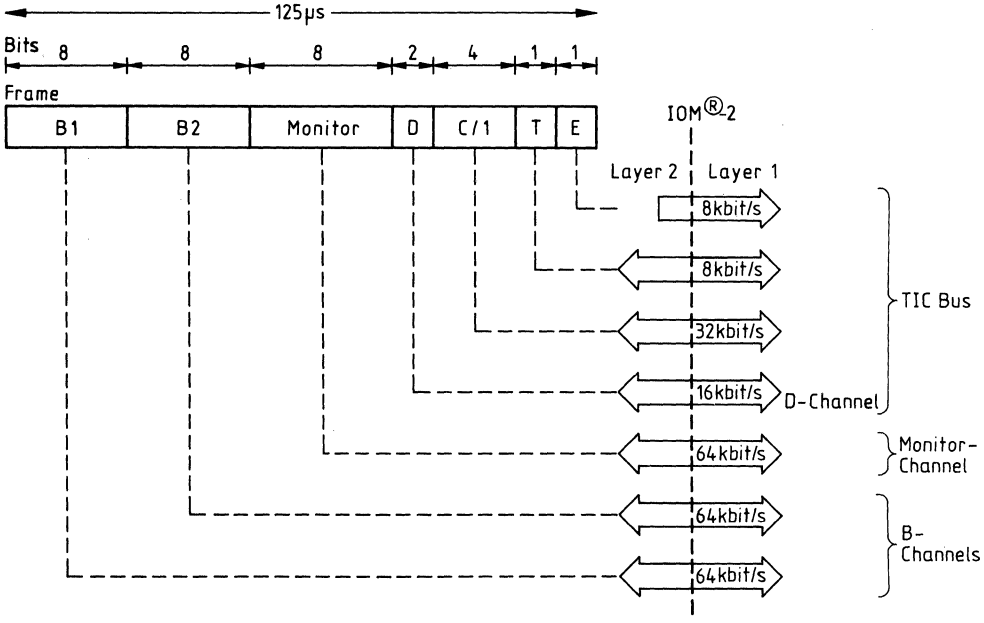
Via this interface four octets are transmitted per 125 µs frame **(figure 12)**. The first two octets constitute the two 64 kbit/s B channels. In the ISAC-S the monitor channel (third octet) serves:

- for arbitration of the access to IOM-TIC bus on IPD1 in case several layer-2 components are connected together **(figure 14)**.
- to indicate the status on the S bus D channel (IDP0, bit 3 of the monitor octet), "stop/go"
- for the exchange of data using the IOM-1 monitor channel protocol which involves the E bit as data validation bit.

Two bits in the fourth octet are used for the 16 bit/s D channel. The controling and monitoring of layer-1 functions (activation/deactivation of the S interface...) is done via the command/indication bits. The T bis is not used in ISAC-S IOM-1 applications.

The last octet in the IOM frame is called the Telecom IC bus (TIC) because of the offered busing capability.

Figure 12
IOM-1 Frame Structure



IOM-1 Timing

In TE mode the IOM timing is internally generated by DPLL circuitry from the S interface and DCLK and FSC 1/2 are outputs.

In LT-S, NT and LT-T modes the clock and frame synchronization signals are inputs.

The IOM interface can be operated either in timing mode 0 or in timing mode 1, selected by SPM bit in SPCR register.

Timing mode 0 **(SPM = 0)** must be programmed when ISAC-S is in TE mode.

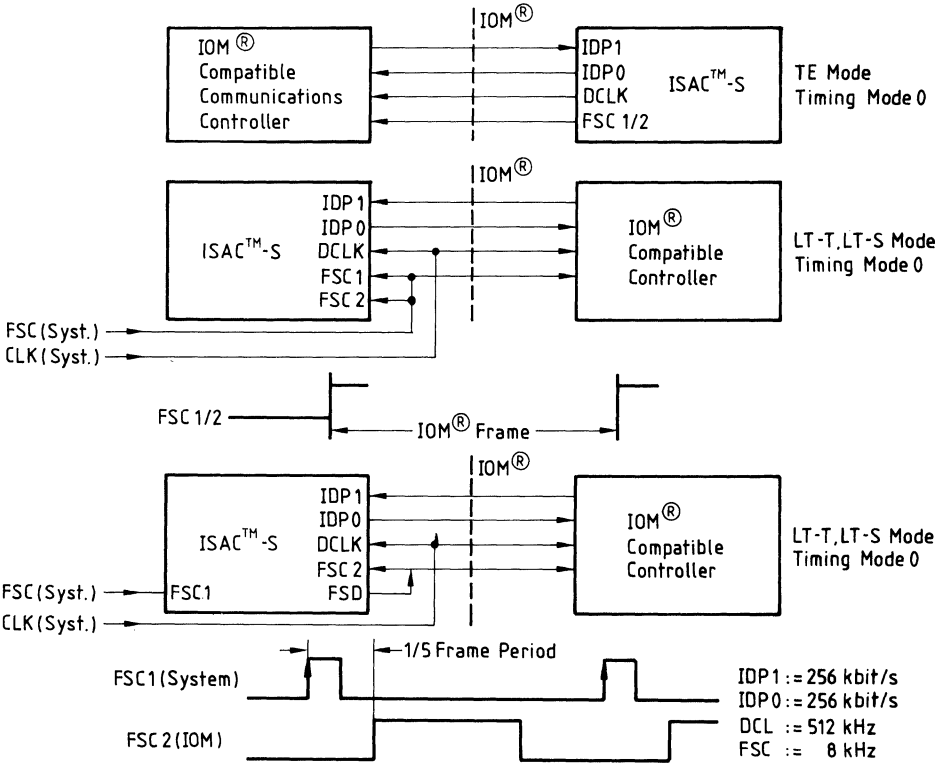
Timing mode 1 **(SPM = 1)** is only meaningful in exchange applications (LT-S, LT-T) when the SLD is used.

In timing mode 0 FSC1 and FSC2 should be connected to one another for correct operation (when FSC1/2 are input, i.e. in non-TE modes).

In timing mode 1 the IOM is synchronized by a frame signal FSD delayed in time with respect to the frame sync pulse input via FSC1. This reduces the B channel round-trip delay time when the SLD is used **(figure 13)**.

For correct operation in timing mode 1, the output FSD should be connected to FSC2 input **(see figure 10)**.

Figure 13
IOM-1 Interface Signals



The IOM interface has two different clocking states:

- Idle state → FSC1/2 and DCLK are disabled and both data lines are "High" (Power Down)
- Clocked state → FSC1/2 and DCLK are enabled (Stand By).

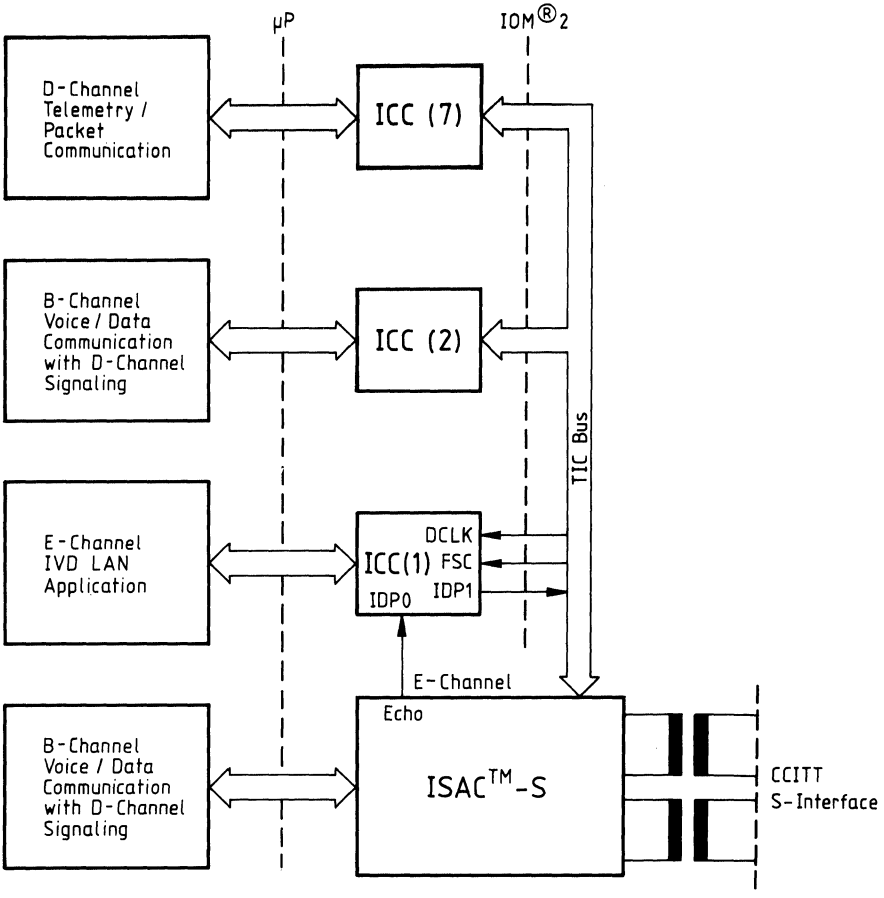
Unlike in digital exchange configurations, in which the IOM interface always remains in the synchronized state, in terminal equipment both clocking states can be selected.

The idle state is reached if the CFS (Configuration Select) bit in register SQXR is set to "1" and the S/T interface is inactive.

The transition from idle state to clocked state will be automatically initiated by an incoming call from network side. An activation of the IOM interface from the subscriber end has to be programmed by setting and resetting the SPU (Software Power Up) bit in the SPCR register, before the IOM interface can be used (e.g. for the activation/deactivation procedure at the S interface.

The arbitration mechanism implemented in the monitor channel of the IOM allows the access of external communication controllers (up to 7) to the layer-1 functions provided in the ISAC-S and to the D channel. (TIC bus; **see figure 14)**. To this effect the outputs of the controllers (ICC:ISDN Communication Controller 2070) are wired-or-ed and connected to pin IDP1, a pull-up resistor being already provided in the ISAC-S. The inputs of the ICCs are connected to pin IDP0.

Figure 14
Applications of IOM Bus Configuration



IOM-2

The IOM-2 is a generalisation and enhancement of the IOM-1. While the basic frame structure is very similar, IOM-2 offers further capacity for the transfer of maintenance information. In terminal applications, the IOM-2 constitutes a powerful backplane bus offering inter-communication and sophisticated control capabilities for peripheral modules.

Figure 15
Channel Structure of IOM-2

B1	B2	Monitor	D	C/I	MR	MX

- The 64 kbit/s channels, B1 and B2, are conveyed in the first two octets.
- The third octet (monitor channel) is used for transferring maintenance information between the layer-1 functional blocks (SBC, IBC, IEC) and the layer-2 controller.
- The fourth octet (control channel) contains
  - two bits for the 16 kbit/s D channel
  - four command/indication bits for controlling activation/deactivation and for additional control functions
  - two bits MR and MX for supporting the handling of the monitor channel.

In the case of an IOM-2 interface the frame structure depends on whether TE- or non-TE mode is selected, via bit SPM in SPCR register.

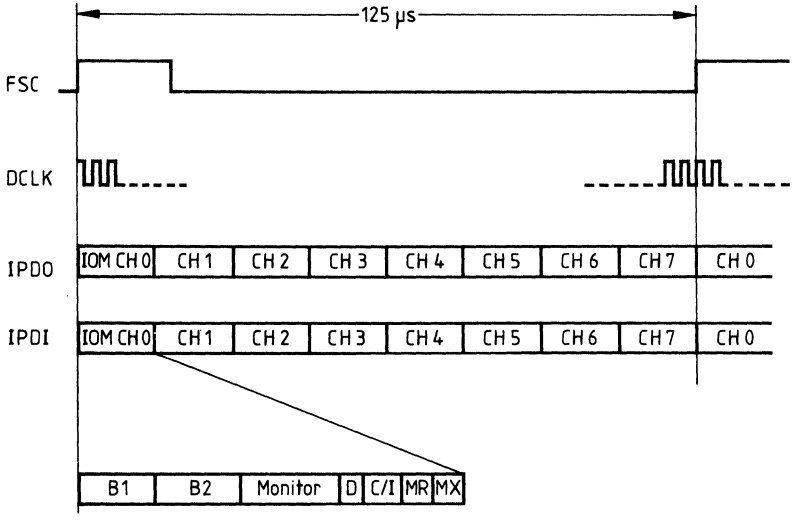
Non-TE Timing Mode (SPM = 1)

This mode is used in LT-S and LT-T applications. The frame is a multiplex of eight IOM-2 channels **(figure 16)**, each channel has the structure in **figure 15**.

Thus the data rate per subscriber connection (corresponding to one channel) is 256 kbit/s, whereas the bit rate is 2048 kbit/s. The IOM-2 interface signals are:

IDP0,1: 2048 kbit/s
DCLK: 4096 kHz input
FSC1: 8 kHz input

Figure 16
Multiplexed Frame Structure of the IOM-2 Interface in Non-TE Timing Mode



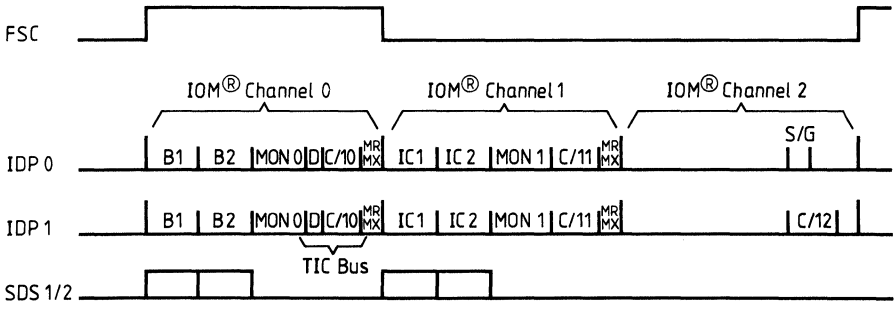
The ISAC-S is assigned to one of the eight channels (0 to 7) via register programming.

The Timing Mode (SPM = 0)

The frame is composed of three channels **(figure 17)**:

- Channel 0 contains 144 kbit/s (for 2B + D) plus monitor and command/indication channels for the layer-1 device.
- Channel 1 contains two 64 kbit/s intercommunication channels plus monitor and command/indication channels for other IOM-2 devices.
- Channel 2 is used for IOM bus arbitration (access to the TIC bus).

Figure 17
Definition of IOM-2 Channels in Terminal Mode



The IOM-2 signals are:

IDP0,1:	768 kbit/s	
DCLK:	1536 kHz	output
FSC1:	8 kHz	output.

In addition, to support standard combos/data devices the following signals are generated as outputs:

BCLK:	768 kHz	bit clock
SDS1/2:	8 kHz	programmable data strobe signals for selecting one or both B/IC channel(s).

The clocking states (idle/clocked) are identical to the IOM-1 case and are controlled in the same manner via bits CFS and SPU.

Important Note: If the ISAC-S is configured in NT mode, the IOM frame structure is identical to that of the IOM-1 case.

SSI (Serial Port A)

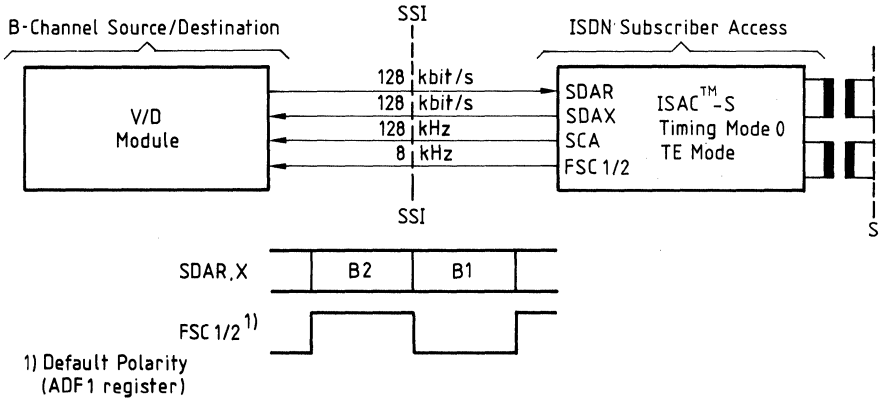
The SSI (Serial Synchronous Interface) is available in IOM-1 interface mode. Timing mode 0 (SPM = 0) and TE operation has to be programmed.

The serial port SSI serves as a full duplex connection to B- channel sources/destinations in terminal equipment with a data rate of 128 kbit/s.

It consists of one data line in each direction (SDAX and SDAR), an 8-kHz strobe output (FSC1 and/or FSC2) and the 128-kHz clock output (SDA).

Figure 18

Connection of B-Channel Sources/Destinations to the ISAC-S via SSI



This serial interface allows the connection of voice/data modules, such as serial synchronous transceiver devices (USART's, ICC PEB 2070, HSCX SAB 82525, ITAC PSB 2110,...) and various codec filters directly to the ISAC-S, as illustrated in **figure 18**.

By programming the ADF1 register it is possible to independently set the strobe signal FSC1/2 polarities so that either B1 or B2 is selected by the V/D module.

The µC system has access to B-channel data via the ISAC-S registers BCR1/2 and BCX1/2.

The µC access must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR).

SLD

The SLD is available in IOM-1 interface mode.

The standard SLD interface is a three-wire interface with a 512-kHz clock (DCLK), an 8-kHz frame direction signal (TE mode: FSC1/2 output; LT-S/LT-T modes: FSC1 sync input), and a serial ping-pong data lead (SIP) with an effective full duplex data rate of 256 kbit/s.

The frame is composed of four octets per direction. Octets 1 and 2 contain the two B channels, octet 3 is a feature control byte, and octet 4 is a signaling byte **(figure 19)**.

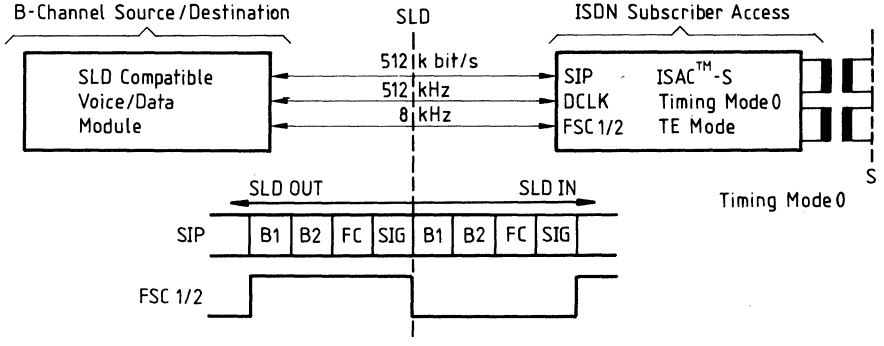
The SLD interface can be used in:

– **Terminal applications** (TE) as a full duplex time-multiplexed (ping-pong) connection to B-channel sources/destinations.

  Codec filters, such as the SICOFI (PEB 2060) or the ARCOFI (PSB 2160) as well as other SLD compatible voice/data modules may be connected directly to the ISAC-S as depicted in **figure 19.** In TE applications timing mode 0 has to be programmed, hence SLD operates in master mode. Moreover, terminal specific functions have to be deselected (TSF = 0).

Figure 19

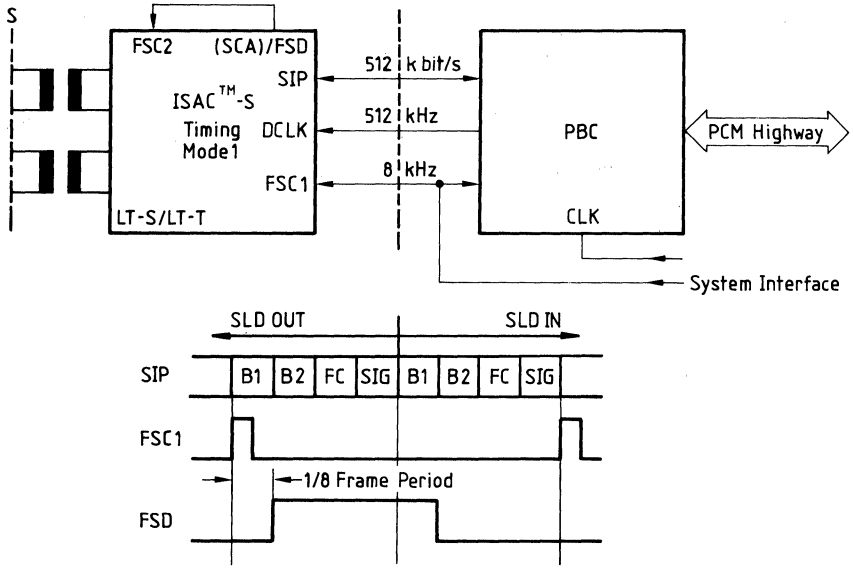
Connection of B-Channel Destinations to the ISAC-S via SLD



– **Digital exchange applications** (LT-S/LT-T) as a full duplex time-multiplexed connection to convey the B channels between the S/T interface and a Peripheral Board Controller (e.g. PBC PEB 2050 or PIC PEB 2052), which performs time-slot assignment on the PCM highways, forming a system interface to a switching network **(figure 20)**.

Timing mode 1 (SPM = 1) has to be programmed, hence SLD operates in slave mode.

Figure 20
Connection of the ISAC-S as B-Channel Source/Destination to a Peripheral Board Controller via SLD



The µC system has access to B-channel data, the feature control byte and the signaling byte via the ISAC-S registers:

– C1R, C2R → B1/B2
– MOR1 and MOR2 → FC
– CIR1 and CIR1 → SIG

The µP access to C1R, C2R, MOR1/MOX1, CIR1 and CIX1 must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR) and the BVS-bit (STAR).

Individual Functions

Layer-1 Functions for the ISDN Basic Access

The common functions in all operating modes are:

- line transceiver functions for the S/T interface according to the electrical specifications of CCITT I.430;
- conversion of the frame structure between IOM and S/T interface;
- conversion from/to binary to/from pseudo-ternary code;
- level detect.

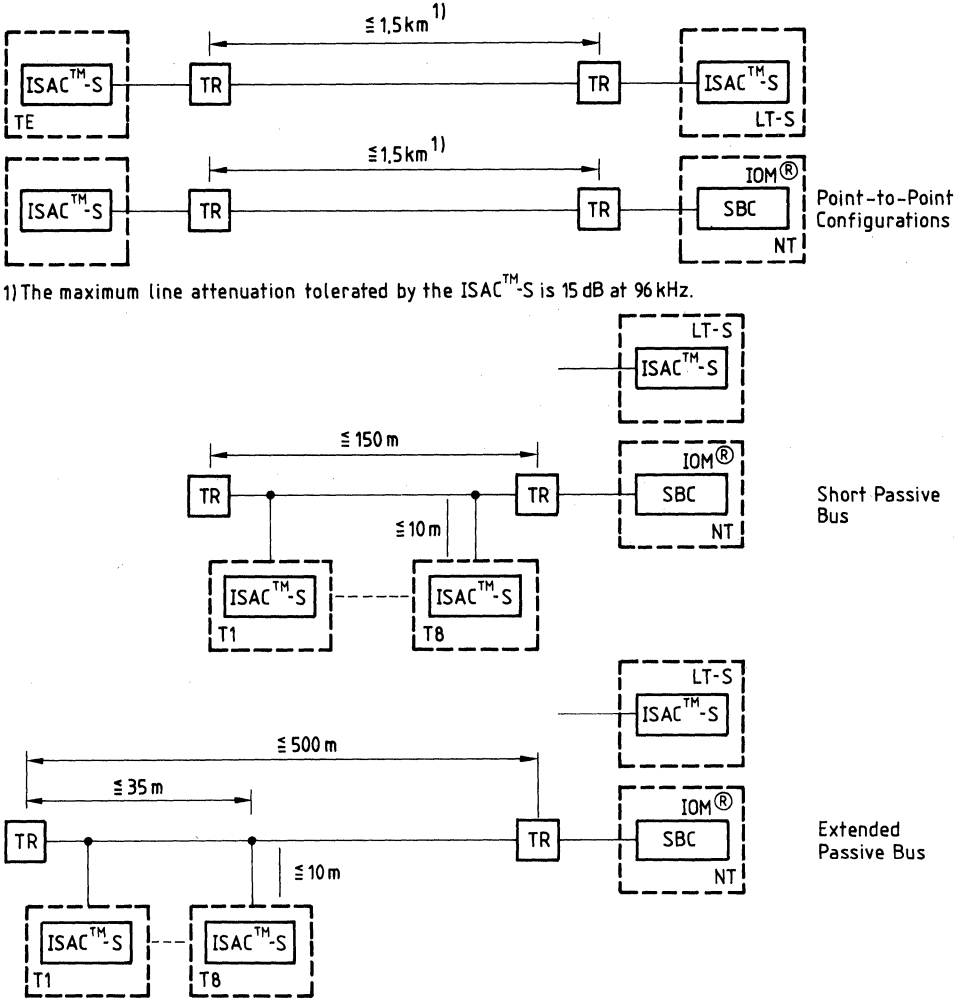
Mode specific functions are:

- receive timing recovery for point-to-point, passive bus and extended passive bus configuration;
- S/T timing generation using IOM timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation by handling of the global echo bit;
- activation/deactivation procedures, triggered by primitives received over the IOM C/I channel or by INFO's received from the line;
- frame alignment according to CCITT Q.503;
- execution of test loops.

For a block diagram, **see figure 9**.

The wiring configurations in user premises, in which the ISAC-S can be used are illustrated in **figure 21**.

Figure 21
Wiring Configurations in User Premises



1) The maximum line attenuation tolerated by the ISAC™-S is 15 dB at 96 kHz.

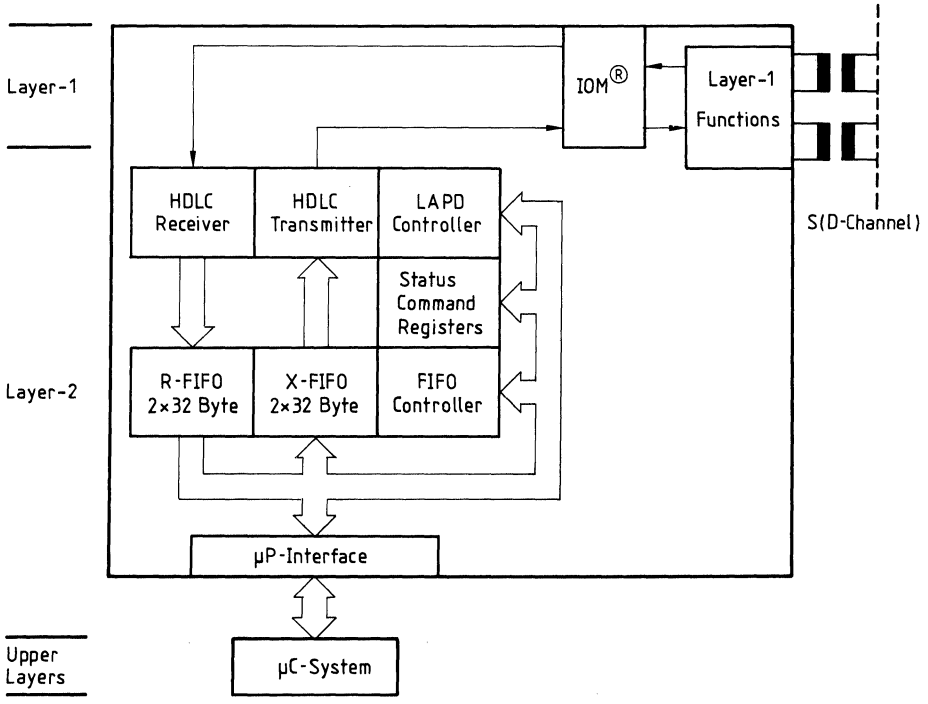
Layer-2 Functions for the ISDN Basic Access

LAPD, layer 2 of the D-channel protocol (CCITT .441) includes functions for:

- Provision of one or more data link connections on a D channel (multiple LAP). Discrimination between the data link connections is performed by means of a data link connection identifier (DLCI = SAPI + TEI)
- HDLC-framing
- Application of a balanced class of procedure in point-multipoint configuration.

The simplified block diagram in **figure 22** shows the functional blocks of the ISAC-S which support the LAPD protocol.

Figure 22
D-Channel Processing of the ISAC-2



For the support of LAPD the ISAC-S contains an HDLC transceiver which is responsible for flag generation/recognition, bit stuffing mechanism, CRC check and address recognition.

A powerful FIFO structure with two 64-byte pools for transmit and receive directions and an intelligent FIFO controller permit flexible transfer of protocol data units to and from the µC system.

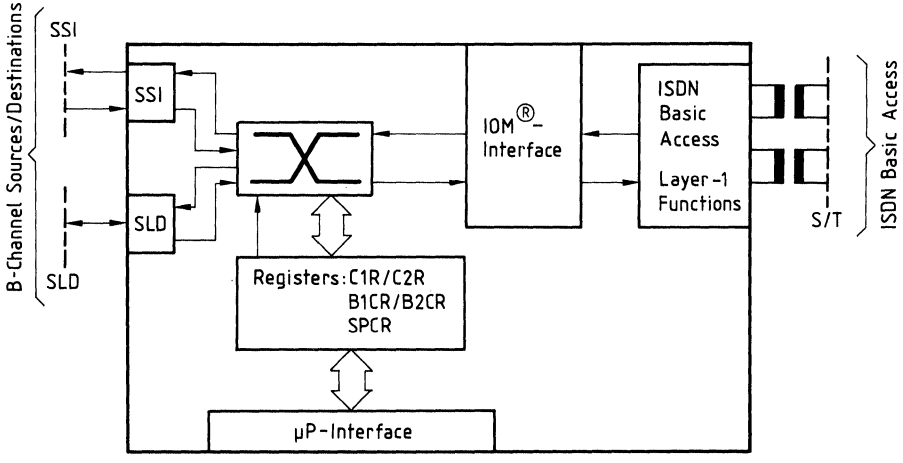
B Channel Switching (IOM-1)

The ISAC-S contains two serial interfaces, SLD and SSI, which can serve as interfaces to B channel sources/destinations. Both channels B1 and B2 can be switched independently of one another to the IOM interface and to the four-wire S/T interface **(figure 23)**.

The following possibilities are provided:

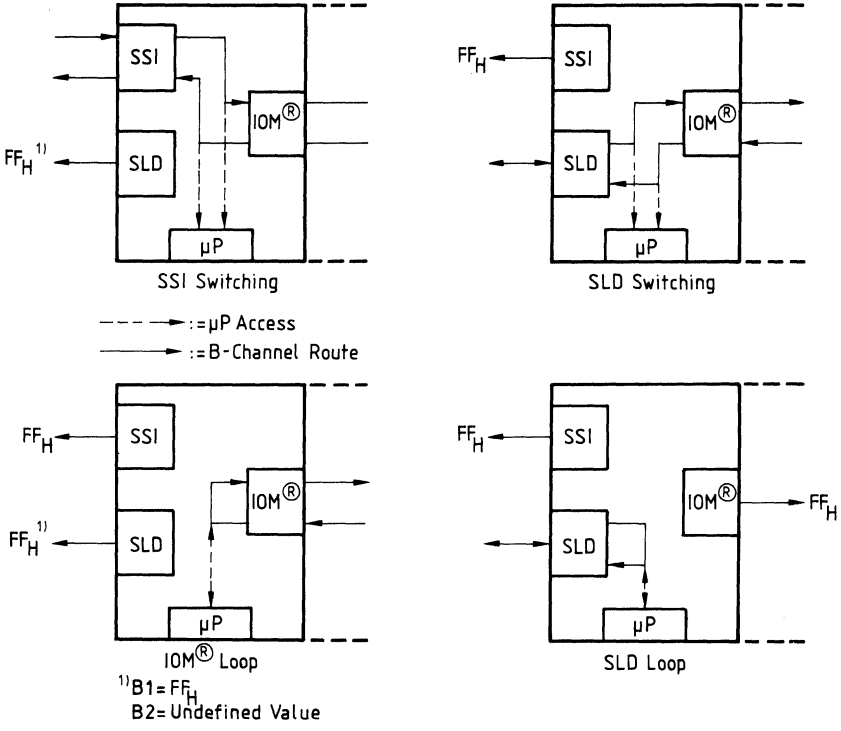
- Switching from/to SSI
- Switching from/to SLD
- IOM looping
- SLD looping

Figure 23
Principle of B-Channel Switching



The microcontroller can select the B-channel switching in the SPCR register. In **figure 24** all possible selections of the B-channel routes and access to B-channel data via the microprocessor interface are illustrated. This access from the microcontroller is possible by writing or reading the C1R/C2R register on reading the B1CR/B2CR register.

Figure 24
B-Channel Routes and Access to B-Channel Data



Access to B/IC Channels

IOM-1 Mode (IMS = 0)

The B1 and/or B2 channel is accessed by reading the B1CR/B2CR or by reading and writing the C1R/C2R registers. The µP access can be synchronized to the serial interface by means of a synchronous transfer programmed in the STCR register.

The read/write access possibilities are shown in **table 4**.

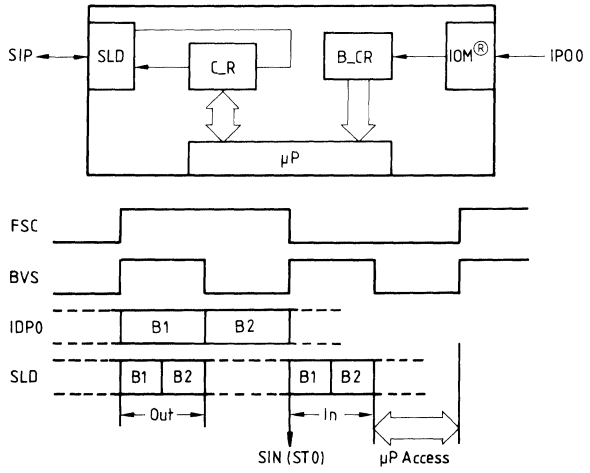
Table 4
µP Access to B Channel

		C_R		B_CR	
C_C1	**C_C0**	**Read**	**Write**	**Read**	**Application(s)**
0	0	SLD	SLD	IOM	B_not switched, SLD looping
0	1	SLD	–	IOM	B_switched to/from SLD
1	0	SSI	–	IOM	B_switched to/from SSI
1	1	IOM	IOM	–	IOM looping

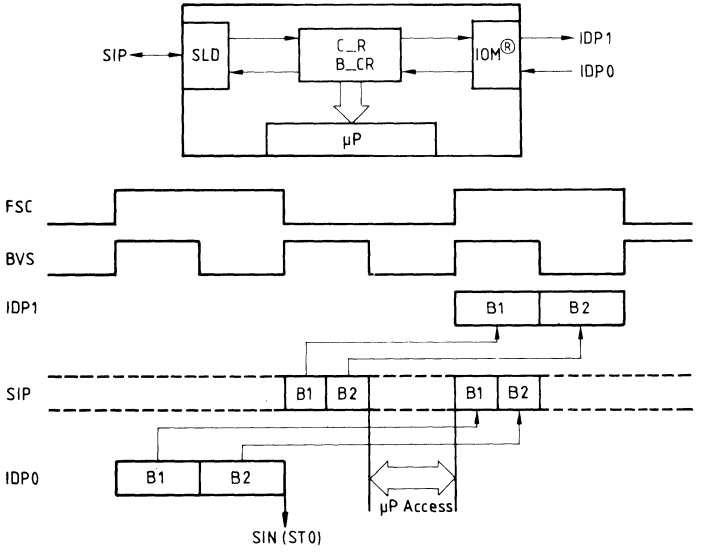
The synchronous transfer interrupt (SIN, ISTA register) can be programmed to occur at either the beginning of a 125 µs frame or at its center, depending on the channel(s) to be accessed and the current configuration, **see figure 25.**

Figure 25
B-Channel Access

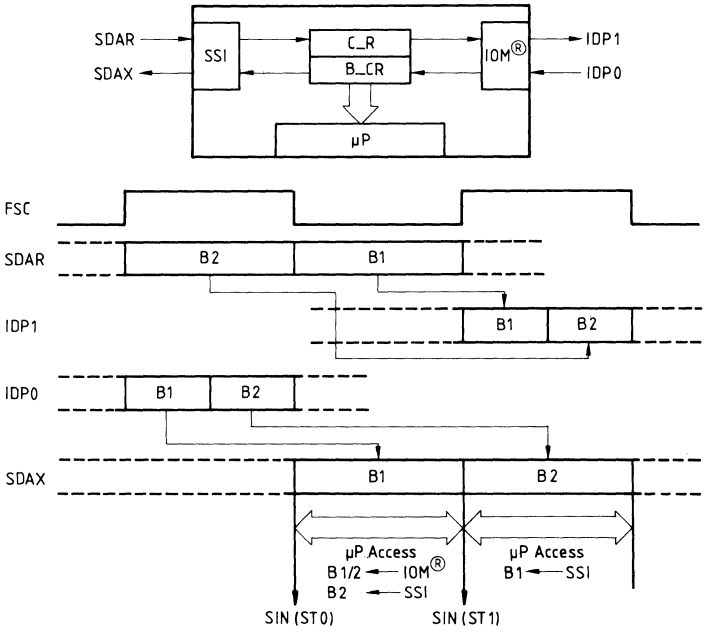
(a) C_C1, C_C0 = 00
SLD loop



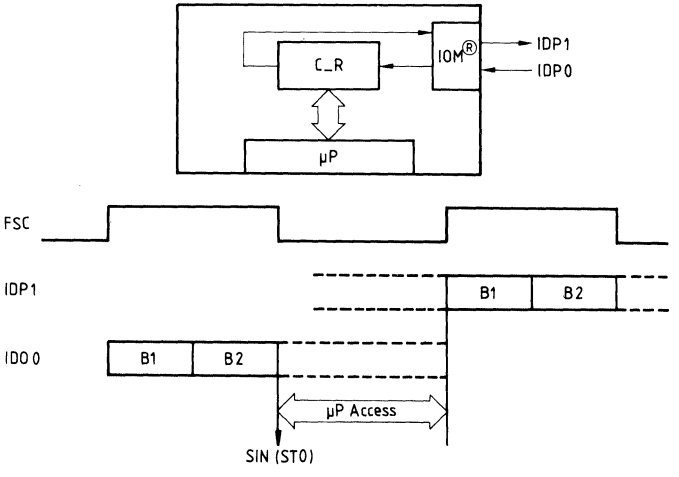
(b) C_C1, C_C0 = 01
SLD – IOM connection



(c) C_C1, C_C0 = 10
SSI – IOM connection



(d) C_C1, C_C0 = 11
IOM loop



IOM-2 Mode (IMS = 1)

The B1, B2 and/or IC1, IC2 channels are accessed by reading the B1CR/B2CR or by reading and writing the C1R/C2R registers. The µP access can be synchronized to the IOM interface by means of a synchronous transfer programmed in the STCR register.

The read/write access possibilities are shown in **table 5**.

Table 5
µP Access to B/IC Channels

C_C1	C_C0	C_R Read	C_R Write	B_CR Read	Output to IOM-2	Application(s)
0	0	IC_	–	B_	–	B_monitoring, IC_ monitoring
0	1	IC_	IC_	B_	IC_	B_monitoring, IC_looping from/to IOM-2
1	0	–	B_	B_	B_	B_access from/to S_0; transmission of a constant value in B_channel to S_0.
1	1	B_	B_	–	B_	B_looping from S_0; transmission of a variable pattern in B_channel to S_0.

The general sequence of operations to access the B/IC channels is:

(set configuration, register SPCR)

→ Program synchronous interrupt (ST0)

SIN → Read register (B_CR, C_R)
(write register)

Acknowledge SIN (SC0)

C/I Channel Handling

The command/indication channel carries real-time status information between the ISAC-S and another device connected to the IOM.

1) One C/I channel (called C/I0) conveys the commands and indications between a layer-1 device and a layer-2 device. This channel is available in all timing modes (IOM-1 or IOM-2). It can be accessed by an external layer-2 device e.g. to control the layer-1 activation/deactivation procedures. C/I0 channels access is arbitrated via the TIC bus access protocol:

– in IOM-1 mode, this arbitration is done in the monitor channel
– in IOM-2 TE timing mode, this arbitration is done in C/I channel 2 **(figure 17)**.

The C/I0 channel is accessed via register CIR0 (in receive direction, layer 1 to layer 2) and register CIX0 (in transmit direction, layer 2 to layer 1). The C/I0 code is four bits long.

In the receive direction, the code from layer 1 is continuously monitored, with an interrupt being generated anytime a change occurs. A new code must be found in two consecutive IOM frames to be considered valid and to trigger a C/I code change interrupt status (double last look criterion).

In the transmit direction, the code written in CIX0 is continuously transmitted in C/I0.

2) A second C/I channel (called C/I1) can be used to convey real time status information between the ISAC-S and various non-layer-1 peripheral devices e.g. PSB 2160 ARCOFI. The channel consists of six bits in each direction. It is available only in the IOM-2 TE timing mode **(see figure 17)**.

   The C/I1 channel is accessed via registers CIR1 and CIX1. A change in the received C/I1 code is indicated by an interrupt status without double last look criterion.

Monitor Channel Handling

IOM-1

The monitor channel protocol can be used to exchange one byte of information at a time between the ISAC-S and another device (e.g. a layer-1 transceiver).

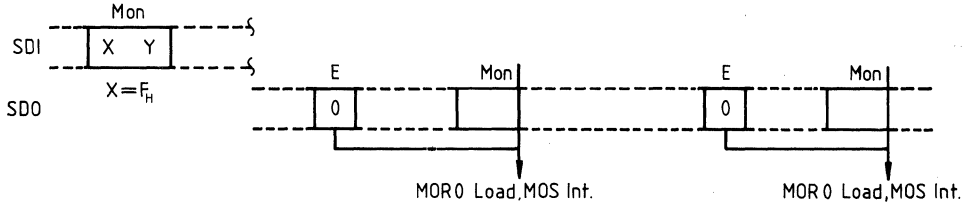
The procedure is as follows:

Monitor transmit channel 0 (MOX0) register is loaded with the value to be sent in the outgoing monitor channel. (Bytes of the form Fx_H are not allowed for this purpose because of the TIC bus collision resultion procedure).

The receiving device interprets the incoming monitor value as a control/information byte, Fx_H excluded. If no response is excepted, the procedure is complete. If the receiving device shall react by transmitting information to the ISAC-S, it should set the E bit to 0 and send the response in the monitor channel of the following frame. The ISAC-S

- latches the value in the monitor channel of the frame immediately following a frame with "E = 0" into MOR0 register.
- generates a monitor status interrupt MOS (EXIR register) to indicate that the MOR0 register has been loaded **(see figure 26)**.

Figure 26
Monitor Channel Protocol (IOM-1)



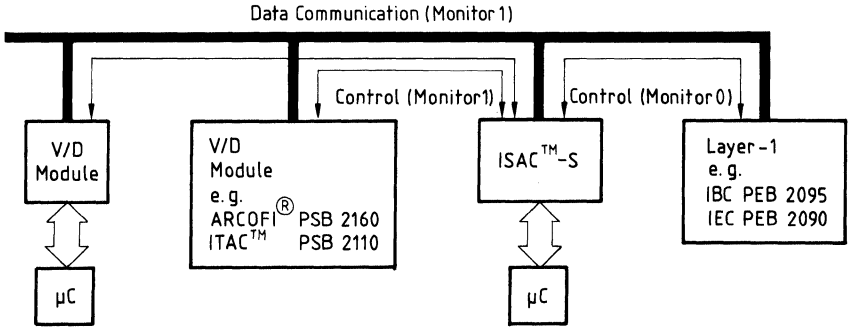
IOM-2

In this case, the monitor channel protocol is a handshake protocol used for high speed information exchange between the ISAC-S and other devices, in monitor channel 0 or 1 **(see figure 17)**. In the non-TE mode, only one monitor channel is available ("monitor channel 0").

The monitor channel protocol is necessary **(see figure 27)**:

- For programming and controlling devices attached to the IOM. Examples of such devices are: layer-1 transceivers (using monitor channel 0), and peripheral V/D modules that do not have a parallel microcontroller interface (monitor channel 1), such as the audio ringing codec filter PSB 2160.
- For data exchange between two microcontroller systems attached to two different devices on one IOM-2 backplane. Use of the monitor channel avoids the necessity of a dedicated serial communication path between the two systems. This greatly simplifies the system design of terminal equipment **(figure 27)**.

Figure 27
Examples of Monitor Channel Applications



The monitor channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the Monitor Channel Receive (MR0 or 1) and Monitor Channel Transmit (MX0 or 1) bits. For example: data is placed onto the monitor channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The microprocessor may either enforce a "1" (idle) in MR, MX by setting the control bit MRC1,0 or MXC1,0 to "0" (MOnitor Control Register MOCR), or enable the control of these bits internally by the ISAC-S according to the monitor channel protocol. Thus, before a data exchange can begin, the control bit MRC(1,0) or MXC(1,0) should be set to "1" by the microprocessor.

The monitor channel protocol is illustrated in **figure 28**. Since the protocol is identical in monitor channel 0 and monitor channel 1 (available in TE mode only), the index 0 or 1 has been left out in the illustration.

The relevant status bits are:

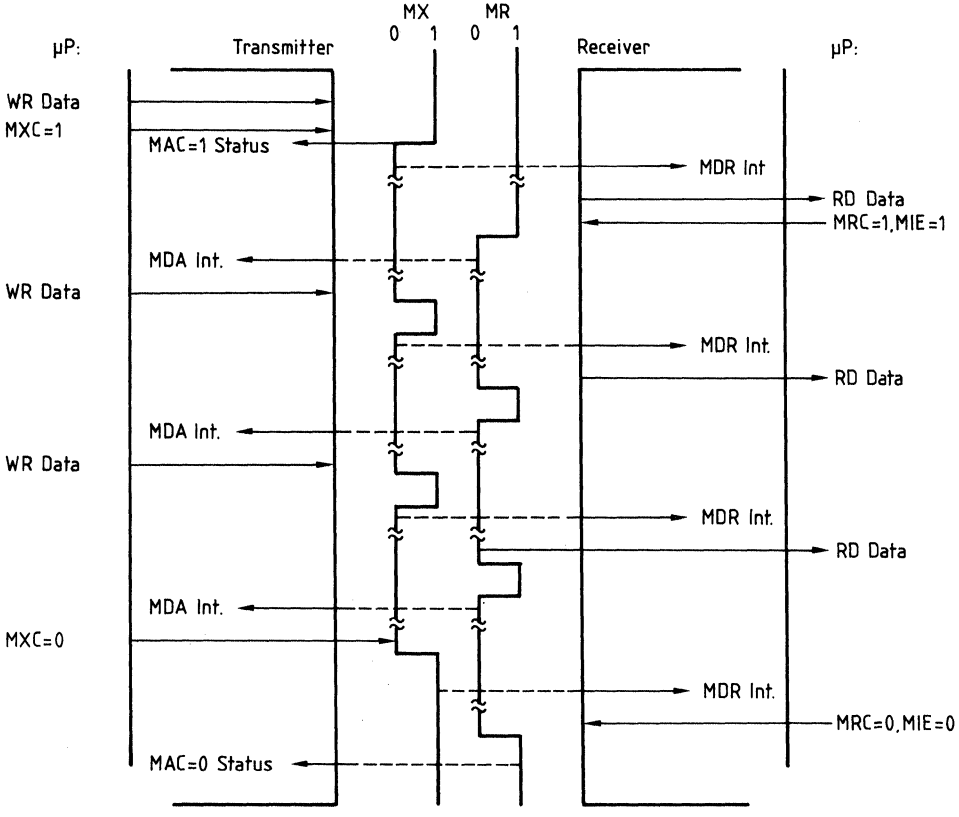
Monitor Channel Data Received MDR (MDR0, MDR1)
Monitor Channel End of Reception MER (MER0, MER1)

for the reception of monitor data, and

Monitor Channel Data Acknowledged MDA (MDA0, MDA1)
Monitor Channel Data Abort MAB (MAB0, MAB1)

for the transmission of monitor data (Register: MOSR).
In addition, the status bit:
Monitor Channel Active MAC (MAC0, MAC1)
indicates whether a transmission is in progress (Register: STAR).

Figure 28
Monitor Channel Protocol



Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a "0" in the monitor channel active MAC status bit.

After having written the monitor data transmit (MOX) register, the microprocessor sets the monitor transmit control bit MXC to 1. This enables the MX bit to go active (0), indicating the presence of valid monitor data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the monitor byte in its monitor receive MOR register and generates a MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the monitor receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to "1" to enable the receiver to store succeeding monitor channel bytes and acknowledge them according to the monitor channel protocol. In addition, it enables other Monitor channel interrupts by setting monitor interrupt enable to "1".

As a result, the first monitor byte is acknowledged by the receiving device setting the MR bit to "0". This causes a monitor data acknowledge MDA interrupt status at the transmitter.

A new monitor data byte can now be written by the microprocessor in MOX. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the monitor channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the monitor byte in MOR and generates a new MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate a MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send. Note that the monitor channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the monitor transmit control bit MXC to 0. This enforces an inactive ("1") state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a monitor channel end of reception MER interrupt status is generated by the receiver when the MX is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the monitor channel active MAC bit return to "0".

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending a inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to 0. An aborted transmission is indicated by a monitor channel data abort MAB interrupt status at the transmitter.

Terminal Specific Functions

In addition to the ISAC-S standard functions supporting the ISDN basic access, the ISAC-S contains optional functions, useful in various terminal configurations.

The terminal specific functions are enabled by setting bit TSF (STCR register) to "1". This has two effects:

- The SIP/EAW line is defined as external awake input (and not as SLD line);
- Second, the interrupts SAW and WOV (EXIR register) are enabled:
  - SAW (subscriber awake) generated by a falling edge on the EAW line
  - WOV (watchdog timer overflow) generated by the watchdog timer. This occurs when the processor fails to write two consecutive bit patterns in ADF1:

ADF1	WTC1	WTC2	

Watchdog Timer Control 1, 0.

The WTC1 and WTC2 bits have to be successively written in the following manner within 128 ms:

	WTC1	WTC2
1.	1	0
2.	0	1

As a result the watchdog timer is reset and restarted. Otherwise a WOV is generated.

Deactivating the terminal specific functions is only possible with a hardware reset.

Having enabled the terminal specific functions via TSF = 1, the user can make the ISAC-S generate a reset signal by programming the Reset Source Select **RSS** bit (CIX0 register), as follows:

0 → A reset signal is generated as a result of
  - a falling edge on the EAW line (subscriber awake)
  - a C/I code change (exchange awake).

  A falling edge on the EAW line also forces the IDP1 line of the IOM interface to zero. The consequence of this is that the IOM interface and the ISAC-S leaves the power-down state.

  A corresponding interrupt status (CISQ or SAW) is also generated.

1 → A reset signal is generated as a result of the expiration of the watchdog timer (indicated by the WOV interrupt status).

  Note that the watchdog timer is not running when the ISAC-S is in the power-down state (IOM not clocked).

Note: Bit RSS has a signifinace only if terminal specific functions are activated (TSF = 1).

The RSS bit should be set to "1" by the user when the ISAC-S is in power-up to prevent an edge on the EAW line or a change in the C/I code from generating a reset pulse.

Switching RSS from 0 to 1 or from 1 to 0 resets the watchdog timer.

The reset pulse generated by the ISAC-S (output via RST pin) has a pulse width of:

- 125 µs when generated by the watchdog timer
- 16 ms when generated by EAW line or C/I code change.

Test Functions

The ISAC-S provides several test and diagnostic functions which can be grouped as follows:

- Digital loop via TLP (test loop, SPCR register) command bit: IDP1 is internally connected with IDP0, output from layer 1 (S/T) on IDP0 is ignored; this is used for testing ISAC-S functionality excluding layer 1;
- Test of layer-2 functions while disabling all layer-1 functions and pins associated with them (including clocking, in TE mode), via bit TEM (test mode, SQXR register); the ISAC-S is the fully compatible to the ICC (PEB 2070) seen at the IOM interface.
- Loop at the analog end of the S interface; either info 0 (non-transparent loop: TE/LT-T modes) or info 4 transparent loop: NT/LT-S modes) is sent over the S/T interface during the loop, which is closed via a C/I command written in CIX0 register;
- Special loops programmed via C2C1-0 and C1C1-0 bits (register SPCR);
- Transmission of special test signals on the S/T interface according to the modified AMI code, initiated via a C/I command written in CIX0 register:
  - Single pulses of alternating polarity, one S/T interface bit period wide, with a 2-kHz repetition frequency;
  - Continuous pulses of alternating polarity, one S/T interface bit period wide, with a 96-kHz repetition frequency.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SSA} = 0\ V$, $V_{SSD} = 0\ V$

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	Remarks
L-input voltage		V_{IL}	−0.4	0.8	V		All pins except SX1,2, SR1,2
H-input voltage (all except X1 and RST)		V_{IH}	2.0	V_{DD} +0.4	V		All pins except SX1,2 SR1,2
L-output voltage L-output voltage (IDPO)		V_{OL} V_{OL1}		0.45 0.45	V V	$I_{OL} = 2$ mA $I_{OL} = 7$ mA	All pins except SX1,2 SR1,2
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD} −0.5		V V	$I_{OH} = -400$ µA $I_{OH} = -100$ µA	All pins except SX1,2 SR1,2
Power supply current	operation	I_{CC}		15 17 27	mA mA mA	DCLK = 512 kHz DCLK = 1536 kHz DCLK = 4096 kHz	$V_{DD} = 5$ V Inputs at V_{SS}/V_{DD} No output loads
	power down	I_{CC}		1.5	mA		
Input leakage current Output leakage current		I_{LI} I_{LO}		10	µA	$0\ V < V_{IN} < V_{DD}$ to 0 V $0\ V < V_{OUT} < V_{DD}$ to 0 V	All pins except SX1,2, SR1,2
Absolute value of output pulse amplitude $V_{SX2} - V_{SX1}$		V_X	2.03 2.10	2.31 2.39	V V	$R_L = 50\ \Omega$ [1] $R_L = 400\ \Omega$ [1]	SX1,2
Transmitter output current		I_X	7.5	13.4	mA	$R_L = 5.6\ \Omega$ [1]	SX1,2
Transmitter output impedance		R_X	10		kΩ	Inactive or during binary one	SX1,2
			0		Ω	during binary zero $R_L = 50\ \Omega$	
Receiver output voltage		V_{SR1}	2.4	2.6	V	$I_O < 5$ µA	SR1,2
Receiver threshold voltage $V_{SR2} - V_{SR1}$		V_{TR}	+225	+375	mV	Dependent on peak level	SR1,2

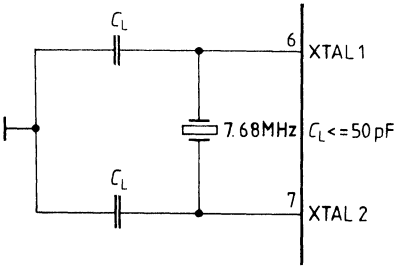
[1]) Due to the transformer, the load resistance seen by the circuit is four times R_L.

Capacitances

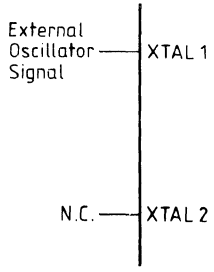
$T_A = 25\,°C$; $V_{DD} = 5\,V \pm 5\%$, $V_{SSD} = 0\,V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Remarks
Input capacitance I/O capacitance	C_{IN} C_{IO}		7 7	pF pF	All pins except SR1,2, XTAL1,2
Output capacitance against V_{SSA}	C_{OUT}		10	pF	SX1,2
Input capacitance	C_{IN}		7	pF	SR1,2
Load capacitance	C_L		50	pF	XTAL1,2

Recommended Oscillator Circuits



Crystal Oscillator Mode



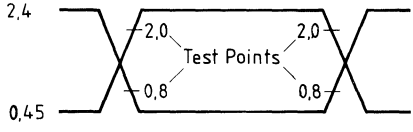
Driving from External Source

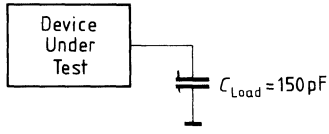
AC Characteristics

$T_A = 0$ to $70\,°C$; $V_{DD} = 5\,V \pm 5\%$

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown below.

Figure 29
Input/Output Waveform for AC Test

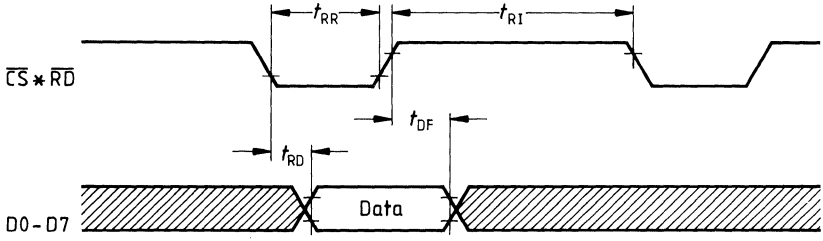




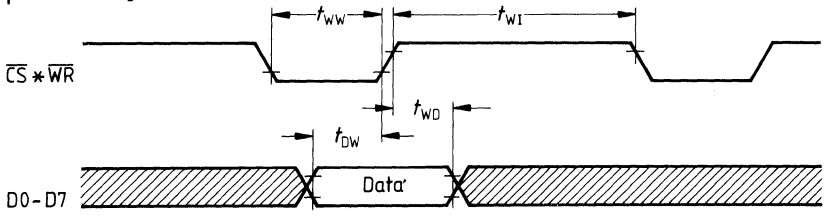
Microprocessor Interface Timing

Intel Bus Mode

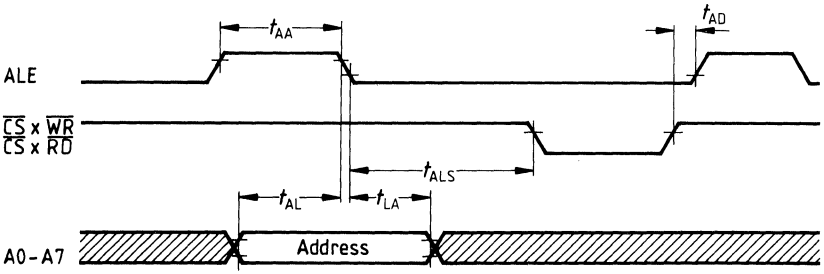
µP Read Cycle



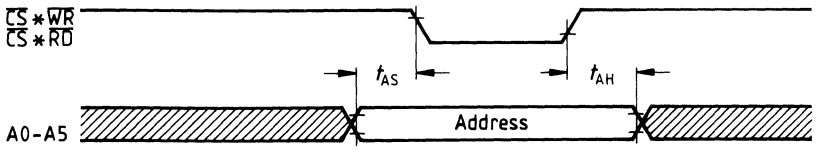
µP Write Cycle



Multiplexed Address Timing

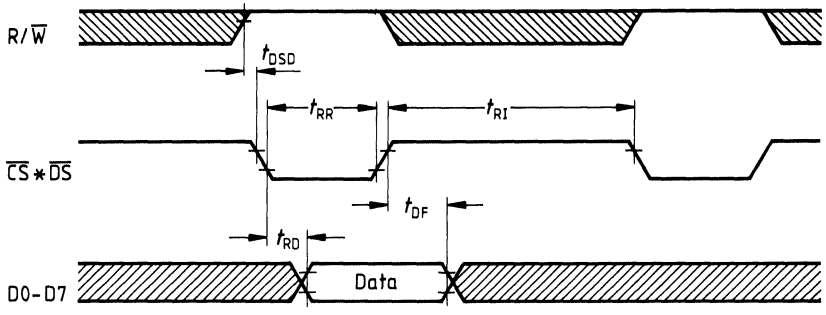


Non-multiplexed Address Timing

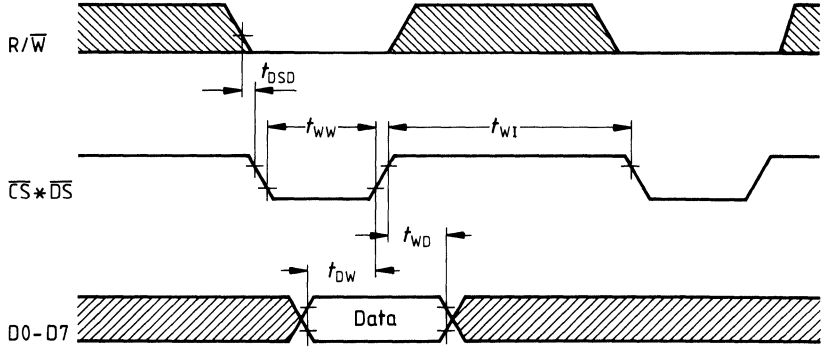


Motorola Bus Mode

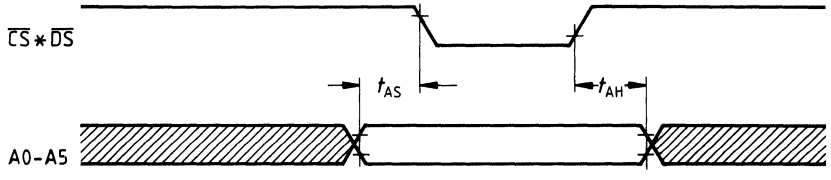
µP Read Cycle



µP Write Cycle



Address Tming

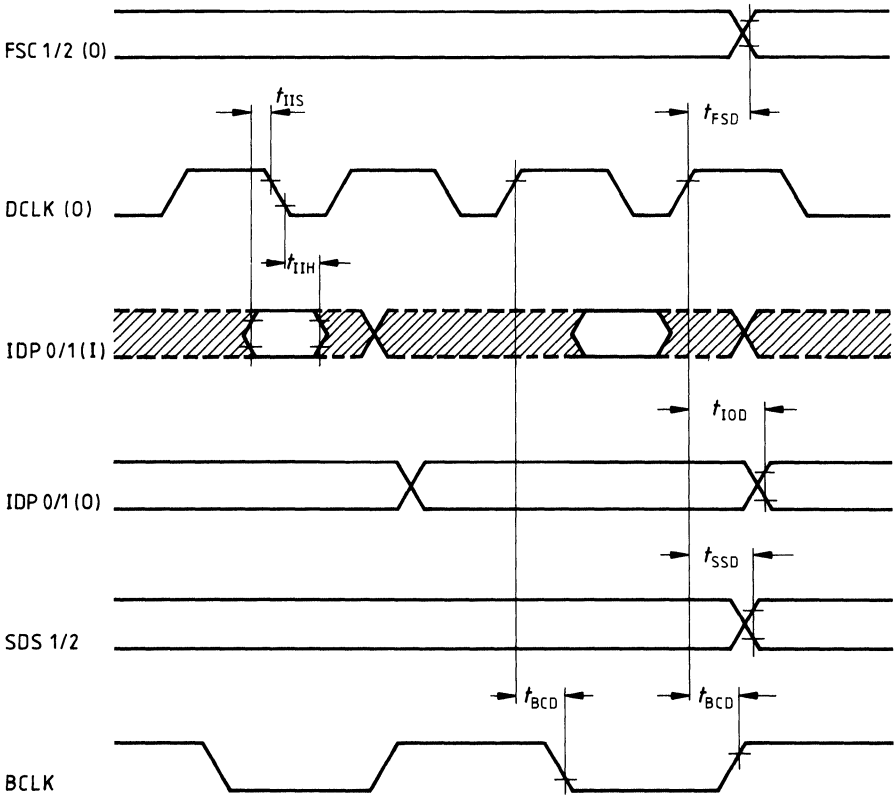


Switching Times

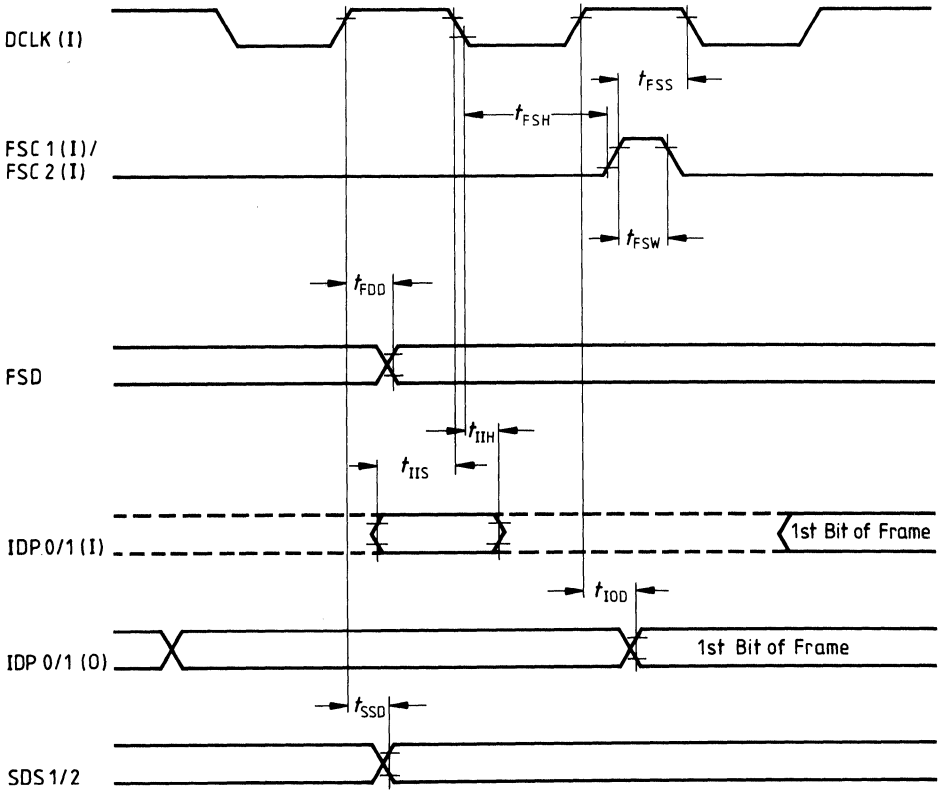
Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	20		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	20		ns
ALE pulse delay	t_{AD}	15		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ * $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{WR}$ * $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

Serial Interface Timing
IOM Timing
IOM Mode

IOM Timing (TE Mode)



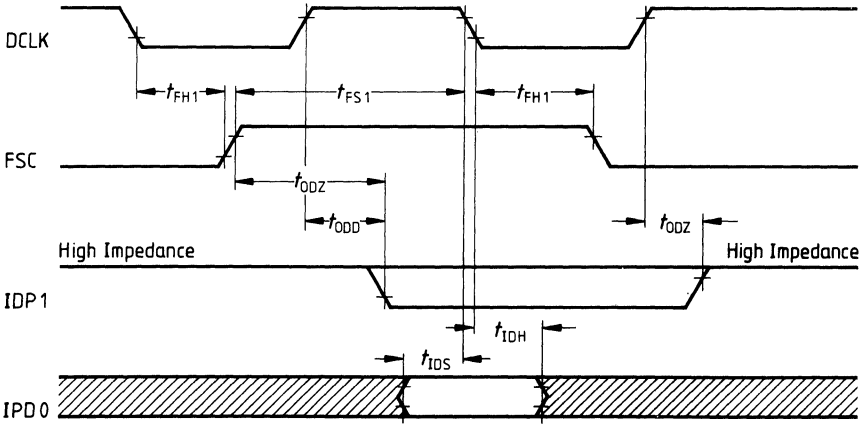
IOM Timing (LT-S, LT-T, NT Mode)



Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
IOM output data delay	t_{IOD}	20 20	140 100	ns ns	IOM-1 IOM-2
IOM input data setup	t_{IIS}	40 + t_{WH} 20		ns ns	IOM-1 IOM-2
IOM input data hold	t_{IIH}	20		ns	
FSC1/2 strobe delay	t_{FSD}	−20	20	ns	
Strobe signal delay	t_{SDD}		120	ns	
Bit clock delay	t_{BCD}	−20	20	ns	
Frame sync setup	t_{FSS}	50		ns	
Frame sync hold	t_{FSH}	30		ns	
Frame sync width	t_{FSW}	40		ns	
FSD delay	t_{FDD}	20	140	ns	

HDLC Mode

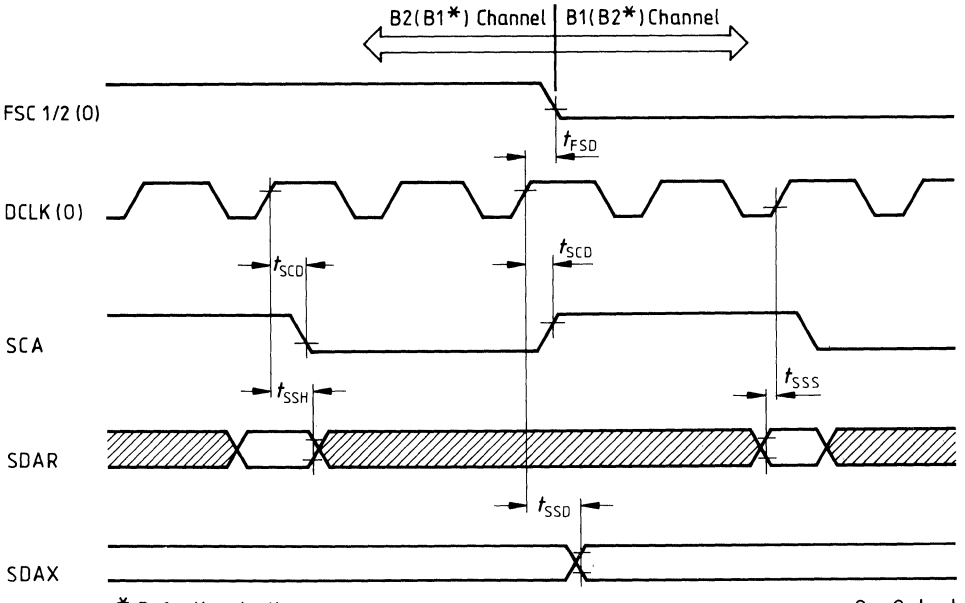
FSC1 (Strobe) Characteristics



Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC1 setup time	t_{FS1}	100		ns
FSC1 hold time	t_{FH1}	30		ns
Output data from high impedance to active	t_{OZD}		80	ns
Output data from active to high impedance	t_{ODZ}		40	ns
Output data delay from DCL	t_{ODD}	20	100	ns
Input data setup	t_{IDS}	10		ns
Input data hold	t_{IDH}	30		ns

Serial Port A (SSI) Timing

SSI Timing (TE, Timing Mode 0)



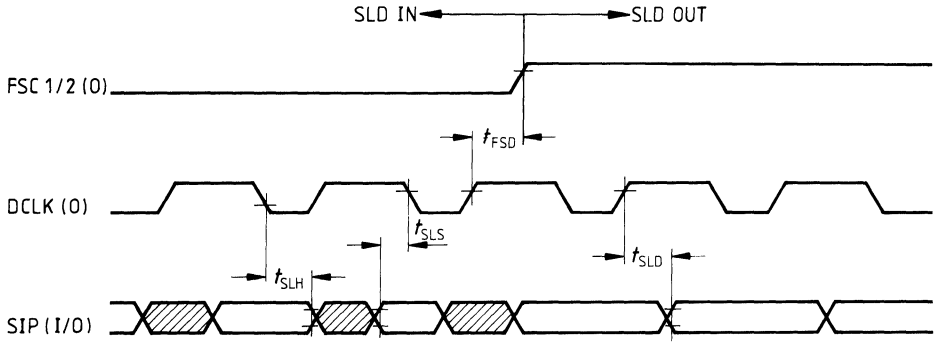
* Default polarity
Individual B channel switching to the B1- or B2 channel can be selected by programming the output polarity of FSC 1 and FSC 2 in the ADFR register

0: = Output

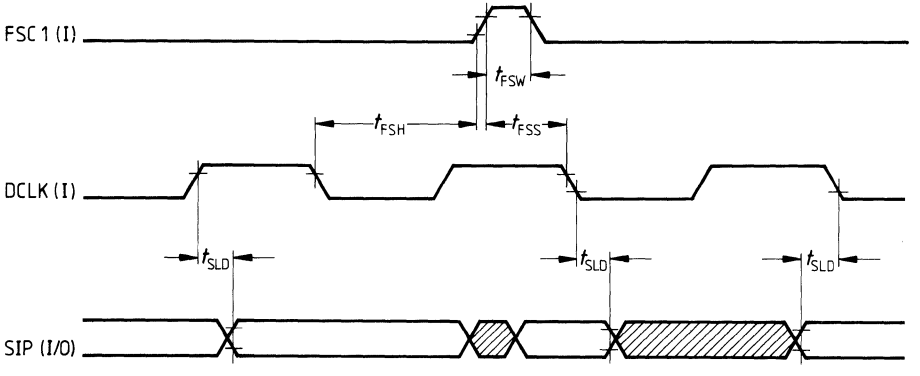
Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCA clock delay	t_{SCD}	20	140	ns
SSI data delay	t_{SSD}	20	140	ns
SSI data setup	t_{SSS}	40		ns
SSI data hold	t_{SSH}	20		ns
FSC1/2 strobe delay	t_{FSD}	−20	20	ns

SLD Timing

SLD Timing (TE Mode)



SLD Timing (LT-S/LT-T Mode)



SLD Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SLD data delay	t_{SLD}	20	140	ns
SLD data setup	t_{SLS}	30		ns
SLD data hold	t_{SLH}	30		ns
FSC1/2 strobe delay	t_{FSD}	−20	20	ns
Frame sync setup	t_{FSS}	50		ns
Frame sync hold	t_{FSH}	30		ns
Frame sync width	t_{FSW}	40		ns

Clock Timing

The clocks in the different operating modes are summarized in **table 7-8,** with the respective duty ratios.

Table 7
ISAC-S Clock Signals (IOM-1 Mode)

Application	M2	M0	DCLK	FSC1/2	CP	X1
TE	0	0	o: 512 kHz* 2:1	o: 8 kHz* 1:1	o: 1536 kHz* 3:2	o: 3840 kHz 1:1
LT-S	1	0	i: 512 kHz	i: 8 kHz		o: 7680 kHz 1:1
LT-T	0	1	i: 512 kHz	i: 8 kHz	o: 512 kHz* 2:1	
NT	1	1	i: 512 kHz	i: 8 kHz		

* synchronized to S i: input o: output

Table 8
ISAC-S Clock Signals (IOM-2 Mode)

Application	M1	M0	DCLK	FSC1	CP/BCLK	X1	SDS1/2
TE	0	0	o: 1536 kHz* 3:2	o: 8 kHz* 1:1	o: 768 kHz* 1:1	o: 3840 kHz 1:1	o: 8 kHz 1:11 2:10
LT-S	1	0	i: 4096 kHz	i: 8 kHz		o: 7680 kHz 1:1	o: 8 kHz 1:11 2:10
LT-T	0	1	i: 4096 kHz	i: 8 kHz	o: 512 kHz* 2:1		o: 8 kHz 1:11 2:10
NT	1	1	i: 512 kHz	i: 8 kHz			o: 8 kHz 1:11 2:10

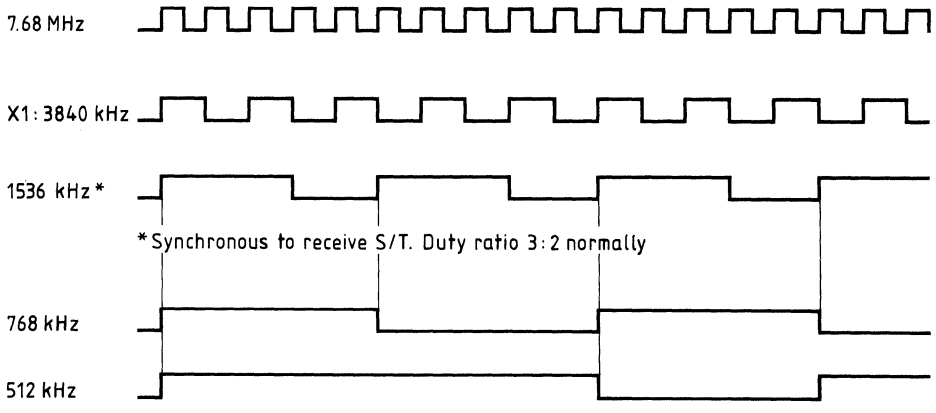
* synchronized to S i: input o: output

The 1536-kHz clock (TE mode) and the 512-kHz clock (LT-T mode) are phase-locked to the receive S signal, and derived using the internal DPLL and the 7.68 MHz ±100 ppm crystal.

A phase tracking with respect to "S" is performed once in 250 µs. As a consequence of this DPLL tracking, the "high" state of the 1536-kHz clock may be either reduced or extended by one 7.68-MHz period (duty ratio 2:2 or 4:2 instead of 3:2) once every 250 µs. Since the other signals are derived from this clock (TE mode), the "high" or "low" states may likewise be reduced or extended by the same amount once every 250 µs.

The phase relationships of the clocks are shown in

Figure 30



The timing relationship between the clocks are specified in **figure 31** and **table 9.**

Figure 31

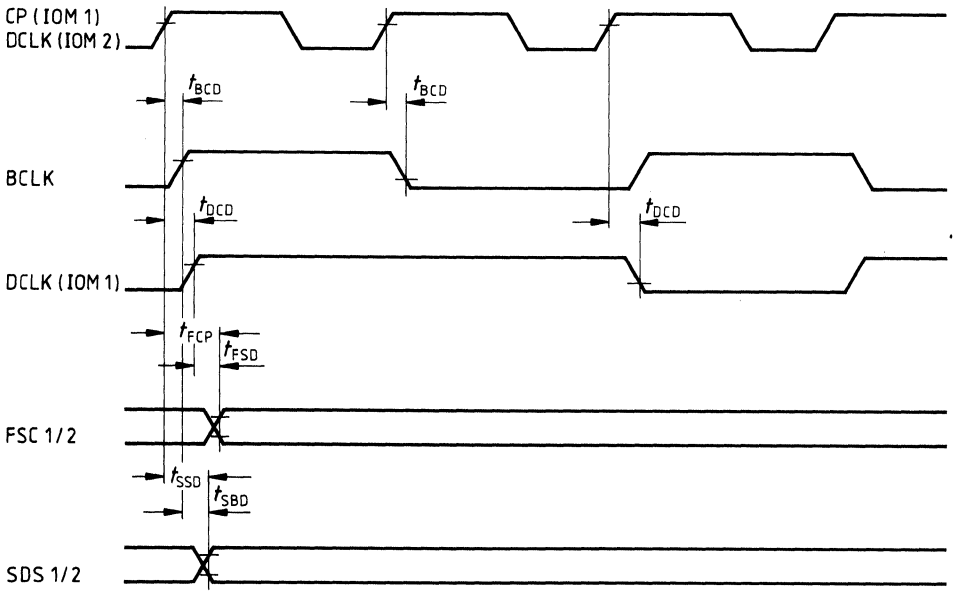


Table 9

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Bit clock delay	t_{BCD}	−20	20	ns	IOM-2
SDS1/2 delay from DCLK	t_{SDD}		120	ns	IOM-2
SDS1/2 delay drom BCLK	t_{SBD}		120	ns	IOM-2
DCLK delay from CP	t_{DCD}	0	50	ns	IOM-1
FSC1/2 delay from CP	t_{FCP}	0	50	ns	IOM-1
FSC1/2 delay from DCLK	t_{FSD}	−20	20	ns	IOM-1

Tables 10 to 15 gives the timing characteristics of the clock.

Definition of Clock Period and Width

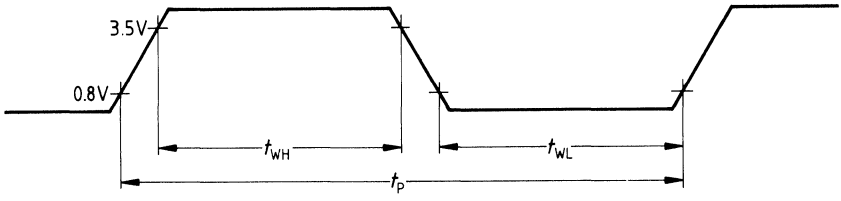


Table 10
DCLK Clock Characteristics (IOM-1)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 512 kHz	$t_{P\,O}$	1822	1953	2084	ns	OSC ± 100 ppm
(TE) 512 kHz 2:1	$t_{WH\,O}$	1121	1302	1483	ns	OSC ± 100 ppm
(TE) 512 kHz 2:1	$t_{WL\,O}$	470	651	832	ns	OSC ± 100 ppm
(NT, LT-S, LT-T)	$t_{P\,I}$	1853		2053	ns	
(NT, LT-S, LT-T)	$t_{WH\,I}$	200			ns	
(NT, LT-S, LT-T)	$t_{WL\,I}$	200			ns	

Table 11
DCLK Clock Characteristics (IOM-2)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 1536 kHz	$t_{P\,O}$	520	651	782	ns	OSC ± 100 ppm
	$t_{WH\,O}$	240	391	541	ns	OSC ± 100 ppm
	$t_{WL\,O}$	240	260	281	ns	OSC ± 100 ppm
(LT-S, LT-T)	$t_{P\,I}$	240	244		ns	
	$t_{WH\,I}$	100			ns	
	$t_{WL\,I}$	100			ns	

Note: For NT characteristics, see IOM-1 case.

Table 12
CP Clock Characteristics (IOM-1 TE Mode)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 1536 kHz	t_{PO}	520	651	782	ns	OSC ± 100 ppm
	t_{WHO}	240	391	541	ns	OSC ± 100 ppm
	t_{WLO}	240	260	281	ns	OSC ± 100 ppm
	t_R, t_F			20	ns	C_L = 100 pF
				10	ns	C_L = 50 pF

Table 13
CP Clock Characteristics (LT-T Mode)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(LT-T) 512 kHz	t_{PO}	1822	1953	2084	ns	OSC ± 100 ppm
	t_{WHO}	1121	1302	1483	ns	OSC ± 100 ppm
	t_{WLO}	470	651	832	ns	OSC ± 100 ppm
	t_R, t_F			20	ns	C_L = 100 pF
				10	ns	C_L = 50 pF

Table 14
X1 Clock Characteristics (TE Mode)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 3840 kHz	t_{PO}	−100	260	100	ns	OSC ± 100 ppm
	t_{WHO}	120	130	140	ns	OSC ± 100 ppm
	t_{WLO}	120	130	140	ns	OSC ± 100 ppm

Table 15

X1 Clock Characteristics (LT-S Mode)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(LT-S) 7680 kHz	t_{PO}	−100	130.21	100	ns	OSC ± 100 ppm
	t_{WHO}		65		ns	OSC ± 100 ppm
	t_{WLO}		65		ns	OSC ± 100 ppm

Jitter

In TE mode, the timing extraction jitter of the ISAC-S conforms to CCITT Recommendation I.430 (−7% to +7% of the S interface bit period).

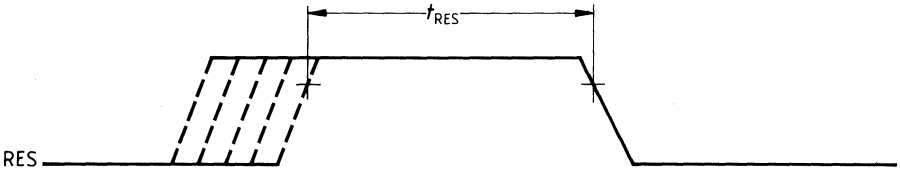
In the NT and LT-S applications, the clock input DCLK is used as reference clock to provide the 192-kHz clock for the S line interface. In the case of a plesiochronous 7.68-MHz clock generated by an oscillator, the clock DCLK should have a jitter less than 100 ns peak-to-peak. (In the case of a zero input jitter on DCLK, ISAC-S generates at most 130 ns "self-jitter" on S interface.)

In the case of a synchronous*) 7.68-MHz clock (input XTAL1), the ISAC-S transfers the input jitter of XTAL1, DCLK and FSC1 to the S interface. The maximum jitter of the NT/LT-S output is limited to 260 ns peak-to-peak (CCITT I.430).

* fixed divider ratio between XTAL1 and DCLK

Reset

Reset Signal Characteristics



Parameter	Symbol	Limit Values min.	Unit	Test Conditions
Length of active high state (Input)	t_{DCLK}	4	ms	Power On/Power Down to Power Up (Standby)
		2* DCLK clock cycles		During Power Up (Standby)