SIEMENS

ISDN Ech-Cancellation Circuit (IEC-Q) PEB 2091

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2091-N	Q67100-H6119	PL-CC-44 (SMD)

The PEB 2091 ISDN Echo-Cancellation Circuit (IEC-Q) is an advanced CMOS transceiver for ISDN Basic Access Digital Subscriber Loops with 2B1Q line code.

Control and algorithmic requirements are implemented according to the layer-1 specification of the American National Standard Institute (ANSI) for a 144 bit/s full duplex data transmission.

Together with the flexible IOM-2 interface, the IEC-Q is fully compatible with the PEB 2081 (SBCX), PEB 2055 (EPIC™) and PEB 2075 (IDEC™) devices.

Features

- U Transceiver with 2B1Q line code according to layer-1 specification of ANSI
- Activation and deactivation procedure according to T1D1 layer-1 specification and CCITT I.430
- Programmable operation modes
- IOM-2 interface
- Adaptive echo cancellation
- Adaptive equalization
- Automatic polarity adaptation
- Clock recovery (frame and bit synchronization)
- Low power consumption

Basic System Functions

- Full duplex data transmission and reception at the U reference point according to the layer-1 specification of the American National Standard Institute:
  - 144 bit/s user bit rate over a two-wire subscriber loop
  - 2B1Q block code (2 binary, 1 quaternary)
  - 4 bit/s maintenance channel for transmission of data loop back commands and detected transmission errors
  - monitoring of transmission errors
  - operating at telephone loop plant LOOP#1 up to LOOP#15 as defined by American National Standard
- Transposition of quaternary to binary data and vice versa (coding, decoding, scrambling, descrambling, phase adaption)
- Built-in wake up unit for activation from power down state
- Activation and deactivation procedure according to T1D1 layer-1 specification and CCITT I.430
- Adaption of internal interfaces to the current signal direction by programmable operation modes:

LT:	Line termination in public or private exchange
TE:	Terminal mode
NT:	Network termination connected to SBCX
NT-PBX:	Trunk module (TDM)

- Adaptive echo cancellation
- Adaptive equalization
- Automatic polarity adaption
- Clock recovery (frame and bit synchronization) in all applications
- Optimized for working in conjunction with SBCX, ICC, EPIC and IDEC telecom ICs via IOM-2 interface
- Data speed conversion between the U reference point and the IOM frames
- Handling of the commands and indications contained in the IOM-2 C/I channel for deactivation, activation, supervision of power supply unit and equipment for testing
- Data availability via monitor-channel:
  - CRC transmission errors
  - Measurement value of the loop current
  - Echo canceler coefficients and status values, which can be used to indicate the state of the loop
- Switching test loops
- Generation of synchronized 7.68-MHz clock for SBCX in NT mode
- Low power consumption: standby: max. 30 mW
  active: max. 300 mW

Functional Description

The IEC-Q can be subdivided into three main blocks:

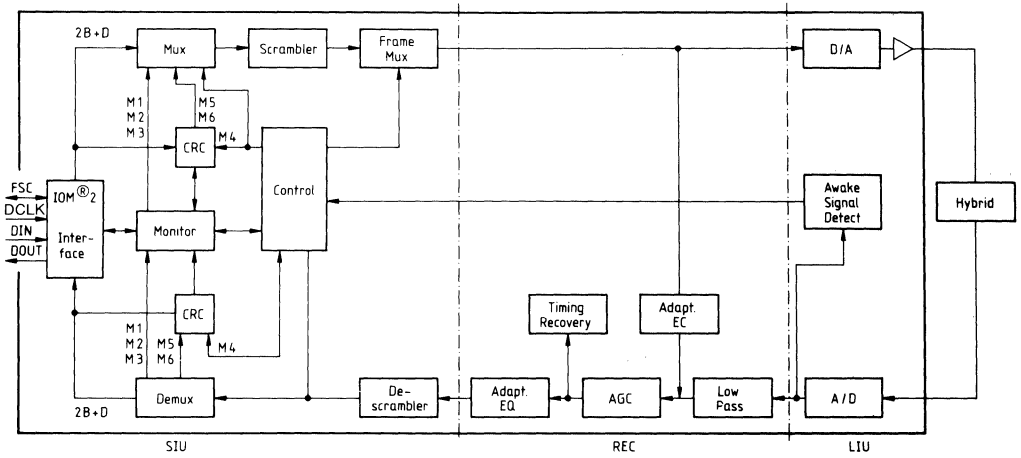
- LIU Line Interface Unit
- SIU System Interface Unit
- REC Receiver

The Line Interface Unit (LIU) contains the crystal oscillator and all of the analog functions, namely the A/D converter in the receive path, pulse shaping D/A converter and line driver in the transmit path.

The System Interface Unit (SIU) features the activation and deactivation procedures, the timing recovery and synchronization, maintenance data handling, frame conversion and speed adaption.

The Receiver block (REC) performs the filter algorithmic functions using digital signal processing techniques. In a modular multi-processor concept modules for echo cancellation, pre- and post-equalization, phase adaption and frame detection are implemented.

Block Diagram of IEC-Q



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
7, 8	V_{DDA1}	S	Analog supply voltage 5 V ± 5%
13	V_{DDA2}	S	Analog supply voltage 5 V ± 5%
5	GNDA1	S	Analog 0 V
16	GNDA2	S	Analog 0 V
1, 2	V_{DDD}	S	Digital supply voltage 5 V ± 5%
23	GNDD	S	Digital 0 V
11	XTAL0	I	Crystal connection or external clock input
10	XTAL1	I	Crystal connection. Left unconnected if external clock is used
15	AIN	I	Received line signal to hybrid
14	BIN	I	Received line signal to hybrid
6	AOUT	O	Transmitted line signal to hybrid
4	BOUT	O	Transmitted line signal to hybrid
9	V_{REF}	O	V_{REF}-pin to buffer internally generated voltage with capacitor 10 nF vs GNDA
31	DCLK	I/O	IOM-2 device clock
30	FSC	I/O	IOM-2 frame clock
26	DIN	I	IOM-2 data input synchronous to DCLK
22	LT	I	LT mode (HIGH input = LT mode) (LOW input = NT mode)
24	BURST	I	NT-, NT-TE mode (LOW) LT-, NT-PBX mode (HIGH)
36	SLOT0	I	256 kbit/s modes select Allocation of time slot for BURST mode
35	SLOT1	I	256 kbit/s modes select Allocation of time slot for BURST mode
33	SLOT2	I	256 kbit/s modes select Allocation of time slot for BURST mode
32	PFCLE	I/O	TE/NT: 7.68-MHz clock out sync to line signal NT-PBX: 512-kHz clock out sync to line signal LT: Power feed off must be clamped to LOW if not used

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
21	PS1	I	NT: Power status (primary)
22	PS2	I	NT: Power status (secondary)
18	PFC	I	Monitor power feed (active HIGH) serial data of power feed current
3	TSP	I	Test single pulses must be clamped to LOW if not used
28	RESQ	I	Power-on reset (active LOW) must be LOW at least 300 usec. The clock on the DCLK pin has to be applied during RESET in the LT-modes and in the NT-PBX-mode. Must be clamped to HIGH if not used.
27	DOUT	O	IOM-2 data output synchronous to DCLK
37	DISS	O	Disable supply (active HIGH)
19	RD1	O	Relay driver control (via IOM monitor)
20	RD2	O	Relay driver control (via IOM monitor)
29	TP	I	Test pin (must be clamped to LOW during normal operation)
44	TM0	I/O	Test pin (must be clamped to HIGH during normal operation)
43	TM1	I/O	Test pin (must be clamped to HIGH during normal operation)
42	TM2	I/O	Test pin (must be clamped to HIGH during normal operation)
41	TM3	I/O	Test pin (must be clamped to HIGH during normal operation)
30	TM4	I/O	TE mode (HIGH) Auto mode (LOW)
39	TM5	I/O	Test pin (must be clamped to HIGH during normal operation)
38	TM6	I/O	Test pin (must be clamped to HIGH during normal operation)
17	TP2	O	Test pin

Slot Assignment

TM4	BURST	LT	SLOT0	SLOT1	SLOT2	Mode	SFR Marker on FSC
0	0	0	0	0	0	NT automode	no
0	0	0	0	1	0	TE automode	no
0	0	0	1	0	0	NT automode	yes
0	0	0	1	1	0	TE automode	yes
0	1	0	slot assignment			PBX automode	
0	1	1	slot assignment			LT automode	
1	0	0	0	0	0	NT transparent	no
1	0	0	0	1	0	TE transparent	no
1	0	0	1	0	0	NT transparent	yes
1	0	0	1	1	0	TE transparent	yes
1	1	0	slot assignment			PBX transparent	
1	1	1	slot assigment			LT transparent	

Time Slot No.	SLOT0	SLOT1	SLOT2	Bit No.
0	0	0	0	0..31
1	0	0	1	32..63
2	0	1	0	64..95
3	0	1	1	96..127
4	1	0	0	128..159
5	1	0	1	160..191
6	1	1	0	192..223
7	1	1	1	224..255

Interfaces of the IEC-Q

The specifications for the U interface with respect to layer-1 maintenance functions are based on the "T1 Basic Access Interface for Application at the Network Side of NT-Layer-1". The IOM-2 interface is described in the "ISDN Oriented Modular Interface Specification.

U Interface

Frame Structure

		FRAMING	2B+D	Overhead Bits (M1-M6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	atc / act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea / ps1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1 / ps2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1 / ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1 / cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3,...									

LT-to-NT direction — NT-to LT direction

"1" = reserve = reserve bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)

act = activation bit
ps1, ps2 = power status bits
ntm = Nt1 in test mode bit
crc = cyclic redundancy check
covers 2B+D & M4
febe = far end block error bit

2B1Q superframe technique & overhead bit assignments
(8x1.5 ms "basic frames" = 12 ms superframe)

Embedded Operation Channel (EOC)

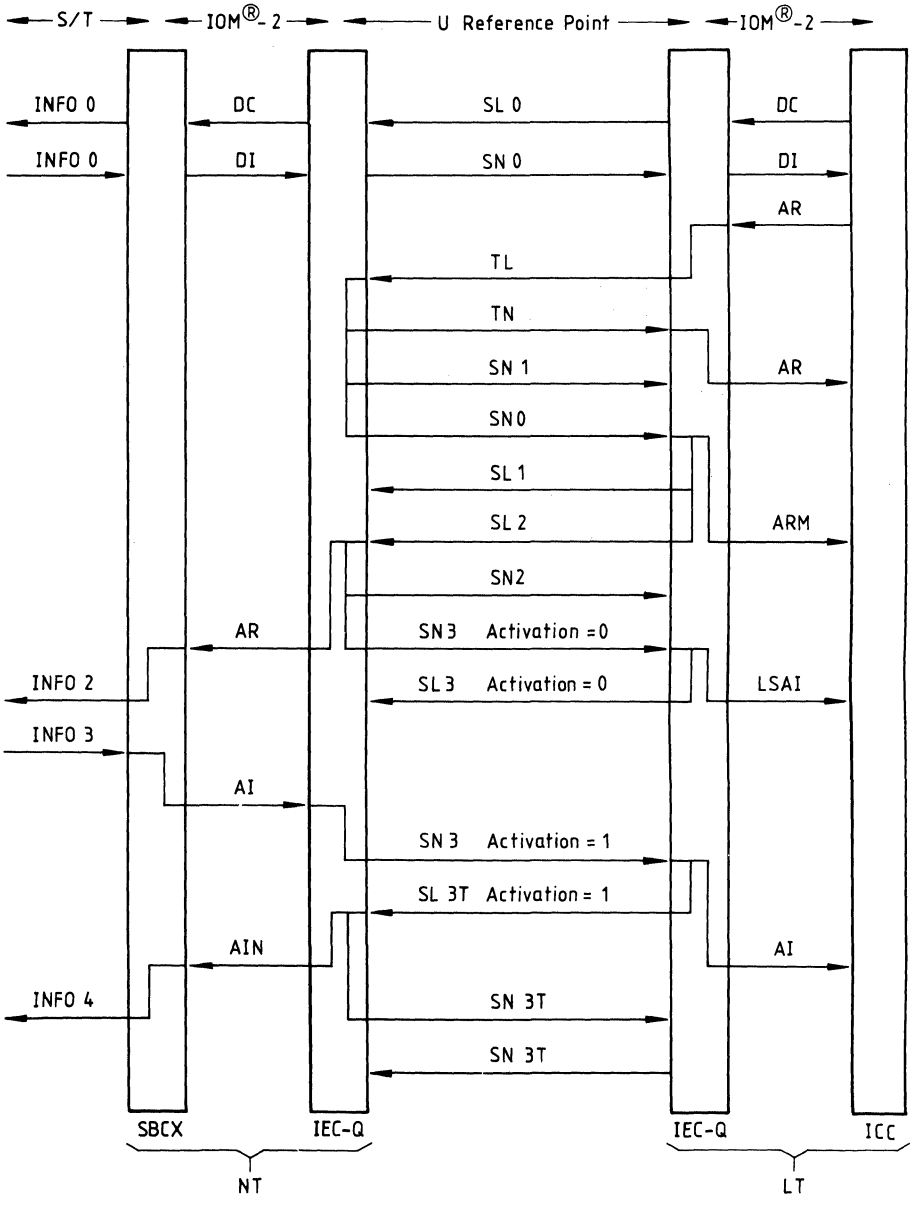
24 bits per superframe are allocated to an embedded operation channel supporting operation communication between network and NT. Two EOC frames of 12 bits are contained within a superframe:

$a_1 - a_3$	dm	$i_i - i_8$		(o) Origin. (d) Dest.		Message
Address Field	**Data/Msg Indicator**	**Info**	**Field**	**LT**	**NT**	
000						NT Address
111						Broadcast
	1					Message
	0					Data
		0101	0000	o	d	Operate 2B+D Loopback
		0101	0001	o	d	Operate B1 Loopback
		0101	0010	o	d	Operate B2 Loopback
		0101	0011	o	d	Request Corrupted CRC
		0101	0100	o	d	Notify of Corrupted CR
		1111	1111	o	d	Return to Normal
		0000	0000	d/o	o/d	Hold State
		1010	1010	d	o	Unable to Comply Acknowledgement

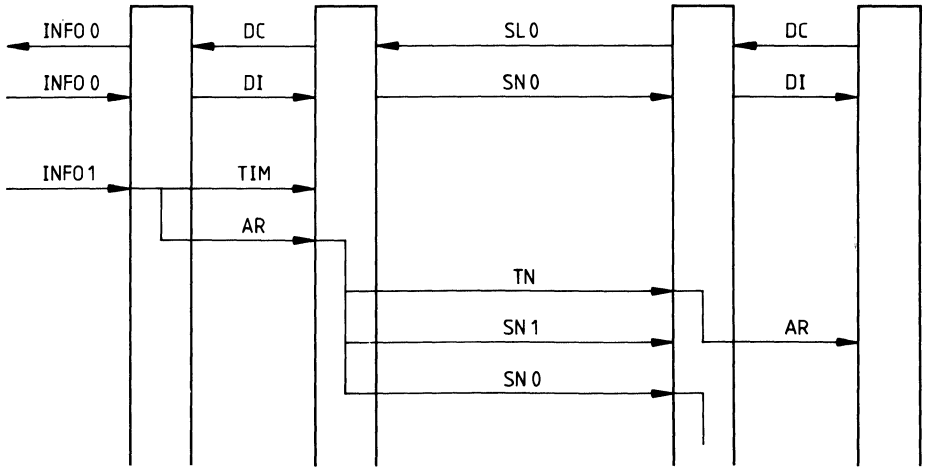
Activation and Deactivation Procedures

Activation occurs either by the LT or NT side.
Deactivation starts always from the LT side.

Activation from LT

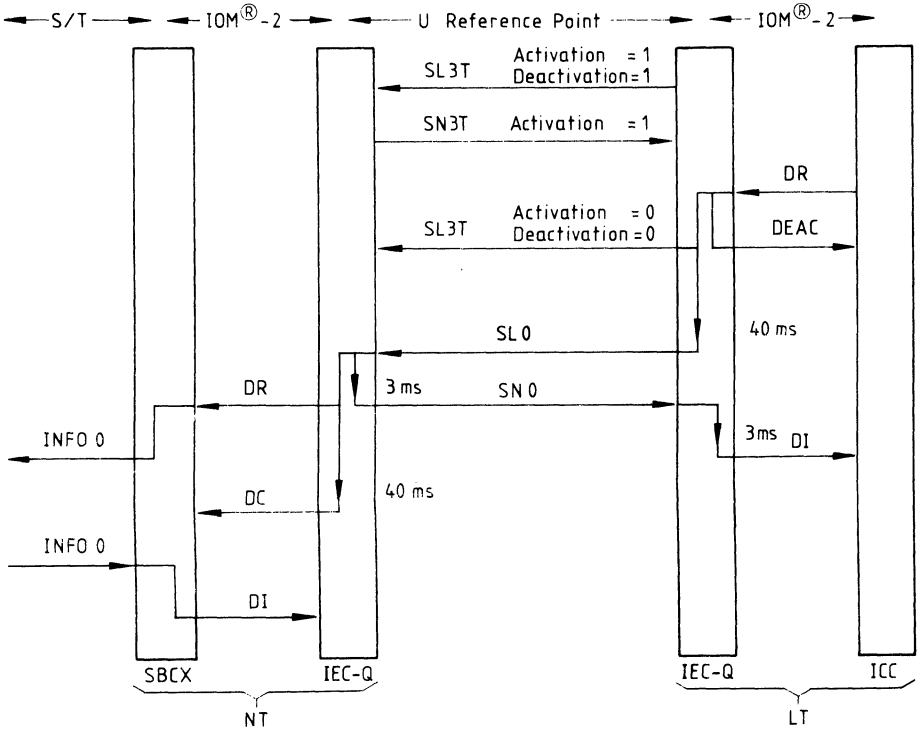


Activation from NT



the following as on previous page

Deactivation Procedure

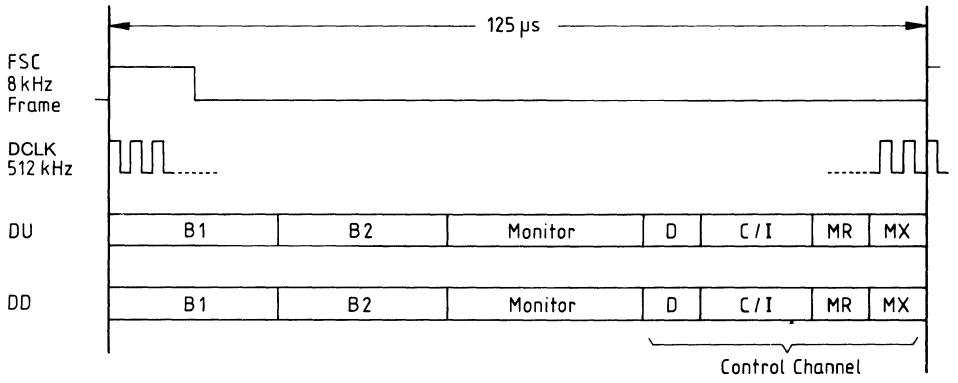


Signal	Synch Word	Super Frame	2B+D	M
TN	+−3	+−3	+−3	+−3
SN0	No Signal	No Signal	No Signal	No Signal
SN1	Present	Absent	1	1
SN2	Present	Absent	1	1
SN3	Present	Present	1	Normal
SN3T	Present	Present	Normal	Normal
TL	+−3	+−3	+−3	+−3
SL0	No Signal	No Signal	No Signal	No Signal
SL1	Present	Absent	1	1
SL2	Present	Present	0	Normal
SL3T	Present	Present	Normal	Normal

* TL/TN alternate +−3 for 10-kHz tone
* SN_x signal from NT to LT
* SL_x signal from LT to NT

The IOM-2 Interface

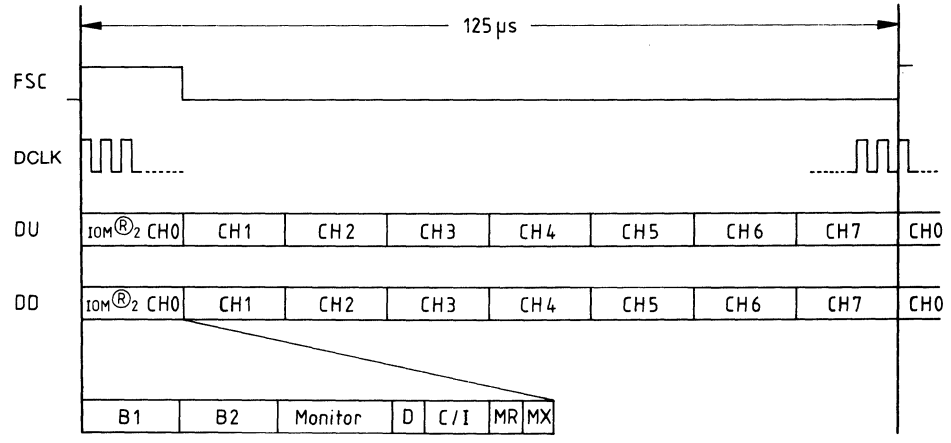
The Frame Structure of IOM-2



B1, B2: Circuit switched voice/data
D: D-channel for signaling and packet switched data
C/I: Command/indication bits for control
MR, MX: Monitor handshake bits

* DCL is programmable for values from 512 kHz to 8.192 MHz

Multiplexed Frame Structure of the IOM-2 Interface (shown for 2.048 kbit/s)



The IOM-2 Interface Monitor Channel

The monitor channel of the IOM-2 interface is designed for safe message oriented data transfer including rate adaption and synchronization features. The dedicated transfer procedure enables the link of several bytes to multi-byte message. For easy identification of the messages, each one starts with a four bit field indicating the structure of the following data. For ISDN basic access layer-1 maintenance four identifier codes are used within the IEC-Q:

MON-0	0 0 0 0	for U interface eoc message
MON-1	0 0 0 1	for S/T interface S1/Q messages and one part of U interface single maintenance bits.
MON-2	0 0 1 0	for the second part of U interface single maintenance bits and the S/T interface S2 channel
MON-8	1 0 0 0	for local messages

if unspecified codes are passed, their receipt is acknowledged, but disregarded by the chip.

EOC Messages on the IOM-2 Interface

The twelve bit eoc messages are transferred over the IOM interface in two monitor channel bytes according to the following structure (cf. T1 U interface specification)

MON-0

0 0 0 0 a a a d	e e e e e e e e

a: address, d: d/m bit, e: eoc command

This monitor message is transferred either only once and then handled autonomously by the device.

Code repetition is performed within the chip by EOC processor.

Only one pending command is allowed, i.e. one may pass (valid for MON- and EOC-channel).

Single Maintenance Bits of the U Interface on the IOM Interface

There are twelve single maintenance bits defined. Some of them have a relationship to the S/T interface such as NTM or FEBE, others are assigned to the layer-1 activation procedure. As a consequence, some are transferred with the identifier "0001" to link U and S/T interfaces maintenance functions, others are transferred separately:

MON-1

0 0 0 1 0 0 0 0	s s s s 1 – – m

s: S1/Q code, m: NTM polarity

S1/Q code	NT		LT	
	d	u	d	u
1 1 1 1		NORM	–	–
0 0 0 1	–	ST	–	–
0 0 1 0	STP	–	–	–
0 1 0 0	FEBE	–	–	–
1 0 0 0	NEBE	–	–	–
1 1 0 0	FNBE	–	–	–

d: Downstream (LT-TE), u: Upstream (TE-LT)

ST: Self test
STP: Self test pass
FEBE, NEBE, FNBE indicates block errors

MON-2

					M_{41}	M_{51}	M_{52}	M_{62}	M_{45}	M_{46}
0	1	1	0		M_{61}	M_{42}	M_{43}	M_{44}	M_{47}	M_{42}

Remaining M-bits (M_{xy}: M_x in frame y)

Local Messages

1	0	0	0	r	a	0	0	b	b	b	b	b	b	b	b

b: Local command

Possible local commands are:

RBEF: Read block error counter far end
RBEN: Read block error counter near end
RDi: Relay driver i activated
RECC: Read echo canceler coefficients
RID: Read identification
RPFC: Read power feed current value

The IEC-Q supplies the desired information in a two byte message with local address.

The IOM-2 Interface C/I Channel

C/I Channel Codes

Code	NT-Mode		LT-Mode	
	IN	OUT	IN	OUT
0000	TIM	DR	DR	–
0001	RES	–	RES	DEAC
0010	–	FJ	–	FJ
0011	–	–	LTD	HI
0100	SI1	EI1	RES1	EI1
0101	SSP	–	SSP	EI2
0110	DT	–	DT	INT
0111	–	PU	–	LSAI
1000	AR	AR	AR	AR
1001	–	–	–	ARM
1010	ARL	ARL	ARL	–
1011	–	–	–	–
1100	AI	AI	–	AI
1101	–	–	–	–
1110	–	AIL	–	–
1111	DI	DC	DC	DI

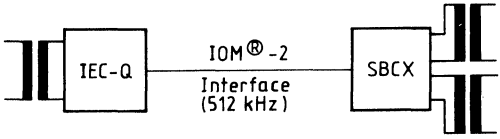
AIL	Activation Indication Local Loop
AI	Activation Indication
AR	Activation Request
ARL	Activation Request Local Loop
ARM	Activation Request Maintenance Bits
DC	Deactivation Confirmation
DR	Deactivation Request
DEAC	Deactivation Accepted
DI	Deactivation Indication
DT	Test Mode (Data Through)
EI1	Error Indication 1 (Error on U)
EI2	Error Indication 2 (Error on S/T)
HI	High Impedance (Set by Pin PFOFF)
INT	Interupt (Set by Power Controler)
LTD	LT Disable (Control of Pin DISS)
LSAI	Line System Activation Indication
RES	Circuit Reset
RES1	Receiver Reset
PU	Power Up
SSP	Test Mode (Send Single Pulses)
TIM	Timing Required

Application

Different hardware configurations as well as different operating modes of the device are selected to cope with different system requirements.

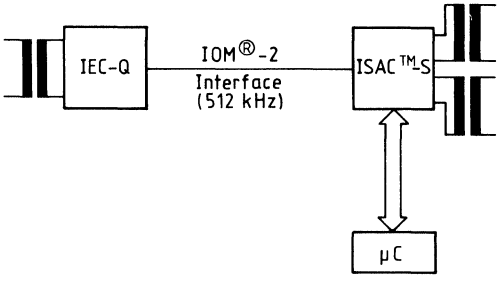
NT1 Mode

T1 S/T and U interface procedure specification by SBCX and IEC-Q



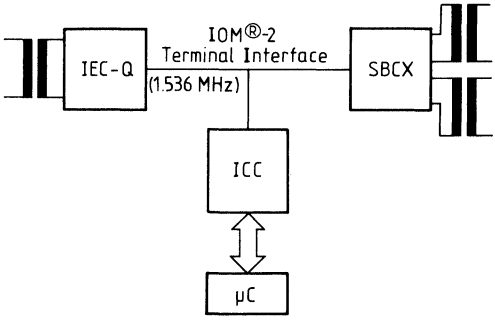
NT2 Mode

Using the ISAC-S together with the IEC-Q it is possible to handle all maintenance functions at the µC. The S1/Q bits are accessed directly in the specific ISAC™-S register, the U interface maintenance data are transferred via monitor channel to the µC. In this configuration, the IEC-Q can be programmed either in automode or in transparent mode.

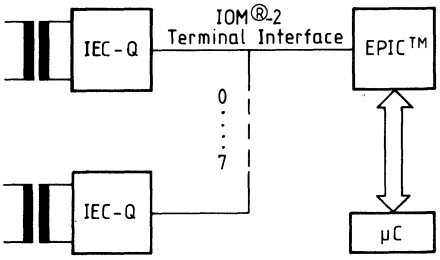


NT Mode, Handling the Complete S Channel

The SBCX is used to get access to the S channel. Since both SBCX and IEC-Q need a monitor channel for transfer of maintenance information to the ICC, a data clock of 1.536 MHz is required for the IOM interface (TE mode of IEC-Q). The SBCX occupies the monitor channel of the second IOM interface channel and runs in the transparent mode.



LT Line Termination in Public or Private Exchange or NT-PBX



The EPIC performs the control of voice, data and signaling for up to eight subscribers on digital line boards with one IOM-2 interface. Since every IEC-Q needs a monitor channel transfering maintenance information to the µP and a data-channel, a time-slot procedure with variable data clock up to 6.176 MHz is required. Each IEC-Q is assigned to one time and runs either in the auto-mode or in the transparent-mode.

Using the IDEC, Handling the D-Channel Protocol for up to Four Subscriber Lines.