SIEMENS

ISDN Subscriber Access Controller (ISAC-P) PEB 20950

Preliminary Data **CMOS IC**

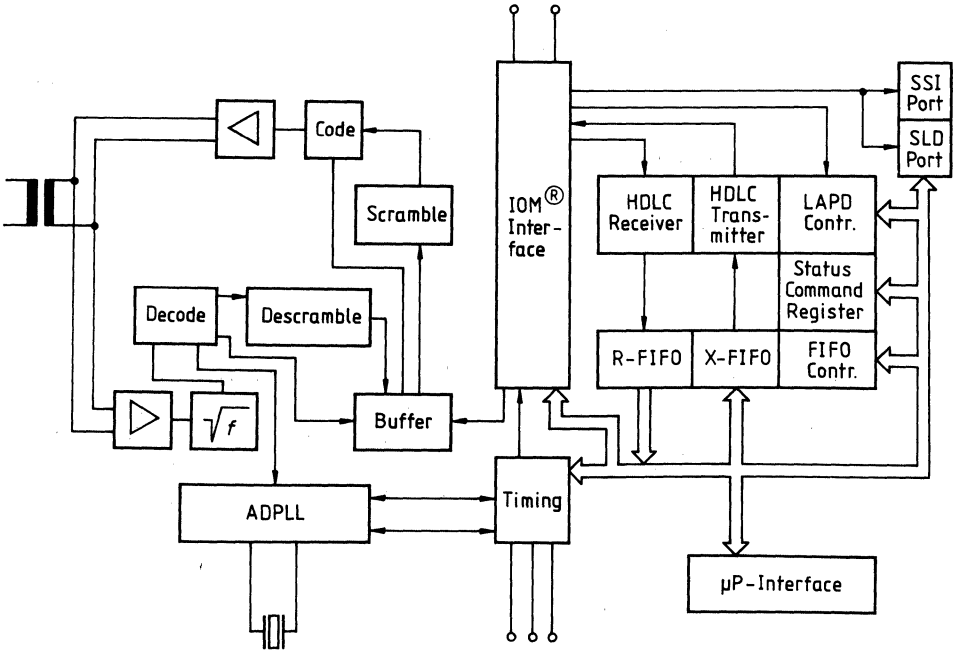
Type	Ordering Code	Package
PEB 20950-C	Q67100-H8613	C-DIP-40
PEB 20950-N	Q67100-H8614	PL-CC-44 (SMD)
PEB 20950-P	Q67100-H8550	P-DIP-40

The PEB 20950 ISAC™-P is a combination transceiver/HDLC controller for ISDN terminals in a two-wire PBX environment. Transceiver functions are performed according to the two-wire PBX industry standard U_{p0} interface. This corresponds to all of the functions available on the PEB 2095 IBC. Similarly, the HDLC protocol is processed as described for the PEB 2070 ICC. The ISAC-P represents both the IBC and ICC on a single IC.

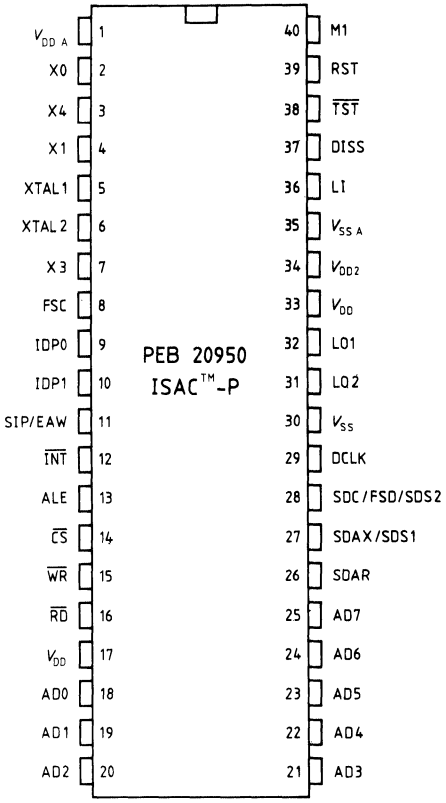
Features

- Half duplex burst mode two-wire transceiver
- AMI line code
- Adaptive line equalization
- High-level support of LAPD protocol
- FIFO buffer (2x64 bytes) for efficient transfer of D-channel packets
- IOM® interface to other ICs
- Switching of test loops
- 8-bit µP interface
- Advanced CMOS technology
- Low power consumption

ISAC-P Block Diagram



Pin Configuration **P-DIP; C-DIP**
(top view)



Pin Definitions and Functions

Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
1	V_{DD}	I	Analog power supply (+5 V)
2	X0	O	**Multifunctional Pin** M1 = 1: Software programmable output M1 = 0: 3.84-MHz clock output
3	X4	I/O	**Multifunctional Pin** M1 = 1: PFOFF M1 = 0: 2.56-MHz clock output
4	X1	O	**Multifunctional Pin** M1 = 1: 15.36-MHz clock output M1 = 0: 1.536-MHz clock output in IOM-1 mode; 768-kHz clock output in IOM-2 mode

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
5	XTAL1	I	**External Crystal** or external clock input
6	XTAL2	O	**External Crystal** output
7	X3	I	**Multifunctional Pin** M1 = 1: MPF input M1 = 0: $\overline{\text{ENCK}}$ input
8	FSC	I/O	**IOM Interface Frame Synchronization** M1 = 1: 8-kHz input clock M1 = 0: 8-kHz output clock
9	IDP0	I/O	**IOM Interface Data Port 0** LT application: Data upstream line TE application: Data downstream line
10	IDP1	I/O	**IOM Interface Data Port 1** LT application: Data downstream line TE application: Data upstream line
11	SIP/EAW	I/O	**SLD Interface Port,** IOM-1 mode This line transmits and receives serial data at standard TTL or CMOS level. External Awake, terminal specific functions If a falling edge on this input is detected, the ISAC-P generates an interrupt and/or a reset pulse
12	$\overline{\text{INT}}$	OD	**Interrupt Request** The signal is activated, when the ISAC-P requests an interrupt. The CPU may determine the particular source and cause of interrupt by reading the ISAC-P interrupt status register (ISTA, EXIR). $\overline{\text{INT}}$ is an open drain output, thus the interrupt request outputs of several ISAC-P's can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull up resistor.
13	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus, which will select one of the ISAC-P's internal registers. The address is latched with the falling edge of ALE.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
14	$\overline{CS}$	I	**Chip Select** A low signal selects the ISAC-P for a read/write operation.
15	$\overline{WR}$	I	**Write** This signal indicates a write operation. When $\overline{CS}$ is active, the ISAC-P loads an internal register with data provided via the address/data bus.
16	$\overline{RD}$	I	**Read** This signal indicates a read operation. When the ISAC-P is selected via $\overline{CS}$ the read signal enables the bus drivers to put data from an internal register on the address/data bus.
17	V_{DD}	I	Power supply (+5 V)
18 19 20 21 22 23 24 25	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address Data Bus** The multiplexed address data bus transfers data and command/status information between the ISAC-P and the µP system.
26	SDAR	I	**Serial Data Port A Receive** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open drain/open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
27	SDAX/ SDS1	O	**Serial Data Port A Transmit,** IOM-1 mode Transmit data is shifted out via this pin at standard TTL or CMOS level. **Serial Data Strobe 1,** IOM-2 mode A programmable strobe signal, selecting either one of two B/IC channels on IOM-2 interface, is supplied via this line. After reset SDAX/SDS1 remains at logical 0 until a write access to SPCR is made.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Symbol	Input (I)	Function
28	SCA/FSD SDS2	O	**Serial Clock Port A,** IOM-1 timing mode 0 A 128-kHz data clock signal for serial port A is supplied. **Frame Sync Delayed,** IOM-1 timing mode 1 A 8-kHz synchronization signal, delayed by 1/8 of a frame, for serial port B (IOM-1 interface) is supplied. In this mode a minimal delay for B1 and B2 channels is guaranteed. **Serial Data Strobe 2,** IOM-2 mode A programmable strobe signal, selecting either one or two B/IC channels on IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 remains at logical 0 until a write access to SPCR is made.
29	DCLK	I/O	**IOM Interface Data Clock** M1 = 1: input 512-kHz IOM-1 mode input 4.096-kHz IOM-2 mode M1 = 0: output 512-kHz IOM-1 mode output 1.536-MHz IOM-2 mode
30	V_{SS}	I	Ground (0 V)
31	LO2	O	**Line Transmitter Output**
32	LO1	O	**Line Transmitter Output**
33	V_{DD}	I	Power supply (+5 V)
34	V_{DD2}	O	2.5 V output; connected to both V_{DD} and V_{SS} via 10 nF capacitor.
35	V_{SSA}	I	Analog ground (0 V)
36	LI	I	**Line Receiver Input**
37	DISS	O	**Disable Supply Indication**
38	$\overline{TST}$	I	**Device Test Pin:** tie always high
39	RES	I/O	**RESET** A high signal on this input forces the ISAC-P into reset state. The minimum pulse length is four clock periods of DCLK. If the terminal specific functions are enabled, the ISAC-P may also supply a reset signal.
40	M1	I	**Operating Mode for IBC-Part.** M1 = 1: IBC in LT mode M1 = 0: IBC in TE mode