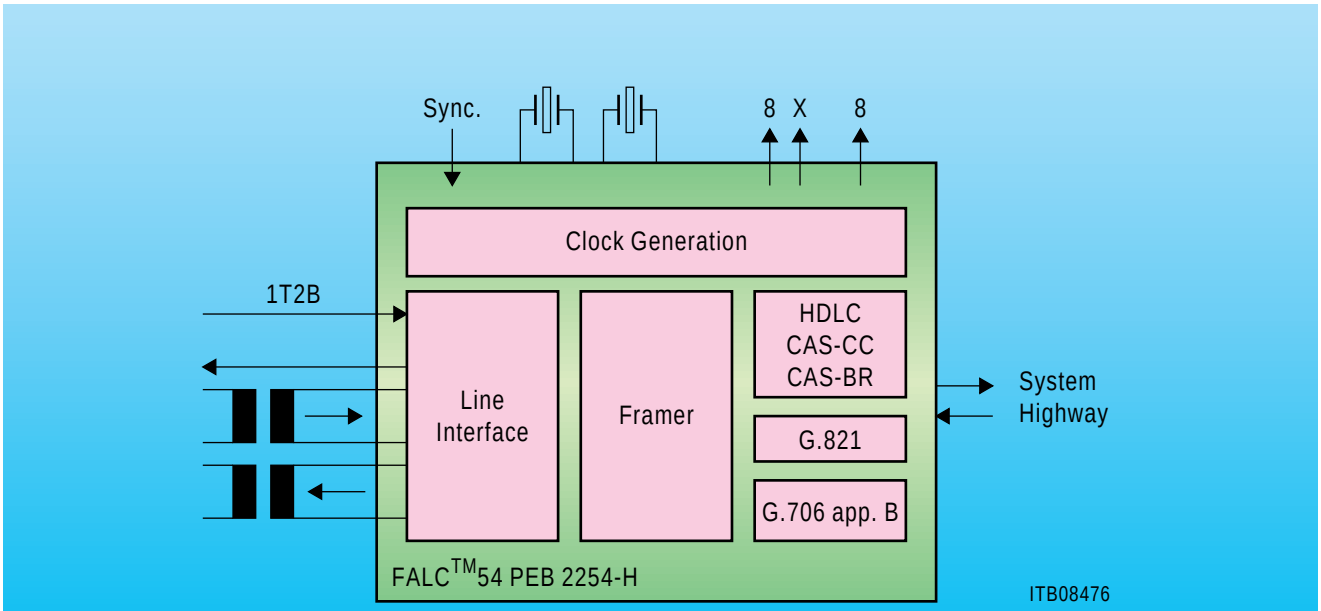
General Description

The Frame and Line Interface Component PEB 2254 (FALC54) is a high sophisticated single-chip solution for primary rate PCM carriers., It may be programmed to operate in either 1.544 Mbit/s (T1) or 2.048 Mbit/s (CEPT) carrier systems. The FALC54 provides the complete functionality of a line interface, a framer, clock generation (2 VCOs) and signaling unit on one chip with greatly increased functionalities. The FALC functions include selectable multiframe, error checking, multiple line codes, alarm reporting, maintenance and performance monitoring. All signaling types are controlled by either the integrated CAS-signaling controller or the integrated HDLC controller. Furthermore, the FALC54 allows flexible access to facility data link and service channels. Controlling and monitoring of the devices is performed via a Siemens/Intel/Motorola compatible 8/16-bit data bus.

Type	Package
PEB 2254-H	P-MQFP-80-1 (SMD)

Features

- Covers both standards E1 and T1
- On-Chip Line Interface including Data & Clock Recovery
- On-Chip CAS-CC/CAS-BR Signaling Controller
- On-Chip HDLC Controller (LAPD, F/DL, Sa-bit data)
- On-Chip System Clock Generation Unit
- Meets CCITT, ETSI and AT&T Requirements for use in systems that are compliant with:
  AT&T CB119, TR-NWT-499, ANSI T1.406, CCITT G.703, G.704, G.706, G.732, G.735-9, G.775, G.823-4, I.431, ETS 300233, V5.1 Interface, V5.2 Interface
- 8-/16-bit microprocessor interface, Siemens/Intel/Motorola compatible
- Performance Monitoring support (16-bit error counters, 1 second timer)
- JTAG-boundary scan interface
- P-MQFP-80 package



Block Diagram