Advanced Information

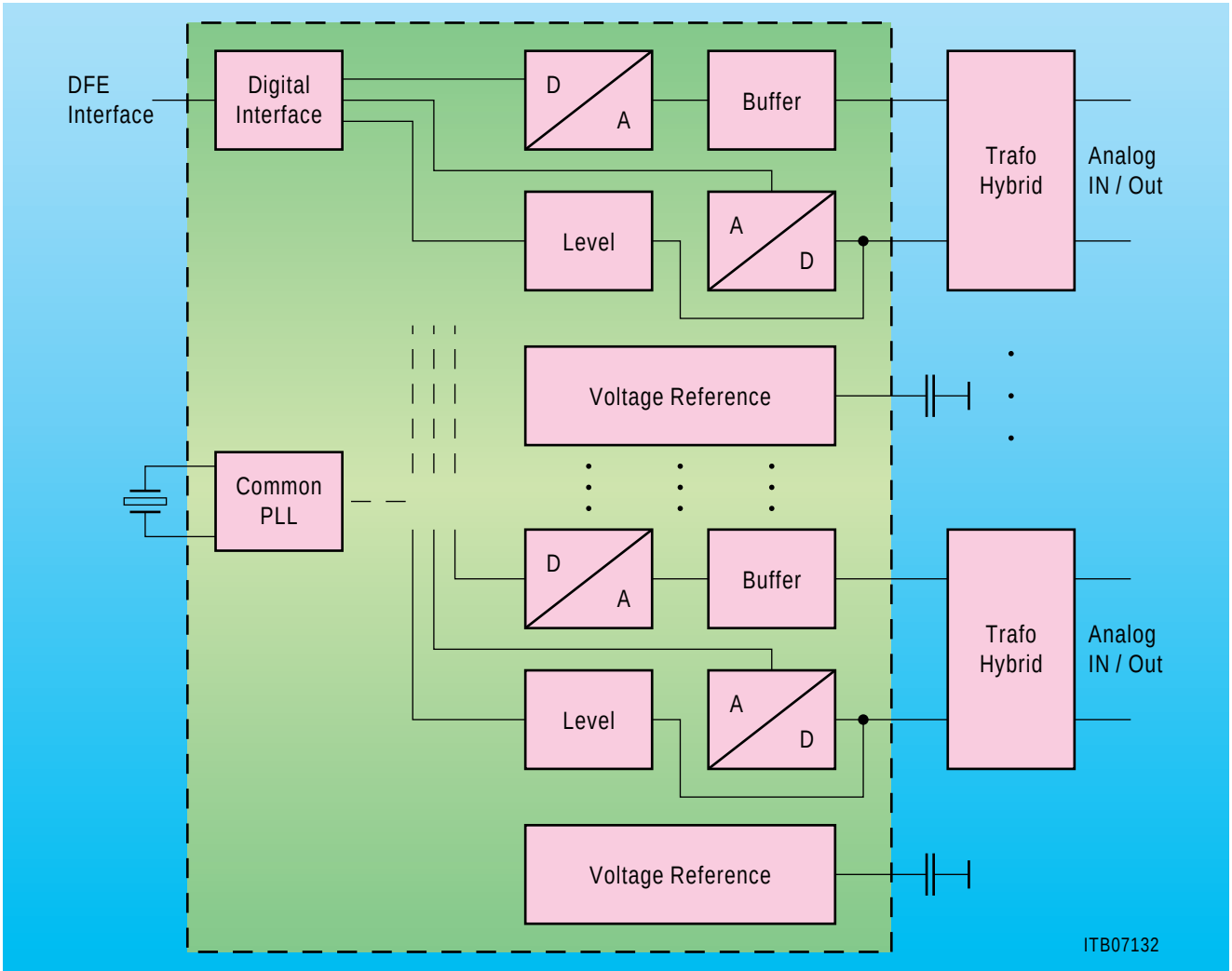
General Description

The PEB 24902 Quad IEC AFE (Quadruple ISDN Echocancellation Circuit Analog Front End) is part of a 2B1Q or 4B3T ISDN U-transceiver chip set. Up to four lines can be accessed simultaneously by the Quad IEC AFE. The Quad IEC AFE is optimized to work in conjunction with the PEB 24901 Quad IEC DFE-T and the PEB 24911 Quad IEC DFE-Q. An integrated PLL synchronizes the 15.36-MHz master clock onto the 8-kHz or 2048-kHz PTT clock. This specification describes the functionallity for 2B1Q and 4B3T interfaces.

Type	Package
PEB 24902	P-MQFP-64-1 (SMD)
PEF 24902	P-MQFP-64-1 (SMD)

Features

- Digital to analog conversion (transmit pulse)
- Output buffering
- Analog to digital conversion
- Detection of signal on the line
- Master clock generation by PLL
- P-MQFP-64 package
- Compliant to ANSI T1.601 (1992), ETSI ETR 080 (1995)
- JTAG-boundary scan path compliant to IEEE 1149.1
- Extended temperature range – 40 °C to 85 °C available (PEF 24902)



Block Diagram