SIEMENS

ICs for Communications

ISDN PC Adapter Circuit
IPAC

PSB 2115 Version 1.1

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PSB 2115		
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1 Overview

The ISDN PC Adapter Circuit IPAC integrates all necessary functions for a host based ISDN access solution on a single chip.

It includes the S-transceiver (Layer 1), an HDLC controller for the D-channel and two protocol controllers for each B-channel. They can be used for HDLC protocol or transparent access. The system integration is simplified by several host interface configurations selected via pin strapping. They include multiplexed and demultiplexed interface options as well as the optional indirect register access mechanism which reduces the number of necessary registers in the address space to 2 locations.

The IPAC combines the functions of the ISDN Subscriber Access Controller (ISAC-S PEB 2086) and the High-Level Serial Communications Controller Extended for Terminals (HSCX-TE PSB 21525) providing additional features and enhanced functionality.

The FIFO size of the B-channel buffers is 2x64 bytes per direction. The S-transceiver supports other terminal relevant operation modes like line termination subscriber side (LT-S) and line termination trunk side (LT-T). A multi-line ISDN solution to support both S and U (2B1Q) line coding is simplified as well as multi-line solution with up to 3 S-interfaces.

An auxiliary I/O port has been added with interrupt capabilities on two input lines. These I/O lines may be used to connect a DTMF receiver or other peripheral components to the IPAC which need software control or have to forward status information to the host. Peripheral data controllers can transfer data on a PCM interface which is mapped into the B-channels on the IOM-2 interface.

A dedicated LED output indicates the activation status of the S-interface.

The IPAC is produced in advanced CMOS technology.

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ISDN PC Adapter Circuit　　　　　　　　　　　　　　　　　　　　**PSB 2115**
IPAC

Version 1.1　　　　　　　　　　　　　　　　　　　　　　　　　　　　**CMOS**

1.1　　　Features

- Single chip host based ISDN solution
- Integrates S-transceiver, D-channel, B-channel protocol controller
- Replaces solutions based on ISAC-S PEB 2086 and HSCX-TE PSB 21525
- Easy adjustment of software using ISAC-S and HSCX-TE
- Various types of protocol support depending on operating mode (Non-auto mode, transparent mode)
- Efficient transfer of data blocks from/to system memory by DMA or interrupt request
- Enlarged FIFO buffers for B-channels (2x64 byte)
- S-transceiver with TE, LT-S and LT-T modes
- D-channel access mechanism in LT-S mode
- Additional I/O interface with 2 interrupt inputs
- PCM interface for non IOM-2 compatible peripheral data controllers
- Reduced register address space due to indirect address mode option
- Programmable timer (1 ... 63 ms) for continuous or single interrupts
- 3 programmable LED outputs, one is capable to indicate S bus activation status automatically
- 8-bit multiplexed or demultiplexed bus interface
- Siemens/Intel or Motorola μP interface
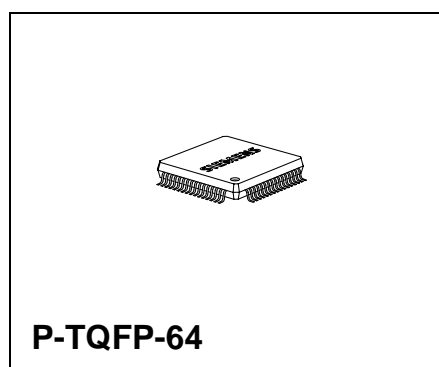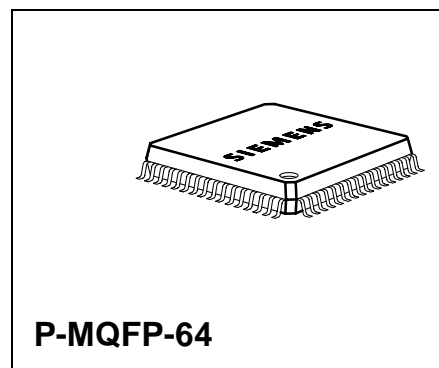
P-MQFP-64

P-TQFP-64

Type	Ordering Code	Package
PSB 2115 H		P-MQFP-64 (SMD)
PSB 2115 F		P-TQFP-64 (SMD)

1.2 Logic Symbol

The logic symbol shows all functions of the IPAC. It must be noted, that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a " * " are multiplexed and not available in all modes.
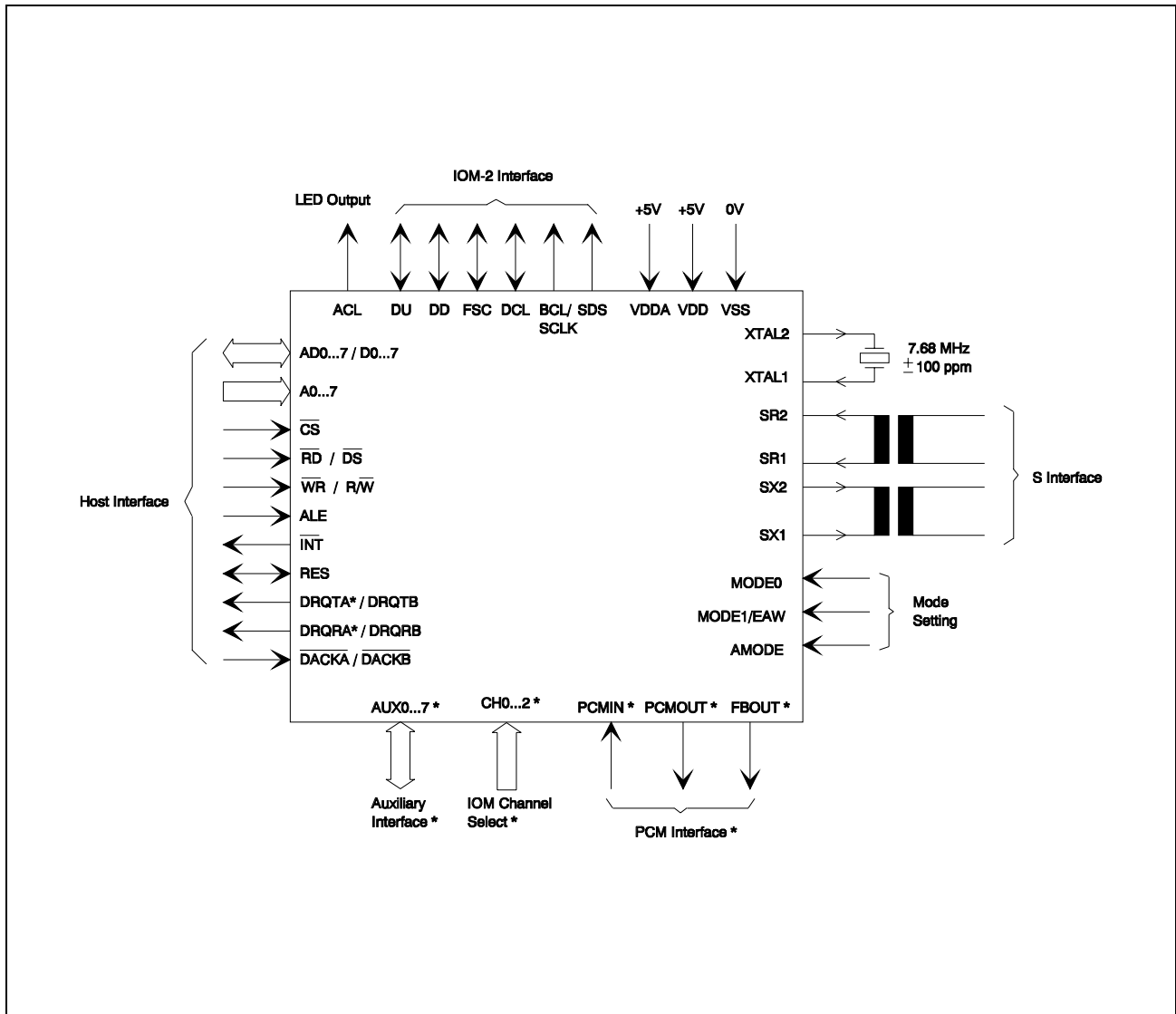

Figure 1
Logic Symbol

1.3   Pin Definitions and Functions

Table 1
Microprocessor Bus Interface

Pin No.	Symbol	Input (I) Output (O)	Function
	AD0-7 D0...7	I/O I/O	**Multiplexed Bus Mode:** **Address/data bus** Transfers addresses from the host system to the IPAC and data between the host system and the IPAC. **Non-Multiplexed Bus Mode:** **Data bus.** Transfers data between the host system and the IPAC.
	A0-A7	I	**Non-Multiplexed Bus Mode:** Address bus transfers addresses from the host system to the IPAC. For indirect address mode only A0 is valid. **Multiplexed Bus Mode** Not used in multiplexed bus mode.
	AMODE	I	**Address Mode** Selects between direct and indirect register access. A high selects indirect address mode and a low selects the direct register access.
	$\overline{\text{RD}}$ $\overline{\text{DS}}$	I I	**Read** Indicates a read access to the registers (Intel bus mode). **Data Strobe** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
	$\overline{\text{WR}}$ R/$\overline{\text{W}}$	I I	**Write** Indicates a write access to the registers (Intel bus mode). **Read/Write** A high level identifies a valid host access as a read operation and a low level identifies a valid host access as a write operation (Motorola bus mode).
	$\overline{\text{CS}}$	I	**Chip Select** A low on this line selects the IPAC for a read/write operation.

Table 1
Microprocessor Bus Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus (multiplexed bus type only). ALE also selects the microprocessor interface type (multiplexed or non multiplexed).
	$\overline{\text{INT}}$	OD	**Interrupt Request** This signal is activated when the IPAC requests an interrupt. It is an open drain output.
	RES	I/O	**Reset** A HIGH on this input forces the IPAC into a reset state. The minimum pulse length is four DCL-clock periods or four ms. If the terminal specific functions are enabled, the IPAC may also supply a reset signal.
	DRQTB	O	**DMA Request Transmitter** (channel B) The transmitter of the IPAC requests DMA data transfer by activating this line. The DRQTB remains high as long as the transmit FIFO requires data transfer. The amount of data bytes to be transferred from system memory to the IPAC (= byte count) must be written first to the XBCH, XBCL register. Always blocks of data (n x 64 bytes + REST, n=0, 1, ..) are transferred till the byte count is reached. DRQTB is deactivated immediately following the falling edge of the last $\overline{\text{WR}}$ cycle. Note: To support DMA for channel A, the DRQTA line is available in TE mode only (see pin AUX0).

Table 1
Microprocessor Bus Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
	DRQRB	O	**DMA Request Receiver** (channel B) The receiver of the IPAC requests DMA data transfer by activating this line. The DRQRB remains high as long as the receive FIFO requires data transfer, thus always blocks of data (64, 32, 16, 8 or 4 bytes) are transferred. DRQRB is deactivated immediately following the falling edge of the last read cycle. Note: To support DMA for channel A, the DRQRA line is available in TE mode only (see pin AUX1).
	$\overline{\text{DACKA}}$ $\overline{\text{DACKB}}$	I	**DMA Acknowledge** (channel A/B) When low, this input signal from the DMA controller indicates to the IPAC, that the requested DMA cycle controlled via DRQTA/B and DRQRA/B is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either read or write). Together with $\overline{\text{RD}}$, if DMA has been requested from the receiver, or with $\overline{\text{WR}}$, if DMA has been requested from the transmitter, this input works like $\overline{\text{CS}}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel. If $\overline{\text{DACKA/B}}$ is active, the input on pins A0-7 is ignored and the FIFO's are implicitly selected. If the $\overline{\text{DACKA/B}}$ signals are not used, these pins must be connected to VDD.
	MODE0	I	**Mode 0 Select** A LOW selects TE-mode and a HIGH selects LT-T and LT-S mode (see MODE1/EAW).
	MODE1	I	**Mode 1 Select / External Awake** The pin function depends on the setting of MODE0. If MODE0=1: **Mode 1 Select** A LOW selects LT-S mode and a HIGH selects LT-T mode.
	EAW	I	If MODE0=0: **External Awake** If a falling edge on this input is detected, the IPAC generates an interrupt and, if enabled, a reset pulse.

Table 1
Microprocessor Bus Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
	AUX0	I/O	**Auxiliary Port 0** **TE Mode: DRQTA (output)** **DMA Request Transmitter** (channel A) The transmitter of the IPAC requests DMA data transfer by activating this line. The DRQTA remains high as long as the transmit FIFO requires data transfer. The amount of data bytes to be transferred from system memory to the IPAC (= byte count) must be written first to the XBCH, XBCL register. Always blocks of data (n x 64 bytes + REST, n=0, 1, ..) are transferred till the byte count is reached. DRQTA is deactivated immediately following the falling edge of the last $\overline{WR}$ cycle. **LT-T/LT-S Mode: CH0 (input)** **IOM-2 Channel Select 0** Together with CH1 (pin AUX1) and CH2 (pin AUX2), this pin selects one of eight channels on the IOM-2 interface.
	AUX1	I/O	**Auxiliary Port 1** **TE Mode: DRQRA (output)** **DMA Request Receiver** (channel A) The receiver of the IPAC requests DMA data transfer by activating this line. The DRQRA remains high as long as the receive FIFO requires data transfer, thus always blocks of data (64, 32, 16, 8 or 4 bytes) are transferred. DRQRA is deactivated immediately following the falling edge of the last read cycle. **LT-T/LT-S Mode: CH1 (input)** **IOM-2 Channel Select 1** Together with CH0 (pin AUX0) and CH2 (pin AUX2), this pin selects one of eight channels on the IOM-2 interface.

Table 1
Microprocessor Bus Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
	AUX2	I/O	**Auxiliary Port 2** **TE Mode: AUX2 (input/output)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **LT-T/LT-S Mode: CH2 (input)** **IOM-2 Channel Select 2** Together with CH0 (pin AUX0) and CH1 (pin AUX1), this pin selects one of eight channels on the IOM-2 interface.
	AUX3	I/O	**Auxiliary Port 3** **TE-Mode: AUX3 (input/output)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **LT-T/LT-S Mode: FBOUT (output)** **FSC/BCL Output** This pin is programmable to output either an FSC clock which is derived from the DCL input divided by 192 (in LT-T: SCLK output provides 1.536 MHz) or a single bit clock from the IOM-2 interface, especially to serve non IOM-2 compatible peripheral devices on the PCM interface. If the PCM interface is switched off, this pin has the same functionality as in TE mode.
	AUX4	I/O	**Auxiliary Port 4** **TE-Mode: AUX4 (input/output)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **LT-T/LT-S Mode: PCMIN (input)** **PCM Data Input** On this line the IPAC receives 8-bit data, which is transmitted from a peripheral device. This data is mapped to a B-channel timeslot on IOM-2. If the PCM interface is switched off, this pin has the same functionality as in TE mode.

Table 1
Microprocessor Bus Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
	AUX5	I/O	**Auxiliary Port 5** **TE-Mode: AUX5 (input/output)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **LT-T/LT-S Mode: PCMOUT (output)** **PCM Data Output** On this line the IPAC transmits 8-bit data, which is received by a peripheral device. This data is taken from a B-channel timeslot on IOM-2. If the PCM interface is switched off, this pin has the same functionality as in TE mode.
	AUX6/7	I/O	**Auxiliary Port 6/7** **All Modes: INT0/1** These pins are programmable as general input/output. The state of the pins can be read from (input) / written to (output) a register. Additionally, as inputs they can generate a maskable interrupt to the host, which is either edge or level triggered. As outputs an LED can directly be connected to these pins.
	$\overline{\text{ACL}}$	O	**Activation LED** This pin can either function as a programmable output or automatically indicate the activated state of the S interface. An LED can directly be connected to $\overline{\text{ACL}}$.
	SX1 SX2	O O	**S-Bus Transmitter Output** Differential output for the S-transmitter. positive negative
	SR1 SR2	I I	**S-Bus Receiver Input** Differential inputs for the S-receiver.
	FSC	I/O	**Frame Sync** Synchronization signal. The rising edge indicates the begin of the IOM frame.

Table 1
Microprocessor Bus Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
	DCL	I/O	**Data Clock** IOM clock signal of twice the IOM data rate. Rising edge is used to transmit data, 2nd falling edge is used to sample data.
	DU	I/O(OD)	**Data Upstream** IOM data signal in upstream direction.
	DD	I/O (OD)	**Data Downstream** IOM data signal in downstream direction.
	BCL/ SCLK	O	**Bit Clock/S-clock** **TE-Mode:** Bit clock output. Clock identical to IOM data rate **LT-T Mode:** 1.536 MHz output synchronous to S-interface.
	SDS	O	**Serial Data Strobe** Programmable strobe signal, selecting either one or two B or IC channels (8 or 16 bit) on the IOM-2 interface.
	XTAL1	I	**Oscillator Input** Input pin of oscillator or input from external clock source. 7.68 MHz crystal or clock required.
	XTAL2	O	**Oscillator output** Output pin of oscillator. Not connected if external clock source is used.
	VDD	I	Supply Voltage +5V (+/- 10%)
	VDDA	I	Supply voltage +5V (+/- 5%)
	VSS	I	GND

Note: OD = Open Drain

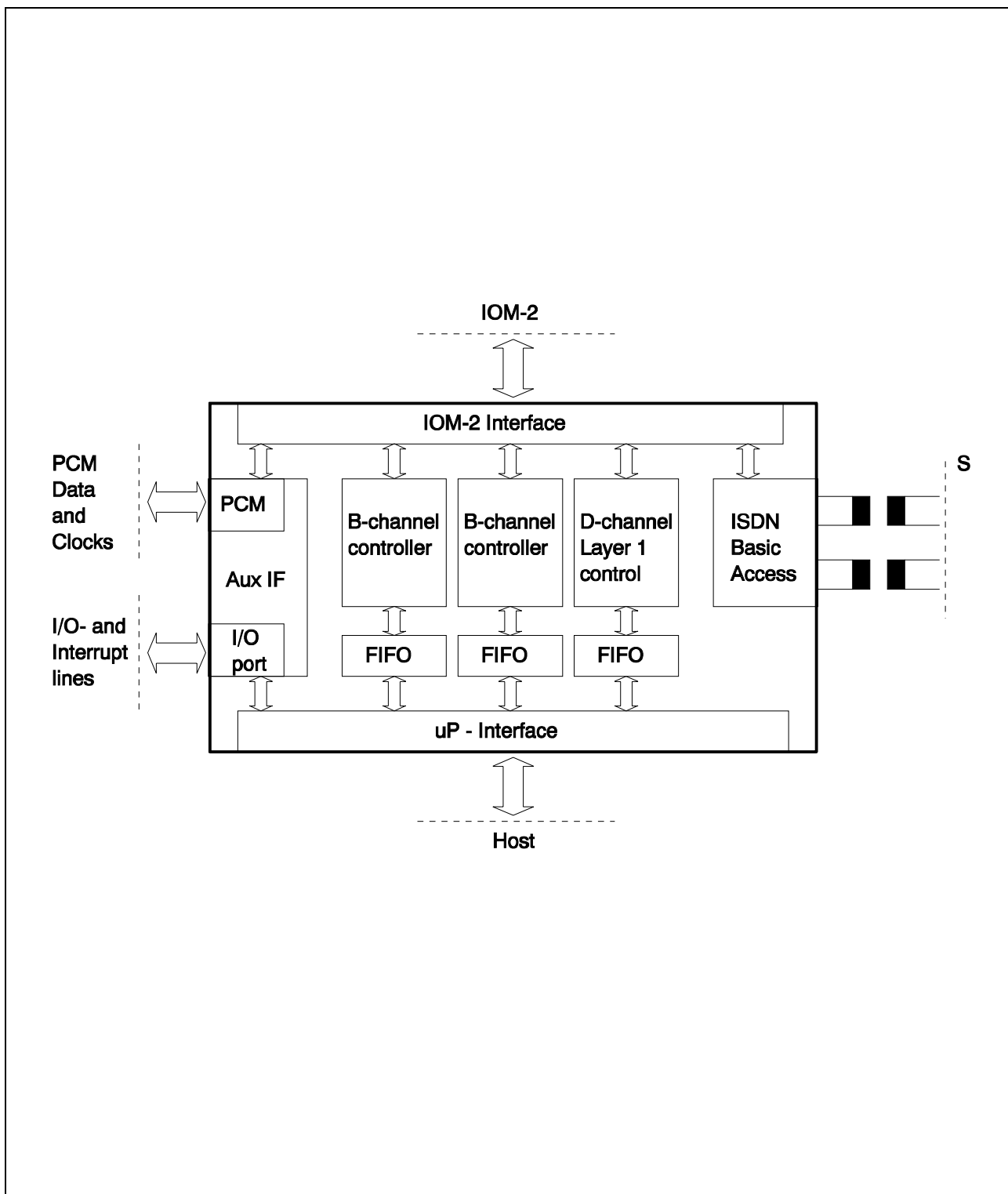## 1.4 Functional Block Diagram

Figure 2
Block Diagram

1.5   System Integration

The IPAC is suited for all host based applications.

ISDN PC Adapter Card for S Interface

An ISDN adapter card for a PC is built around the IPAC using an ISA or PCI interface device depending on the PC interface (figure 3). The IPAC can be connected to any bus interface logic and since it provides the possibility of a one-device terminal architecture, interfacing directly to the printer port applications is rather easy.
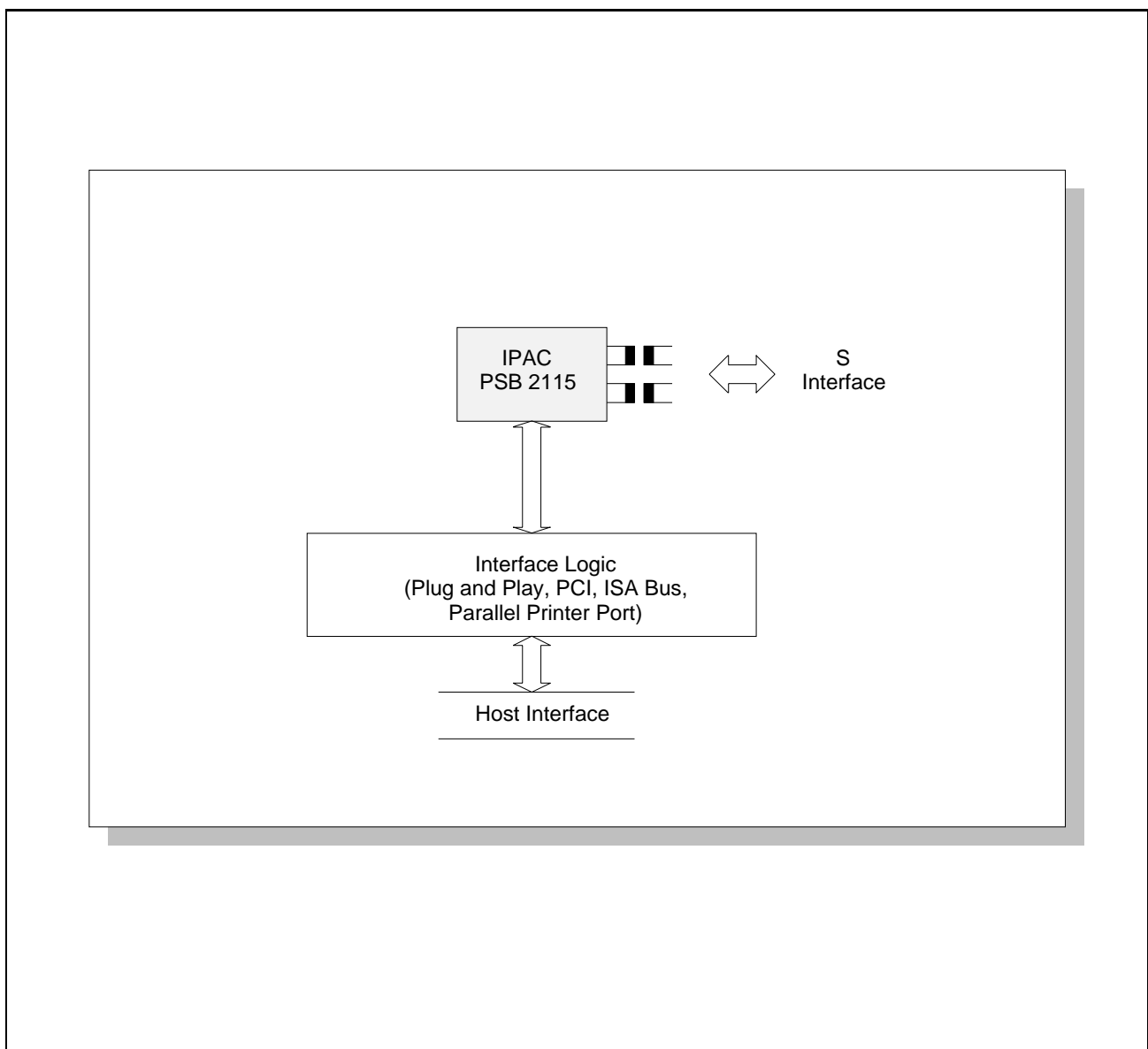
Figure 3
ISDN PC Adapter Card for S Interface

ISDN PC Adapter Card for U or S Interface

An ISDN adapter card which supports both U and S interface may be realized using the IPAC together with the PSB 2091 IEC-Q (figure 4). The S interface may be configured for TE or LT-S mode supporting intelligent NT configurations.
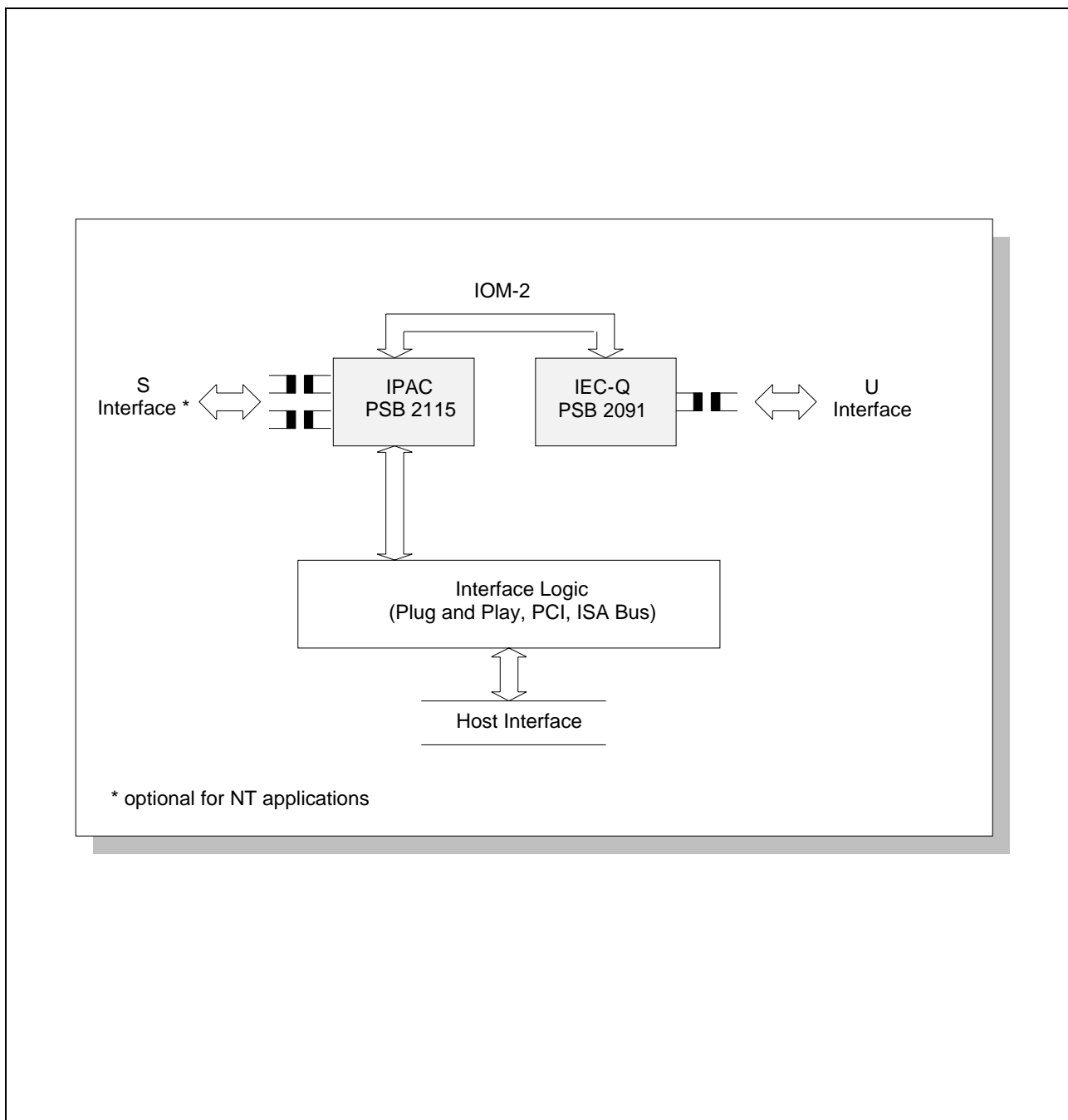

Figure 4
ISDN PC Adapter Card for U or S interface

ISDN Voice/Data Terminal

Figure 5 shows a voice data terminal developed on a PC card, where the IPAC provides its functionality as data controller + S interface within a two chip solution. During ISDN calls the ARCOFI-SP PSB 2163 provides for speakerphone functions and includes a DTMF generator. Additionally, a DTMF receiver or keypad may be connected to the auxiliary interface of the IPAC.
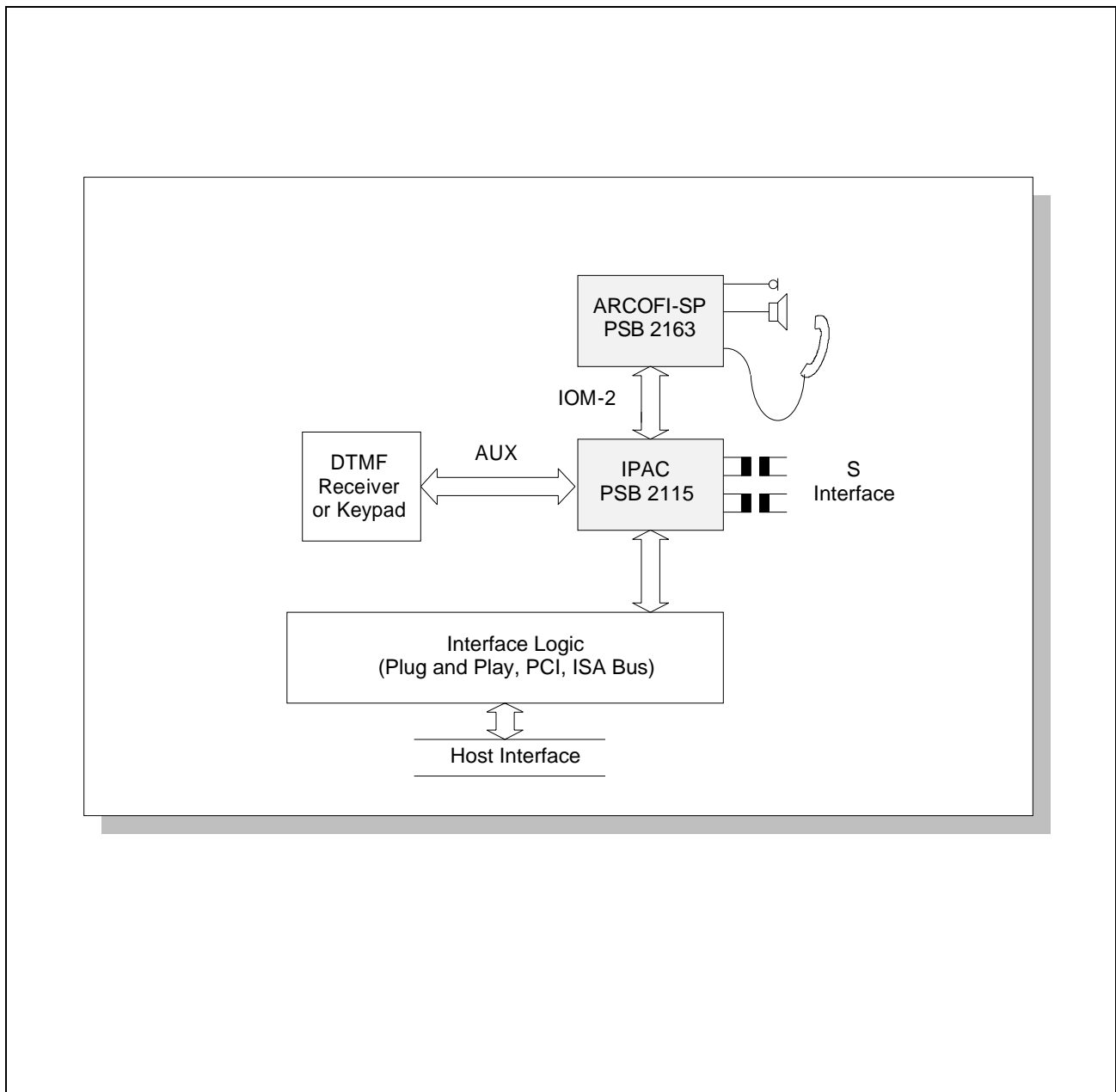

Figure 5
ISDN Voice/Data Terminal

ISDN Standalone Terminal with POTS interface

The IPAC can be integrated in a microcontroller based standalone terminal (figure 6) that is connected to the communications interface of a PC. The ARCOFI-BA PSB 2161 enables connection of analog terminals (e.g. telephones or fax) to the POTS interface.
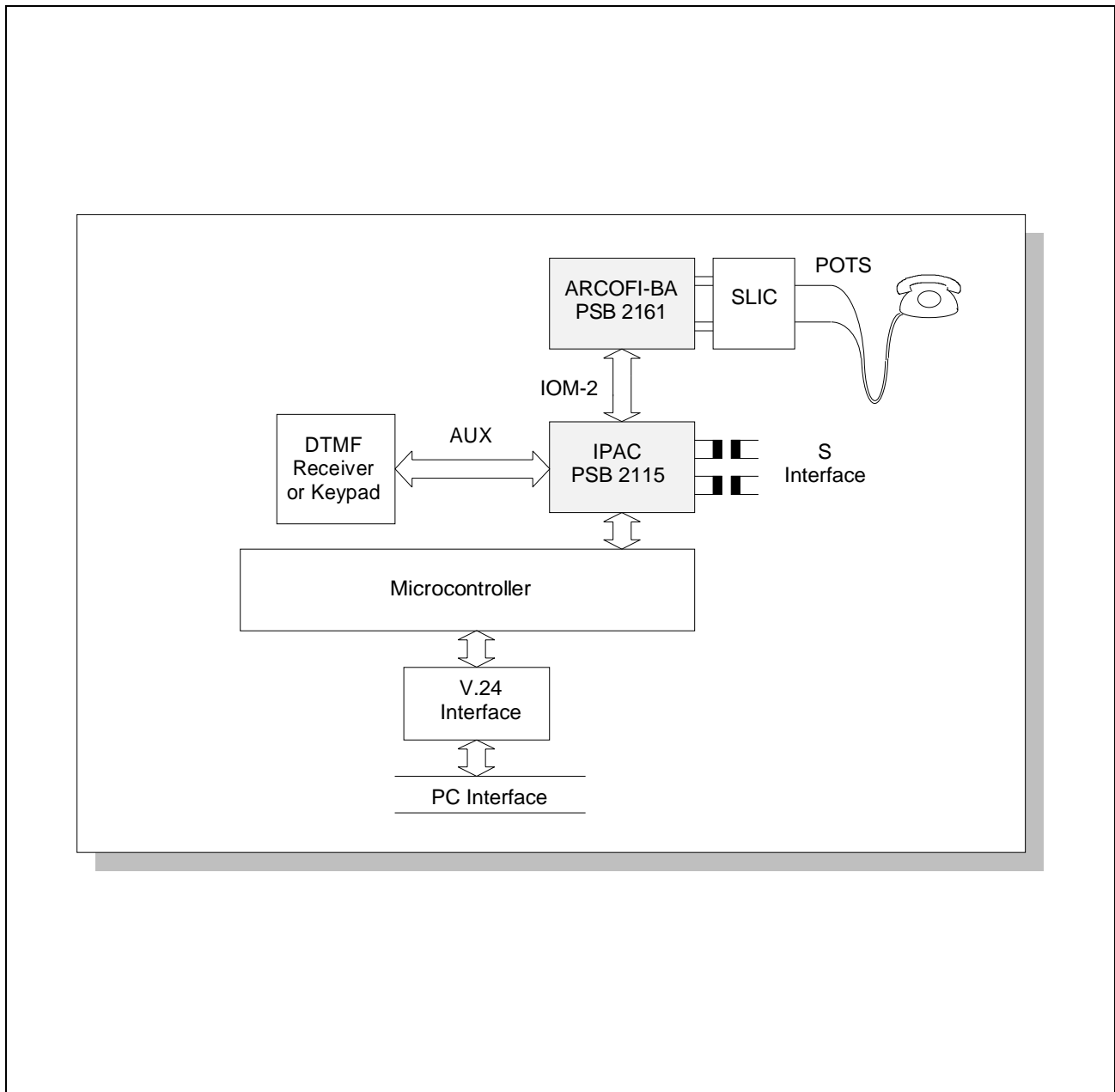

Figure 6
ISDN Standalone Terminal with POTS interface

Multiline PC-Adapter

Up to three S-interfaces can be combined using one IOM interface (figure 7). All three IPACs are configured for LT-T mode in different channels. The SCLK output is used for DCL clock and the FSC clock is generated by one device.
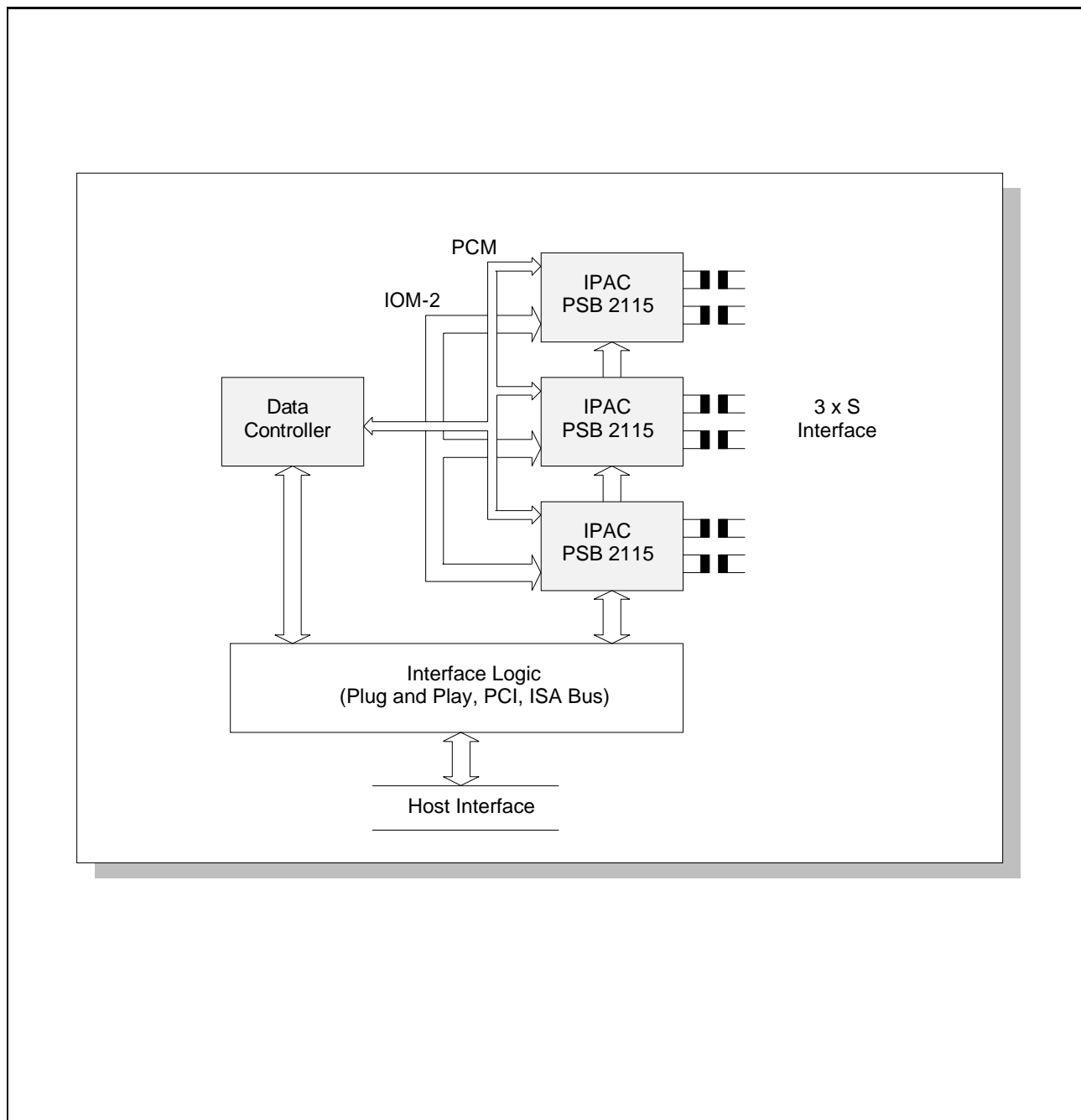

Figure 7
Multiline PC-Adapter

2 Functional Description

The ISDN PC Adapter Circuit IPAC combines functionality which is well known from ISAC-S PEB 2086 and HSCX-TE PSB 21525. Most of the functions of both devices are integrated on the IPAC with further modifications and improvements on certain features.

2.1 Operating Modes

The HDLC controller of each B channel can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be effected in a very flexible way, which satisfies most requirements.

There are 4 different operating modes which can be set via the MODE register.

- Non-Auto Mode (MODE: MDS1, MDS0 = 01)
- Transparent Mode 1 (MODE: MDS1, MDS0, ADM = 101)
- Transparent Mode 0 (MODE: MDS1, MDS0, ADM = 100)
- Extended Transparent Modes 0; 1 (MODE: MDS1, MDS0 = 11)

The S-transceiver supports terminal mode (TE), line termination subscriber side mode (LT-S) and line termination trunk side mode (LT-T). The selection is performed by two mode pins (see table 2), additionally the B-channel receive and transmit data paths are switched to DU or DD line depending on the mode (figure 8). In other words, the DU line always carries data which is transferred from the subscriber to the central office and the DD line carries data which comes from the central office to the subscriber. Therefore the direction of DU and DD is mode dependent:

- DU is input, DD is output (TE and LT-T)
- DU is output, DD is input (LT-S)

In LT-S and LT-T mode the EAW pin is used as the second mode pin.

Table 2
Mode Setting

	MODE0	MODE1/ EAW	Transmit-data on S interface	Receive-data from S interface
TE-mode	0	EAW	DU	DD
LT-T mode	1	1	DU	DD
LT-S mode	1	0	DD	DU

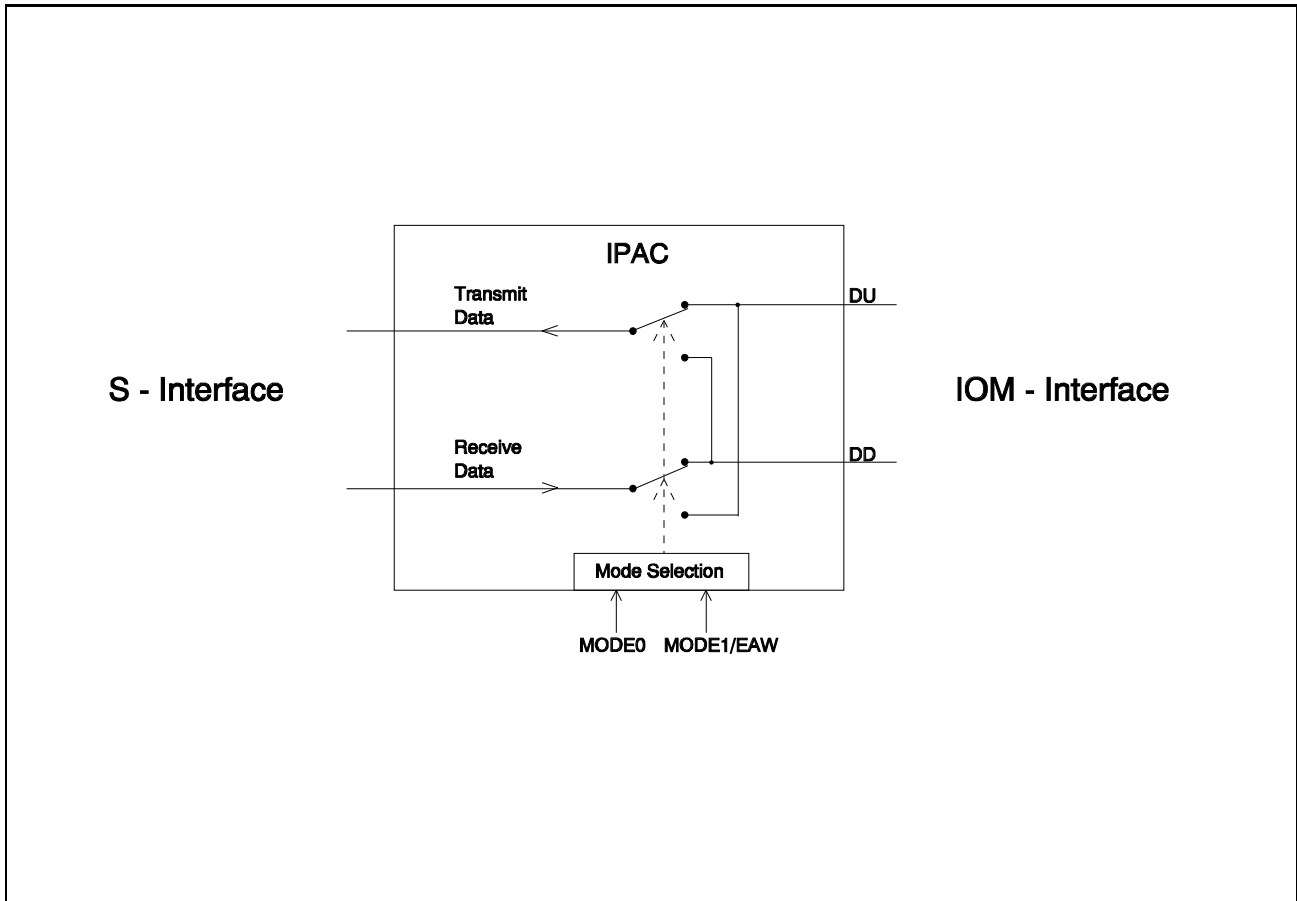**Figure 8**
Data path switching

2.2   Auxiliary Interface

The AUX interface provides for various, mode dependent functions (see table 3).

For all modes two pins can be used as programmable I/O with optional interrupt input capability.

In TE mode two pins are used for the DMA interface (DRQTA, DRQTB), the remaining pins are programmable as I/O.

In LT modes three pins are used to select one of eight timeslots on the IOM-2 interface by pin strapping. Two PCM receive and transmit lines are available for connection to other data controllers (e.g. datapump, video processor). In this way non IOM compatible devices with standard PCM interface can operate on any timeslot on the IOM-2 interface. A BCL output or FSC output (for IOM-2 frame sync signal) is available which is derived from the DCL input by an internal divider.
The PCM interface can be disabled, so AUX3-5 are available as general I/O pins.

Table 3
AUX pin functions

Pin	TE mode	LT-T mode	LT-S mode
AUX0	DRQTA	CH0	CH0
AUX1	DRQRA	CH1	CH1
AUX2	AUX2	CH2	CH2
AUX3	AUX3	AUX3 / FBOUT	AUX3 / FBOUT
AUX4	AUX4	AUX4 / PCMIN	AUX4 / PCMIN
AUX5	AUX5	AUX5 / PCMOUT	AUX5 / PCMOUT
AUX6	INT0	INT0	INT0
AUX7	INT1	INT1	INT1

AUX2..5

These pins are programmable as input or output lines, for the latter case open drain or push pull is selectable.

INT0, 1

The INTx pins are general I/O pins like AUX2..5. In addition to that, as inputs they can generate a maskable interrupt to the host. The interrupt input is either negative edge or negative level triggered (programmable).
As outputs both pins are able to drive $I_{OL} = 5$ mA which allows for direct connection of LEDs in standalone applications for example.

PCMIN, PCMOUT

PCMx are receive and transmit lines of the general PCM interface. If enabled, any timeslot on PCMIN/OUT can flexibly be switched to the B-channels on DU and DD of the IOM-2 interface.

FBOUT (FSC/BCL Output)

In LT-T and LT-S mode this pin can be programmed to one of two functions:
It can either output an FSC clock which is derived from the DCL input divided by 192. This is especially suitable for multiline applications, where one of several IPACs generates the common FSC.

Or it can output a single bit clock equal to the IOM-2 data rate, especially to serve non IOM-2 compatible peripheral devices on the PCM interface.

DRQTA, DRQRA

In TE mode these two pins are additionally required for the DMA interface, so both B-channels can be operated in DMA mode. In the LT modes only channel B can be operated by DMA data transfer.

CH0, CH1, CH2

In LT-T and LT-S mode one of 8 channels on the IOM-2 interface is selected. These pins must be strapped to '1' (VDD) or '0' (VSS) according to table 4.

Table 4
IOM-2 channel selection

CH2	CH1	CH0	Channel on IOM-2	Bit No.	Minimum Frequency of DCL (kHz)
0	0	0	0	0 ... 31	512
0	0	1	1	32 ... 63	1024
0	1	0	2	64 ... 95	1536
0	1	1	3	96 ... 127	2048
1	0	0	4	128 ... 159	2560
1	0	1	5	160 ... 191	3072
1	1	0	6	192 ... 223	3584
1	1	1	7	224 ... 255	4096

2.3   PCM Interface

In LT-S and LT-T mode the IPAC can be connected to devices in general TDM systems through its standard PCM interface. In this way data controllers, which are not IOM-2 compatible, can indirectly be connected to the IOM-2 interface, since the used PCM timeslots are reflected in B1 and B2 of the selected IOM-2 channel.

Figure 9 shows as an example, the switching of timeslots from the PCM lines to the data upstream and data downstream lines of IOM-2 channel B1.

For both, B1-channel and B2-channel one of up to 32 channels on the PCM interface is selected for transfer of B-channel data between the IOM-2 interface and the PCM interface.

By default, for receive data (transmitted from a peripheral device) PCMIN is connected to DU and for transmit data (received by a peripheral device) PCMOUT is connected to DD. However, they can also be programmed vice versa for test loops or to exchange data with other devices on the IOM-2 interface.
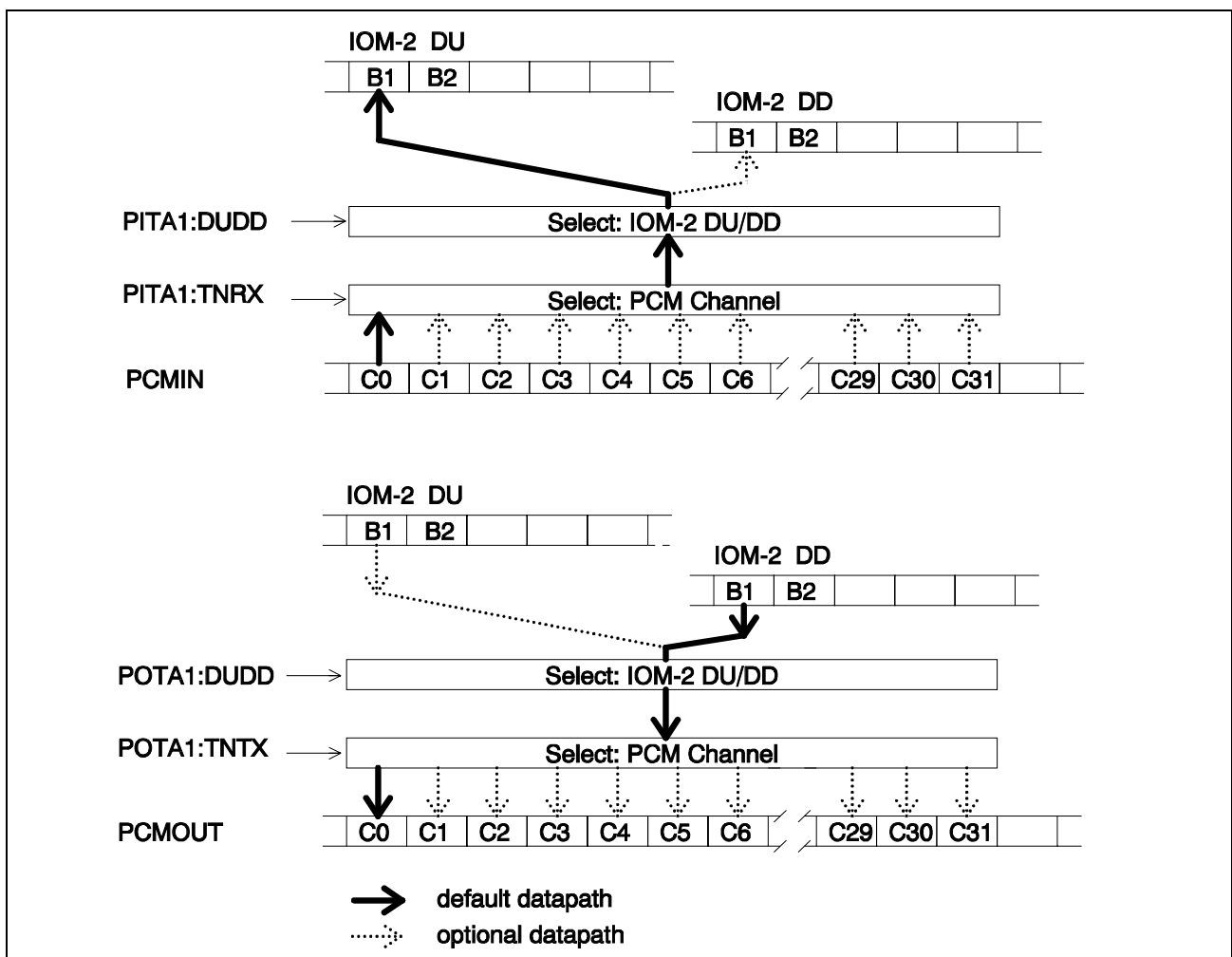

Figure 9
Switching of PCM timeslots on IOM-2 Channel B1

2.4 Host Interface

2.4.1 Register Set

The communication between the host and the IPAC is done via a set of directly or indirectly accessible 8-bit registers. The host sets the operating modes, controls function sequences and gets status information by writing or reading these registers (Command/ Status transfer).
Each of the two B-channels of the IPAC is controlled via an equal, but totally independent register file (channel A and channel B). Additional registers are available for D-channel control, the PCM and the Auxiliary interface.

2.4.2 Data Transfer Mode

Data transfer between the system memory and the IPAC for both transmit and receive direction is controlled by either interrupts (Interrupt Mode), or independently from host interaction using the IPAC's 4-channel DMA interface (DMA Mode).

After RESET, the IPAC operates in Interrupt Mode, where data transfer must be done by the host. The user selects the DMA Mode by setting the DMA bit in a register. In TE mode both channels can independently be operated in either Interrupt or DMA Mode (e.g. Channel A in DMA mode, Channel B in interrupt mode). In LT-S and LT-T mode, only channel B can be operated either in Interrupt or DMA mode, channel A can only be operated in Interrupt mode.

2.4.3   Interrupt Interface

Special events in the IPAC are indicated by means of a single interrupt output, which requests the host to read status information from the IPAC or transfer data from/to the IPAC.

Since only one $\overline{\text{INT}}$ request output is provided, the cause of an interrupt must be determined by the host reading the IPAC's interrupt status registers.

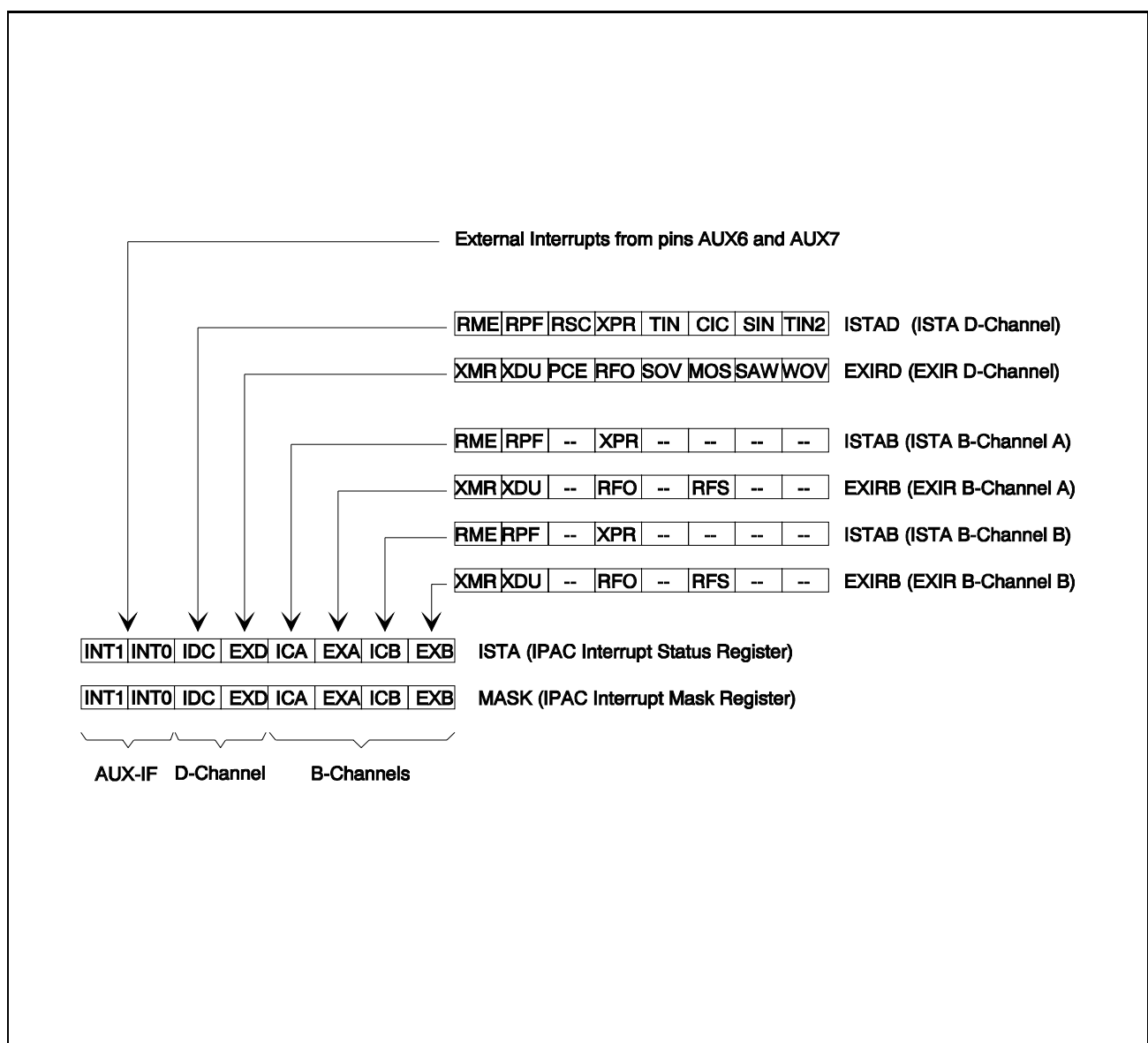The structure of the interrupt status registers is shown in figure 10.

Figure 10
IPAC Interrupt Status Registers

Two interrupt indications can be read directly from the ISTA register and another six interrupt indications from separate interrupt status registers and extended interrupt registers for the B-channels (ISTAA, EXIRA, ISTAB, EXIRB) and the D-channel (ISTAD, EXIRD).

After the IPAC has requested an interrupt by setting its $\overline{\text{INT}}$ pin to low, the host must first read the IPAC interrupt status register (ISTA) in the associated interrupt service routine. The six lowest order bits (bit 5-0) of ISTA (ICD, EXD, ICA, EXA, ICB, EXB) point to those registers in which the actual interrupt source is indicated. It is possible that several interrupt sources are indicated referring to one interrupt request (e.g. if the ICA bit is set, at least one interrupt is indicated in the ISTA register of channel A).

An interrupt source from the general I/O pins AUX6 and AUX7 of the auxiliary interface is directly indicated in bits 6 and 7 of the ISTA register, therefore these bits must always be checked.

The $\overline{\text{INT}}$ pin of the IPAC remains active until all interrupt sources are cleared by reading the corresponding interrupt register. Therefore it is possible that the $\overline{\text{INT}}$ pin is still active when the interrupt service routine is finished.

For some interrupt controllers or hosts it might be necessary to generate a new edge on the interrupt line to recognize pending interrupts. This can be done by masking all interrupts at the end of the interrupt service routine (writing FF_H into the MASK register) and write back the old mask to the MASK register.

Each interrupt indication of the interrupt status registers can selectively be masked by setting the respective bit in the MASK register. Masked interrupt status bits are not indicated when the status register is read, but they remain internally stored and pending until the mask bit is reset.

2.4.4   DMA Interface

The IPAC comprises a 4-channel DMA interface (2 B-channels with receive and transmit direction) for fast and effective data transfer.

For both serial channels, a separate DMA Request Output for transmit (DRQT) and receive direction (DRQR) as well as a DMA Acknowledgment ($\overline{DACK}$) input is provided.

The IPAC activates the DRQ line as long as data transfer is needed from/to the specific FIFO (level triggered demand transfer mode of DMA controller).

It's the responsibility of the DMA controller to perform the correct amount of bus cycles. Either read cycles will be performed if the DMA transfer has been requested from the receiver, or write cycles if DMA has been requested from the transmitter. If the DMA controller provides a DMA acknowledge signal (input to the IPAC's $\overline{DACK}$ pin), each bus cycle implicitly selects the top of the specific FIFO and neither address (via A0-A6) nor chip select need to be supplied (I/O to memory transfers). If no $\overline{DACK}$ signal is supplied, normal read/write operations (providing addresses) must be performed (memory to memory transfers).

The IPAC deactivates the DRQ line immediately after the last read/write cycle of the data transfer has started.

The IPAC supports target synchronous as well as source synchronous DMA transfer. In source synchronous DMA transfer mode a DMA cycle is started when an active level occurs at the DMA request line. This request is controlled by the source (transfer peripheral device $\rightarrow$ memory).

First of all the data is read out of the peripheral device. During the second DMA clock cycle it is written into the memory according to the target address.

If there is target synchronous DMA transfer, the DMA cycle is started when there is an active level on the DMA request line. The request is controlled by the target (transfer memory $\rightarrow$ peripheral device).

First of all the data is read from the memory. During the second DMA clock cycle it is written into the peripheral IC. The DMA request line continues being activated until it is reset by a write cycle to a peripheral device.

2.4.5   Host Interface Operation

The IPAC is programmed via an 8-bit parallel microprocessor interface. Easy and fast microprocessor access is provided by 8-bit address decoding on the chip.

At the IPAC three types of µP buses are provided (see table 5), which are selected via pin ALE:

Table 5
Bus Operation Modes

(1)	ALE tied to V_{DD}	**Motorola** type with control signals $\overline{CS}$, $R/\overline{W}$, $\overline{DS}$
(2)	ALE tied to V_{SS}	**Siemens/Intel non-multiplexed** bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$
(3)	Edge on ALE	**Siemens/Intel multiplexed** address/data bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, **ALE**

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

*Note: If the multiplexed address/data bus type (3) is selected, the unused address pins
A0-A7 must be tied to V_{DD}.*

Register Addressing Modes

The IPAC provides two different ways to read and write its registers. The common way is for non-multiplexed mode to set the register address to the address bus and then access the register location. In multiplexed mode, the address on the address/data bus is latched in, before a read or write access to the register is performed. This mode is selected, if the address select mode pin AMODE is set to 0.

As a second option, the IPAC allows for indirect access of the registers (AMODE=1). Only the LSB (A0) of the address line is used to select either the ADDRESS register or the DATA register. The host writes the register address to the ADDRESS register, before it reads/writes data from/to the corresponding register location through the DATA register. Figure 11 shows both register addressing modes.
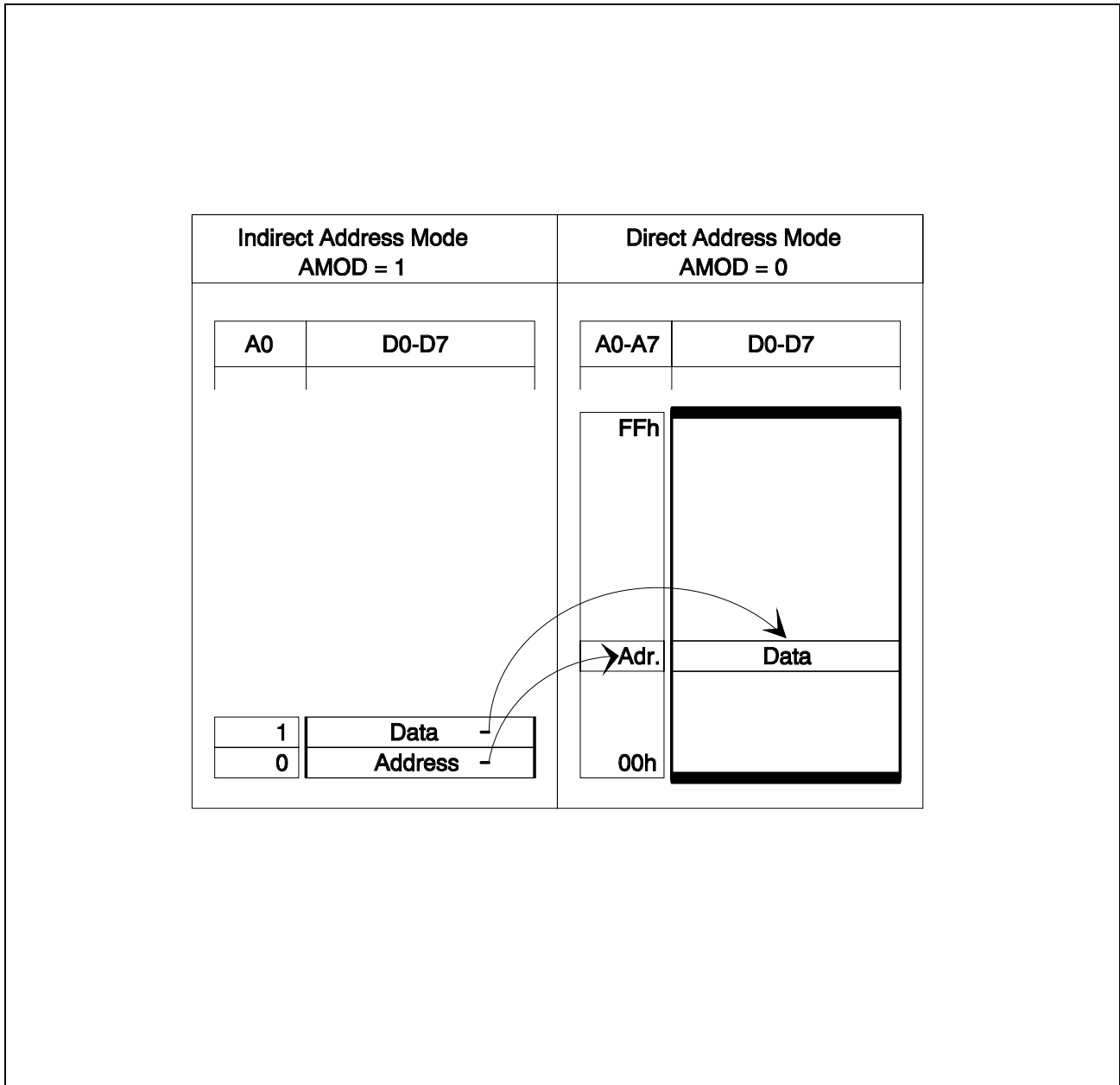
Figure 11
Indirect register address mode

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

| Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias:	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	6	V

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.2 DC-Characteristics

Parameter	Symbol	Limit Values		Unit	Condition
		min.	max.		
L-input voltage	V_{IL}	-0.4	0.8	V	(all pins except SR1/2, XTAL1/2)
H-input voltage	V_{IH}	2.0	V_{DD} + 0.4	V	
L-output voltage	V_{OL}		0.45	V	I_{OL}= 7 mA (DU, DD) I_{OL}= 5 mA ($\overline{ACL}$, AUX6, 7) I_{OL}= 2 mA (all others)
H-output voltage	V_{OH}	2.4		V	I_{OH}= -400 µA
H-output voltage	V_{OH}	V_{DD} - 0.5		V	I_{OH}= -100 µA

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25°C$ and the given supply voltage.

4 Package Outlines
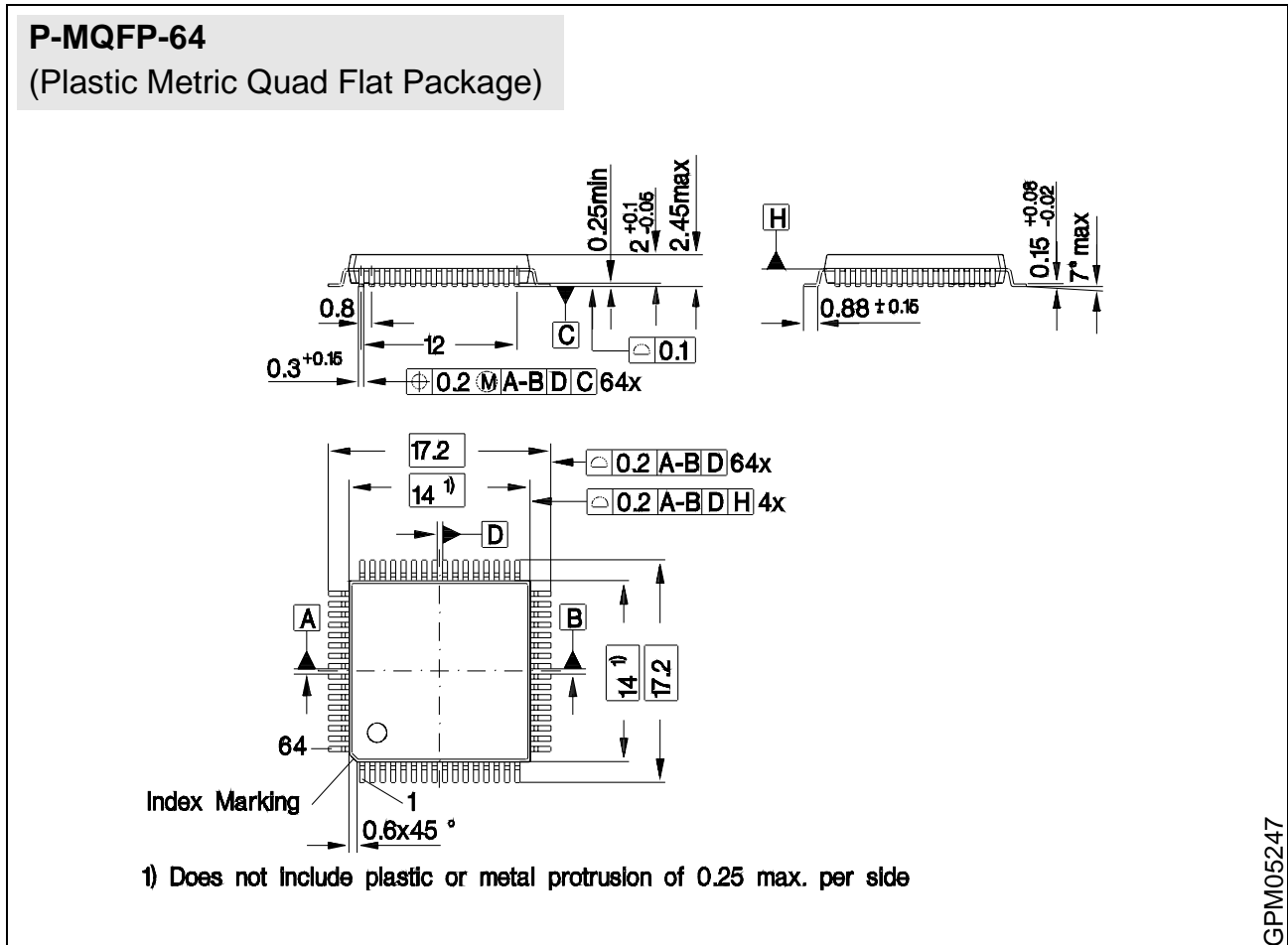
P-MQFP-64
(Plastic Metric Quad Flat Package)

Index Marking
1) Does not include plastic or metal protrusion of 0.25 max. per side
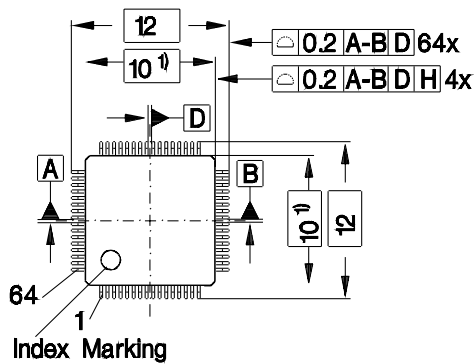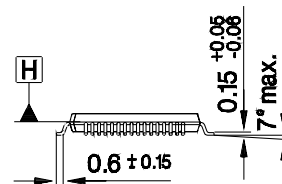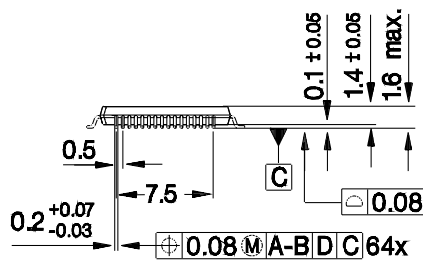
GPM05247

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

P-TQFP-64
(Plastic Thin Quad Flat Package)

1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05613

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm